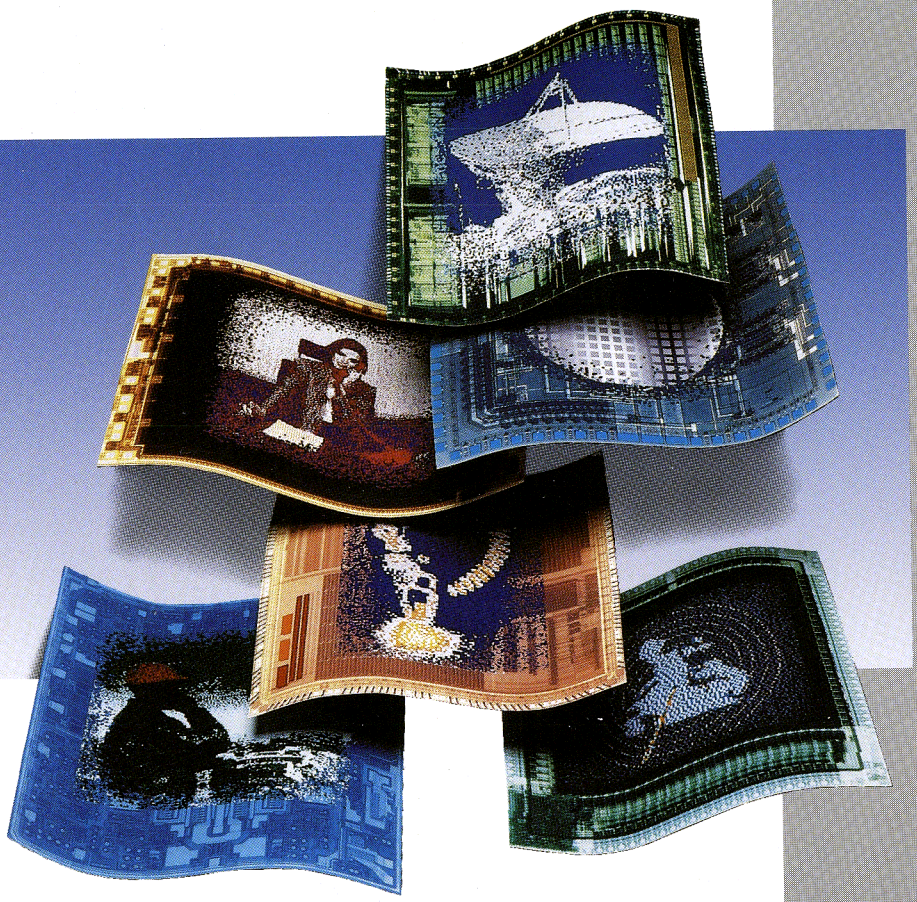
Media

IC Handbook

October 1996



GEC PLESSEY
SEMICONDUCTORS

DATASHEET ANNOTATION

GPS annotate datasheets in the top right hand corner of the first page, to indicate product status. These annotations are as follows:-

TARGET SPECIFICATION

This is the most tentative form of information and represents a very preliminary product specification. No actual design work on the product has started.

PRELIMINARY INFORMATION

The product is in design and development. The datasheet represents the product as it is understood but details may change.

ADVANCE INFORMATION

The product design is complete and final characterisation for volume production is well in hand.

No annotation

The product parameters are fixed and the product is available to datasheet specification in volume.

If you have any queries about the status of any GPS product, please contact your nearest GPS Customer Service Centre.

MEDIA

IC Handbook

GEC PLESSEY

SEMICONDUCTORS

Foreword

Digital television will provide more choice, new services and new ways for the viewer to access information. Initially, this will be done via the set top box.

GEC Plessey Semiconductors (GPS) is totally committed to the set top box market, bringing to it established skills in RF, data conversion and digital signal processing, in order to supply chipsets for the front and back end of such boxes.

Front end:
- Satellite tuner IC
- IQ down-converters
- PLL frequency synthesiser
- ADCs
- QPSK/FEC

Back end:
- MPEG2 A/V chip
- ARM RISC microprocessor
- Video encoder family
- Audio DAC

GPS's high performance building block and algorithm specific DSPs continue to be very popular with designers. Reflecting that demand, some devices have been migrated to newer processes to enhance their performance and allow us to offer even more competitive pricing. Our H.261 chipset provides superior performance for Video Conferencing systems which demand the best quality at the highest data rates while remaining a cost effective solution for PC add-in card Videophone designs. GPS has also just introduced the VP7615 decoder IC which directly supports iVision™ compatible digital cameras. This chip is very much targeted at videophone and other PC-based video communication applications where it can offer improved quality at lower cost than conventional analog solutions.

iVision™, iCam™, CamPort™ and iCamHost™ are trademarks of Silicon Vision, Inc., Fremont, CA.

Contents

Product index

TV/Cable/Satellite Tuner PLL Circuits[1]

Type No.	Function	Frequency	Page
SP5026	SP5510 pin/Toshiba TDA6380, TD6382 function compatible synthesiser	1.0GHz	11
SP5054	3-Wire bus controlled synthesiser	2.6GHz	18
SP5055[2]	Higher frequency version of SP5510	2.6GHz	25
SP5070	Fixed modulus frèquency synthesiser for satellite receivers	2.4GHz	32
SP5502[2]	Bi-directional I²C bus 4-address synthesiser	1.3GHz	36
SP5510[2]	Bi-directional I²C bus controlled synthesiser	1.3GHz	42
SP5511[2]	Bi-directional I²C bus controlled synthesiser	1.3GHz	50
SP5512[2]	Bi-directional I²C bus controlled synthesiser	1.3GHz	58
SP5654	3-Wire bus controlled synthesiser	2.7GHz	66
SP5655[2]	Bi-directional I²C bus controlled synthesiser	2.7GHz	74
SP5657	3-Wire bus controlled synthesiser	2.7GHz	85
SP5658	3-Wire bus controlled synthesiser with low phase noise	2.7GHz	94
SP5659[2]	Bi-directional I²C bus controlled synthesiser with low phase noise	2.7GHz	105

NOTES
1. All are bipolar ICs and operate from a single +5V supply.
2. Purchase of GEC Plessey Semiconductors' I²C components conveys a licence under the Philips I²C Patent Rights to use these components in I²C systems, provided that the systems conform to the I²C Standard Specification as defined by Philips.

Satellite TV Receiver Circuits

Type No.	Function	Supply voltage (V) (typ)	Sample Frequency	Process	Page
VP211	6-Bit dual ADC	5	90ms/s	Bipolar	119
VP213	6-Bit dual ADC	5	90ms/s	Bipolar	125
VP215	6-Bit dual ADC	5	90ms/s	Bipolar	131
VP216	6-Bit dual ADC with VCO	5	90ms/s	Bipolar	137

Type No.	Function	Supply voltage (V) (typ)	IF Frequency (MHz)	Process	Page
SL1461SA	Wideband PLL FM demodulator	5	300-800	Bipolar	143
SL1710	IQ demodulator	5	300-800	Bipolar	154

Teletext and TV Signal Generators

Type No.	Function	Supply	Process	Page
MV1815	625-line single chip teletext decoder, x 1 DRAM	5V	CMOS	163
MV1817	625-line single chip teletext decoder, x 4 DRAM	5V	CMOS	178
MV1820	Video programme delivery control interface circuit	5V	CMOS	197
MV1821	Video cassette recorder PDS and VPS interface circuit	5V	CMOS	202
MV1822	PDC, VPS and time receiver	5V	CMOS	209

Video Compression

Type No.	Function	Clock	Page
VP2611	H.261 encoder	27MHz	221
VP2612	Video multiplexer	27MHz	233
VP2614	H.261 video de-multiplexer	27MHz	242
VP2615	H.261 decoder	27MHz	251
VP520S	PAL/NTSC to CIF/QCIF converter	27MHz	260

Digital Video

Type No.	Function	Clock	Page
VP510	Bi-directional colour space converter	27MHz	283
VP5311A	NTSC/PAL digital video encoder	27MHz	294
VP531D	NTSC/PAL digital video encoder	27MHz	309
VP5511A	NTSC/PAL digital video encoder	27MHz	322
VP551D	NTSC/PAL digital video encoder	27MHz	336
VP7615	Colour digital video camera decoder	30MHz	349

Building block DSP ICs

Type No.	Function	Speed	Page
PDSP1601A	ALU and barrel shifter	20MHz	367
PDSP16112/A	Complex multiplier (16x12 bits)	20MHz	383
PDSP16116/A	Complex multiplier (16x16 bits)	20MHz	390
PDSP16318/A	Complex accumulator	20MHz	405

Algorithm specific DSP ICs

Type No.	Function	Speed	Page
PDSP16256/A	Programmable FIR filter	25MHz	415
PDSP16330/A/B	Pythagoras processor	25MHz	433
PDSP16350	I/Q splitter/NCO	20MHz	440
PDSP16488A	Single-chip 2D convolver	40MHz	451
PDSP16510A	Stand alone FFT processor	40MHz	480
PDSP16515A	Stand alone FFT processor with enhanced accuracy	40MHz	502
VP16256	Low cost alternative to PDSP16256/A	40MHz	524

Product List - Alpha numeric

Section 1
Tuner PLL Circuits

GEC PLESSEY
SEMICONDUCTORS

SP5026

1.0 GHz 3–WIRE BUS CONTROLLED SYNTHESISER

(Supersedes September 1992 edition)

The SP5026 is a programming variant of the SP5510, allowing the design of one tuner with either I^2C bus or 3–wire bus format depending on which device is inserted. The SP5026, when used with a TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divider–by–8 prescaler with its own preamplifier and a15–bit programmable divider controlled by a serially–loaded data register. Four open–collector outputs, each independently programmable, are included. The device has two modes of operation, selected by the 'mode select' input. In mode 1, the comparison frequency is 7.8125kHz and the programmable divider MSB is bypassed; mode 2 comparison frequency is 3.90625kHz. The comparison frequencies are both obtained from a 4MHz crystal controlled on–chip oscillator. The comparator has a charge pump output with an amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

FEATURES

- Complete 1.0GHz Single Chip System
- Dual Standard 62.5kHz or 31.25 kHz Step Size
- Low power Consumption (5V 40mA)
- Function Compatible with Toshiba TD6380 and TD6382*
- Pin Compatible with SP5510 *
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- Charge Pump Disable
- Single Port 18/19 Bit Serial Data Entry
- Four Controllable Outputs
- ESD Protection †

* See notes on pin compatibility on page 4
† Normal ESD handling procedures should be observed

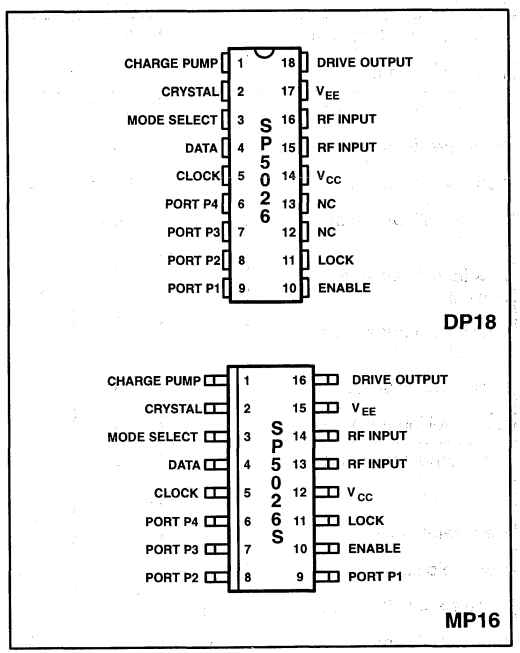


Fig. 1 Pin connections – top view

APPLICATIONS

- Satellite TV when combined with SP4902 2.5GHz prescaler
- Cable tuning systems
- VCRs

ORDERING INFORMATION

SP5026 DP – (18 lead Plastic Package)
SP5026S MP – (16 lead Miniature Plastic Package)

ELECTRICAL CHARACTERISTICS

T_{amb}= −20°C to +80°C, V_{CC}=+4.5V to +5.5V. Frequency Standard = 4MHz. Pin numbers refer to SP5026 (DP package) These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	14		40	55	mA	V_{CC}=5V
Prescaler		15, 16	12.5		300	mV_{RMS}	50MHz to 1GHz sinewave
Prescaler input impedance		15, 16		50		Ω	
Input capacitance				2		pF	
High level input voltage		4, 5, 10	3		V_{CC}	V	
High level input voltage		3	4		V_{CC}	V	
Low level input voltage		3,4,5,10	0		0.7	V	
High level input source current		4, 5, 10			1	µA	V_{IN}=5.5V, V_{CC}=5.5V
Low level input source current		5			5	µA	V_{IN}=0V, V_{CC}=5.5V
Low level input source current		4, 10			250	µA	V_{IN}=0V, V_{CC}=5.5V
High level input sink current		3			150	µA	V_{IN}=5.5V, V_{CC}=5.5V
Low level input sink current		3			1	µA	V_{IN}=0V, V_{CC}=5.5V
Clock input hysteresis		5		0.4		V	
Clock rate		5			0.5	MHz	
Data setup time	t_2	4	300			ns	See Fig,3
Data hold time	t_3	4	600			ns	See Fig. 3
Enable setup time	t_1	10	300			ns	See Fig. 3
Enable hold time	t_5	10	600			ns	See Fig.3
Clock–to–enable time	t_4	10	300			ns	See Fig. 3
Charge pump output current		1		±150		µA	V pin 1=2.0V
Charge pump output leakage current		1			±5	nA	V pin 1=2.0V
Drift due to leakage					5	mV/s	At collector of external varicap drive transistor
Charge pump drive output current		18	1			mA	V pin 18=0.7V
Charge pump amplifier gain				6400			Pin 18 current =100µA
Oscillator temperature stability					2	ppm/°C	
Oscillator stability with supply voltage					2	ppm/V	
Recommended crystal series resistance			10		200	Ω	"Parallel resonant crystal". Figure quoted is under all conditions including startup
Crystal oscillator drive level		2		40		mV p–p	
Crystal oscillator source impedance		2		−400		Ω	Normal spread ±15%
Port and lock sink current		6–9, 11	10			mA	V_{OUT}=0.7V

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb}= –20°C to +80°C, V_{CC}= +4.5V to +5.5V. Frequency Standard = 4MHz. Pin numbers refer to SP5026 (DP package) These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Port leakage current		6–9			10	µA	V_{OUT}=13.2V
Lock leakage current		11			10	µA	V_{OUT}=V_{CC}
Varactor drive amp. disable		10	350			µA	V_{OUT}<0V. Current sourced from device
Charge pump disable		4	350			µA	V_{OUT}<0V. Current sourced from device

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE}=0V

Parameter	Pin SP5026	Pin SP5026S	Value		Units	Conditions
			Min	Max		
Supply voltage	14	12	–0.3	6	V	
Prescaler inputs	15, 16	13, 14		2.5	Vp–p	
Output ports	6–9	6–9	–0.3	14	V	Port in off state
			–0.3	6	V	Port in on state
Total port output current	6–9	6–9		50	mA	
Prescaler DC offset	15, 16	13, 14	–0.3	V_{CC}+0.3	V	
Loop amplifier DC offset	1, 18	1, 16	–0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	2	–0.3	V_{CC}+0.3	V	
Data bus inputs	4, 5, 10	4, 5, 10	–0.7	V_{CC}+0.3	V	With V_{CC} applied
Storage temperature			–55	+125	°C	
Junction temperature				+150	°C	
DP18 thermal resistance, chip–to–ambient				78	°C/W	
DP thermal resistance, chip–to–case				24	°C/W	
MP16 thermal resistance, chip–to–ambient				111	°C/W	
MP16 thermal resistance, chip–to–case				41	°C/W	
Power consumption at 5V				275	mW	All ports off

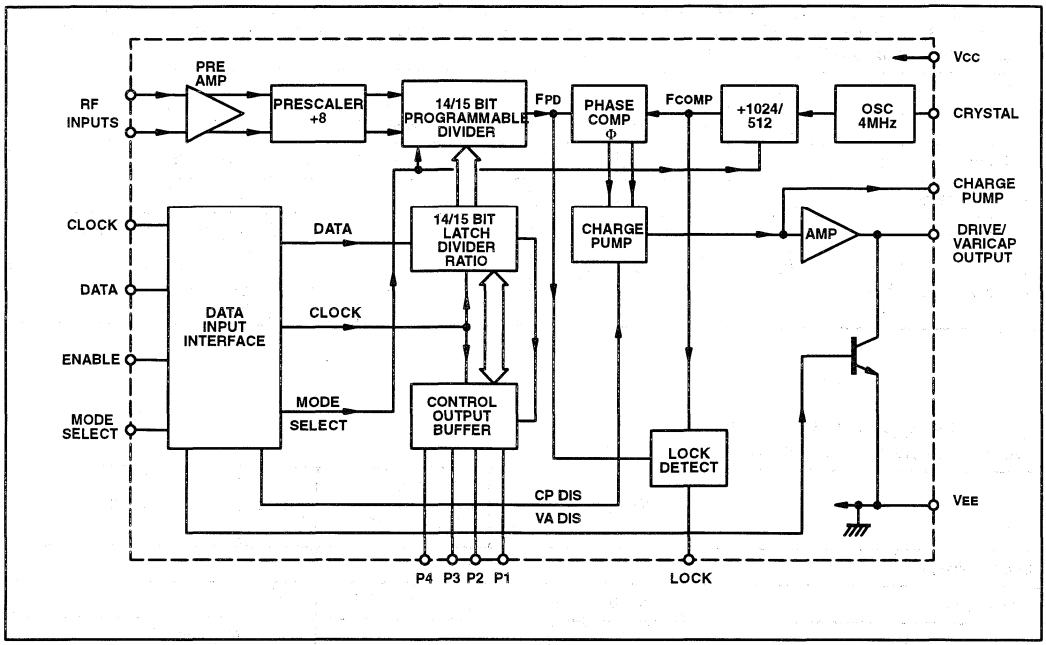


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The SP5026 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard data, clock enable three–wire bus. The data load normally consists of a single word, which contains the frequency and port information and is only transferred to the internal data shift register during an enable high period. The clock is disabled during low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable, so giving improved fine tune facility for digital AFC etc.

The data sequence and timing follows the format as displayed in Fig. 3

The frequency is set by loading the programmable divider with the required 14/15–bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator, where it is compared in phase and frequency domain to the internally generated comparison frequency, F_{COMP}.

The F_{COMP} is obtained by dividing the output of an on–chip crystal controlled oscillator. the crystal frequency used is generally 4MHz which gives an F_{COMP} of 3.90625kHz/7.8125kHz. When multiplied back up to the LO this gives a minimum step size of 31.25kHz/62.5kHz, respectively.

The programmable diver is preceded by an input RF preamplifier and high speed low radiation prescaler. The preamplifier is arranged to be self–oscillating, so giving excellent input sensitivity. The input sensitivity and impedance are shown in Figs. 5 and 7, respectively.

The SP5026 contains an improved lock detect circuit which generates a flag when the loop has attained lock. 'Out of lock' is indicated by a high impedance state.

The SP5026 contains four general–purpose open collector outputs, ports P1 – P4, which are capable of sinking at least 10mA. These outputs are set by the remaining four bits within the data word.

PIN COMPATIBILITY

The SP5026 may by used in SP5510 applications which require 3–wire bus as opposed to I^2C bus data format. In SP5510 applications where the reference crystal is grounded to pin 3, a small modification is required to ground the crystal as shown in Fig.4.

Appropriate connections to the mode select input (pin 3) must also be made.

With pin 3 'HIGH (mode 1) the SP5026 is function compatible with the Toshiba TD6380; with pin 3 'LOW' (mode 2) it is compatible with the TD6382.

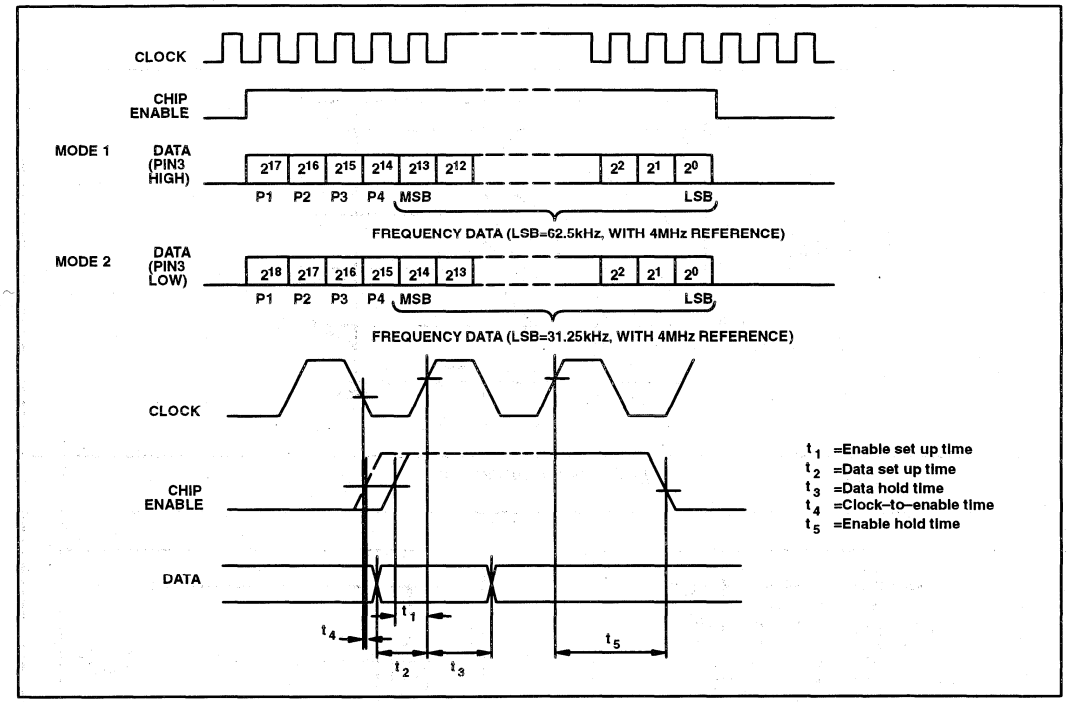


Fig. 3 Data format and timing

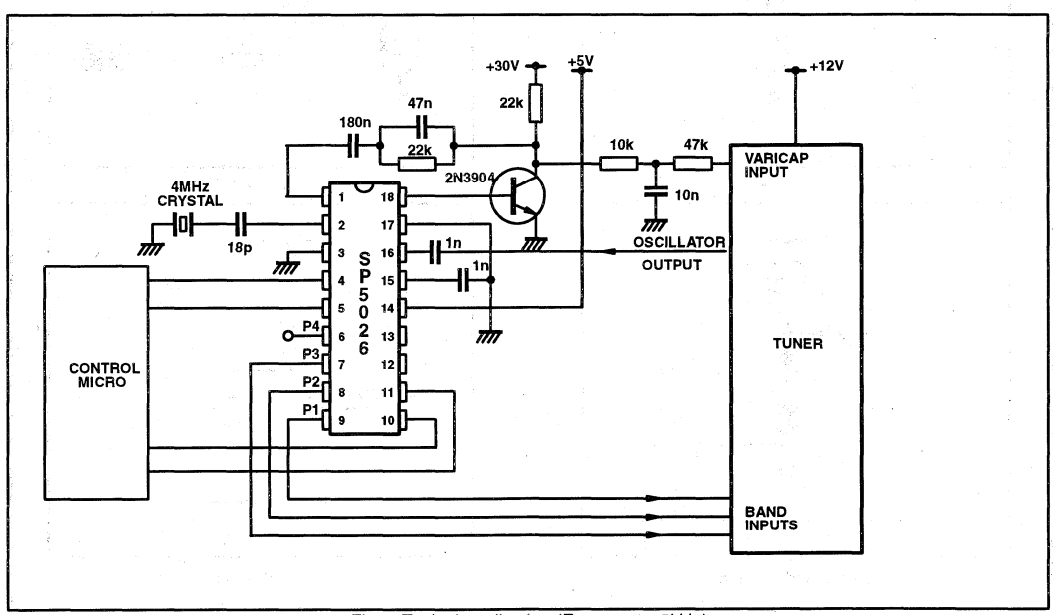


Fig. 4 Typical application (F_{STEP}=31.25kHz)

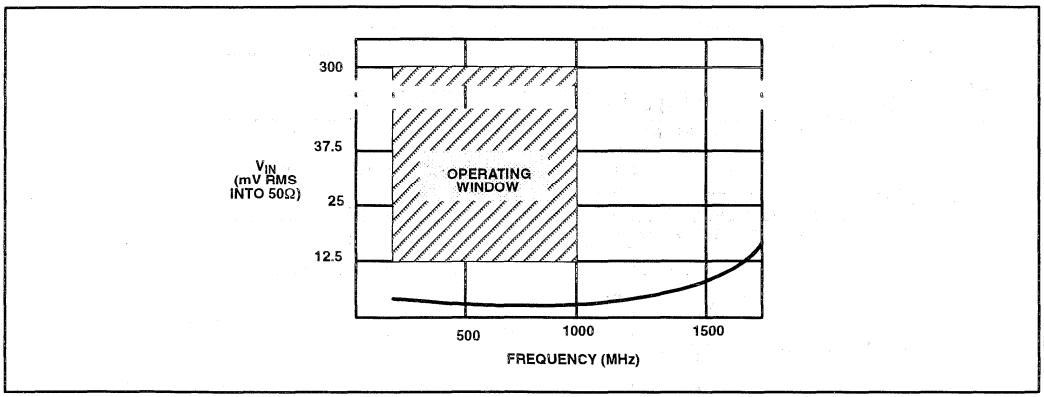


Fig. 5 Typical input sensitivity

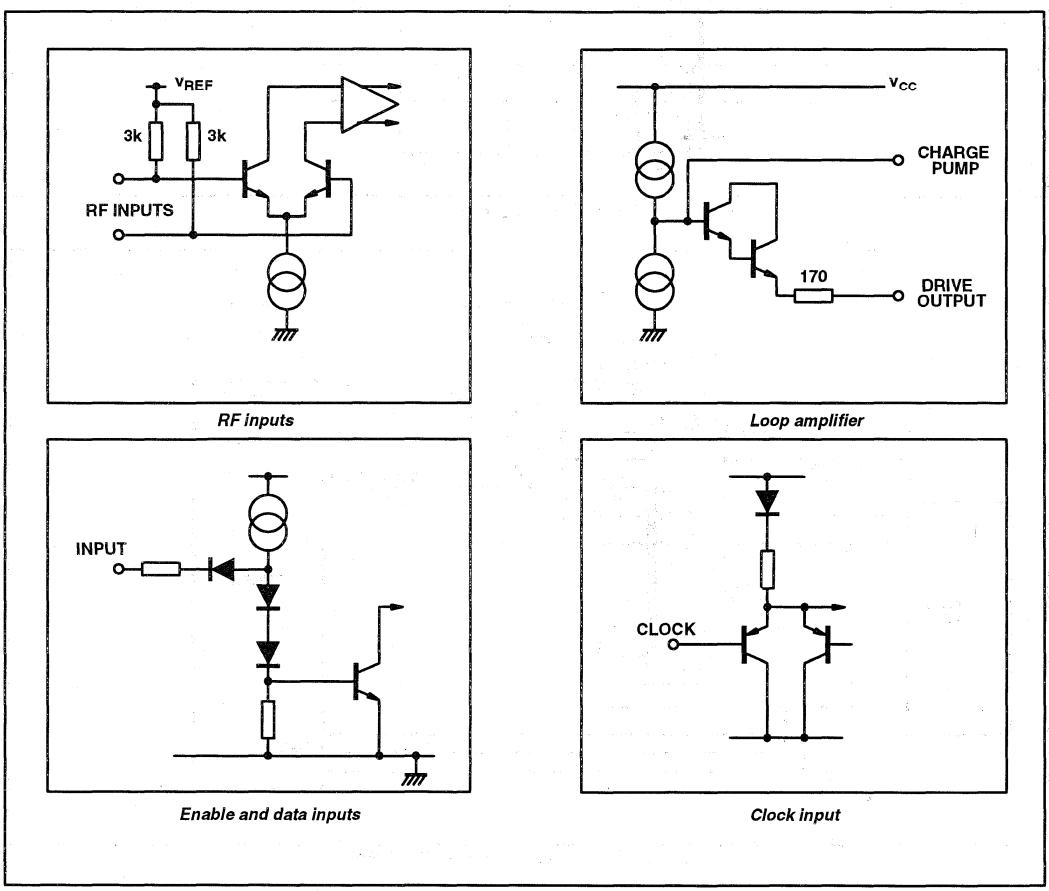


Fig. 6a Input /output interface circuits

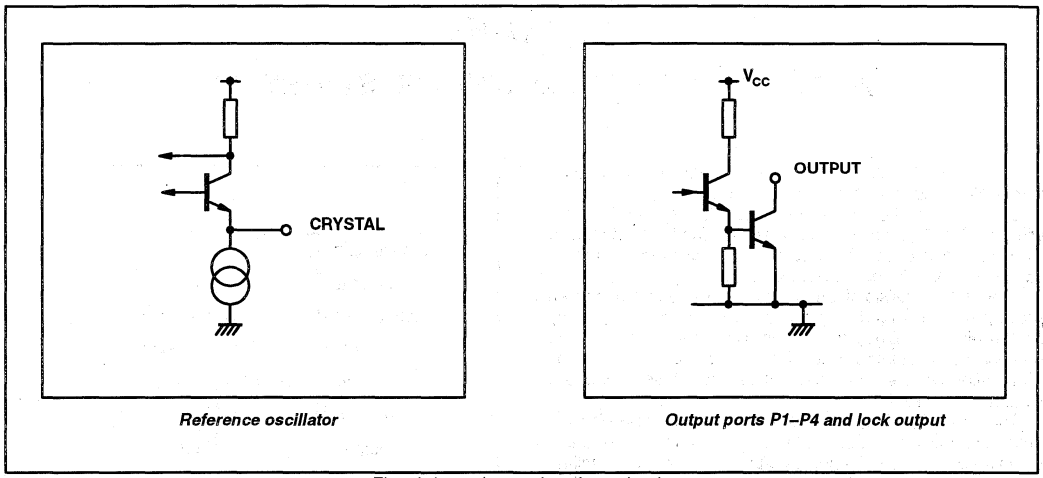


Fig. 6b Input /output interface circuits

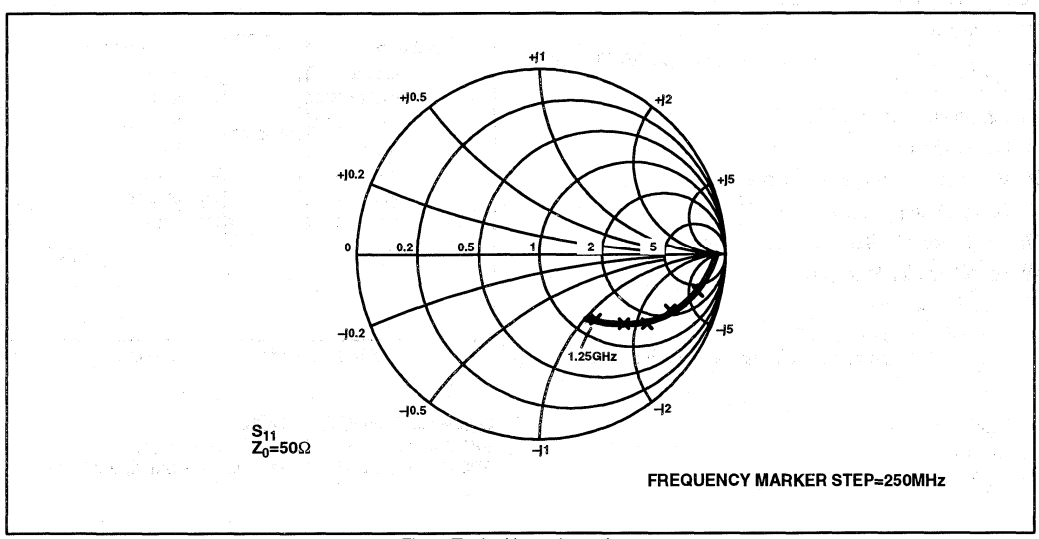


Fig. 7 Typical input impedance

3048-3.4

SP5054

2·6 GHz 3-WIRE BUS CONTROLLED SYNTHESISER

The SP5054 is a single-chip frequency synthesiser designed for satellite TV tuning systems. It is a programming variant of the SP5055, allowing the design of one tuner with either I^2C bus or 3-wire bus format, depending on which device is inserted. The SP5054, when used with a satellite varactor tuner, forms a complete phase locked loop tuning system.

The circuit consists of a divide-by-16 prescaler with its own preamplifier and a 14/15-bit programmable divider controlled by a serially-loaded data register. Four independently programmable open-collector outputs are included. The device has four modes of operation, selected by the Mode Select input; these modes are summarised in Table1.

The comparison frequencies are obtained by the division of the output of a 4MHz crystal controlled on-chip oscillator. The phase comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varactor line driving.

FEATURES

- Complete 2·6GHz Single Chip System
- 62·5kHz, 100kHz and 125kHz Step Size
- Low Power Consumption (325mW Typ.)
- Programming Compatible with Toshiba TD6380, TD6381 and TD6382*
- Pin Compatible with SP5055*
- Low Radiation
- Varactor Drive Amplifier Disable
- Charge Pump Disable
- Single Port 18/19 Bit Serial Data Entry
- Four Controllable Outputs
- ESD Protection†

* See notes on pin compatibility
† Normal ESD handling precautions should be observed

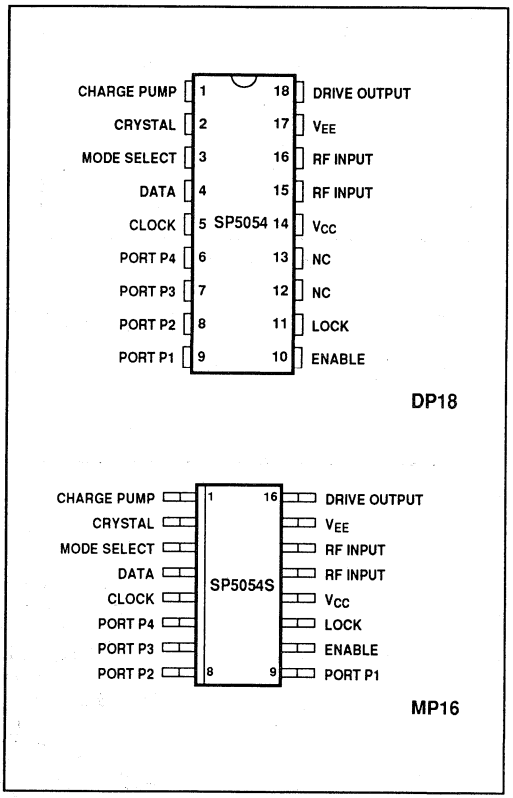


Fig. 1 Pin connections – top view

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

ORDERING INFORMATION

SP5054 KG DPAS (18-lead plastic package)
SP5054S KG MPAS (16-lead miniature plastic package)

ELECTRICAL CHARACTERISTICS

T_{AMB} = −20°C to +80°C, V_{CC} = +4·5V to +5·5V. Frequency standard = 4MHz. All pin connections refer to DP package. These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	14		65	80	mA	V_{CC} = 5V
Prescaler input voltage	15,16	50		400	mVrms	500MHz to 2·6GHz sinewave
Prescaler input voltage		100		400	mVrms	120MHz and 500MHz, see Fig. 6
Prescaler input impedance	15,16		50		Ω	
Input capacitance			2		pF	
High level input voltage	4,5,10	3		V_{CC}	V	
Low level input voltage	4,5,10	0		0·7	V	
High level input current	4,5,10			1	µA	V_{IN} = 5·5V, V_{CC} = 5·5V
Low level input current	5			5	µA	V_{IN} = 0V, V_{CC} = 5·5V
Low level input current	4,10			−250	µA	V_{IN} = 0V, V_{CC} = 5·5V
High level input current	3			700	µA	V_{IN} = 5·5V, V_{CC} = 5·5V
Low level input current	3			−700	µA	V_{IN} = 0V, V_{CC} = 5·5V
Clock inout hysteresis	5		0·4		V	
Clock rate	5			0·5	MHz	
Data set up time, t_2	4	300			ns	See Fig. 4
Data hold time, t_3	4	600			ns	See Fig. 4
Enable set up time, t_1	10	300			ns	See Fig. 4
Enable hold time, t_5	10	600			ns	See Fig. 4
Clock-to-enable time, t_4	10	300			ns	See Fig. 4
Charge pump output current	1		±150		µA	V pin 1 = 2·0V
Charge pump output leakage current	1			±5	nA	V pin 1 = 2·0V
Drift due to leakage				5	mV/s	At collector of external transistor
Charge pump drive output current	18	1			mA	V pin 18 = 0·7V
Charge pump amplifier gain			6400			I pin 18 = 100µA
Oscillator temperature stability				2	ppm/°C	
Oscillator stability with supply voltage				2	ppm/V	
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 1)
Crystal oscillator drive level	2		40		mV p-p	
Crystal oscillator source impedance	2		−400		Ω	Nominal spread = ±15%
Ports and Lock Output						
Sink current	6-9,11	10			mA	V_{OUT} = 0·7V
Port leakage current	6-9			10	µA	V_{OUT} = 13·2V
Varactor drive amplifier disable	10	−350			µA	V_{IN} < 0V
Charge pump disable	4	−350			µA	V_{IN} < 0V

NOTE 1. The maximum resistance quoted refers to all conditions, including start-up.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} = 0V

Parameter	Pin		Value		Units	Conditions
	SP5054	SP5054S	Min.	Max.		
Supply voltage	14	12	−0·3	7	V	
RF input voltage	15,16	13,14		2·5	V p-p	
Port voltage	6-9	6-9	−0·3	14	V	Port in off state
	6-9	6-9	−0·3	6	V	Port in on state
Prescaler DC offset	15,16	13-14	−0·3	V_{CC}+0·3	V	
Loop amplifier DC offset	1,18	1,16	−0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	2	−0·3	V_{CC}+0·3	V	
Data bus inputs	4,5,10	4,5,10	−0·3	V_{CC}+0·3	V	With V_{CC} applied
Storage temperature			−55	+150	°C	
Junction temperature				+150	°C	
DP18 thermal resistance, chip-to-ambient				78	°C/W	
DP18 thermal resistance, chip-to-case				24	°C/W	
MP16 thermal resistance, chip-to-ambient				111	°C/W	
MP16 thermal resistance, chip-to-case				41	°C/W	
Power consumption at 5·5V				484	mW	

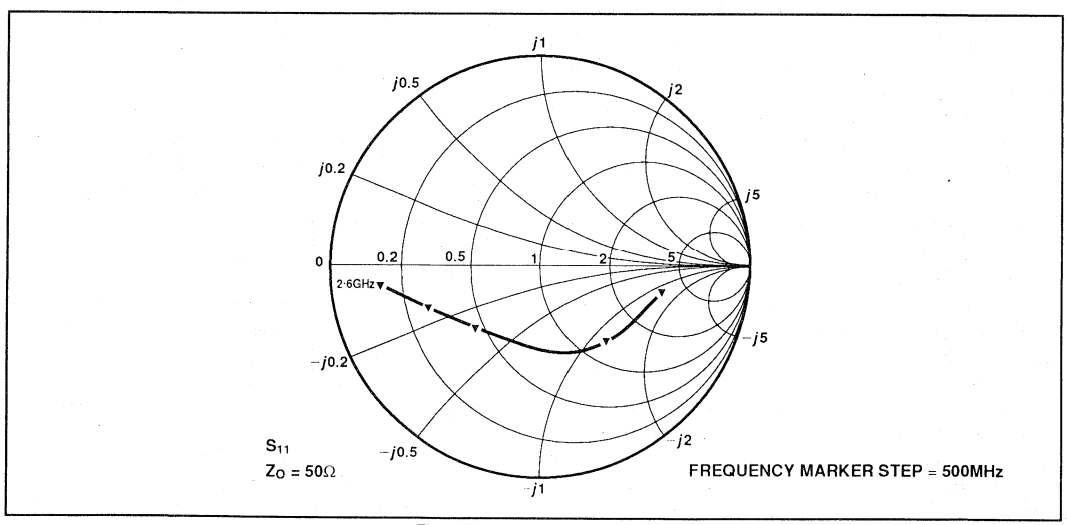


Fig. 2 Typical input impedance

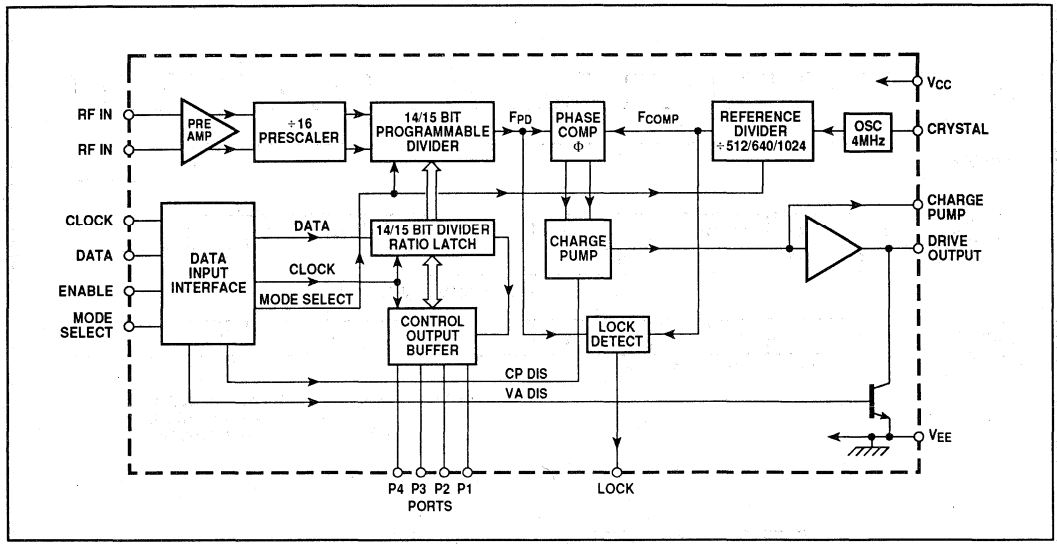


Fig. 3 Block diagram of SP5054

Mode	Mode Select input voltage	Programmable divider bit length	Reference divider ratio	Frequency step size (kHz) *	Maximum operating frequency (GHz) *
3	0·925V_{CC} to V_{CC}	14	512	125	2·0479
2	0·675V_{CC} to 0·825V_{CC}	15	512	125	2·5
1	Open circuit	15	1024	62·5	2·0479
0	0V to 0·325 V_{CC}	15	640	100	2·5

*Table 1 SP5054 modes of operation. * Frequencies stated apply when using a 4MHz crystal.*

FUNCTIONAL DESCRIPTION

The SP5054 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor, to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard Data, Clock and Enable three-wire data bus.

The data load normally consists of a single word, which contains the frequency and port information, and is only transferred to the internal data shift register during an enable high period.

The clock input is disabled during enable low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the Enable, so giving improved fine tune facility for digital AFC etc.

The data sequence and timing follows the format shown in Fig. 4.

The frequency is set by loading the programmable divider with the required 14/15 bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator where it is compared in phase and frequency domain to the internally generated comparison frequency, F_{COMP}.

F_{COMP} is obtained by dividing the output of an on-chip crystal controlled oscillator. The crystal frequency used is generally 4MHz, which gives an F_{COMP} of 3·90625/6·25/7·8125kHz and, when multiplied back up to the synthesised LO, gives a minimum step size of 62·5/100/125kHz, respectively.

The programmable divider is preceded by an input RF preamplifier and high speed, low radiation prescaler. The preamplifier is arranged to be self oscillating, so giving excellent input sensitivity.

The SP5054 contains an improved lock detect circuit which generates a flag when the loop has attained lock. 'In lock' is indicated by high impedance state.

The SP5054 contains 4 general purpose open collector outputs, ports P1-P4, which are capable of sinking at least 10mA. These outputs are set by the remaining four bits within the normal data word.

NOTES ON PIN COMPATIBILITY

The SP5054 may be used in SP5055 applications which require 3-wire bus as opposed to I^2C bus data format. In SP5055 applications where the reference crystal is grounded to pin 3, a small modification is required to ground the crystal as shown in Fig. 5.

Appropriate connections must also be made to the Mode Select input (see Table 1). In Mode 3, The SP5054 is programming compatible with the Toshiba TD6380, in Modes 0 and 2 with the TD6381 and in Mode 1 with the TD6382.

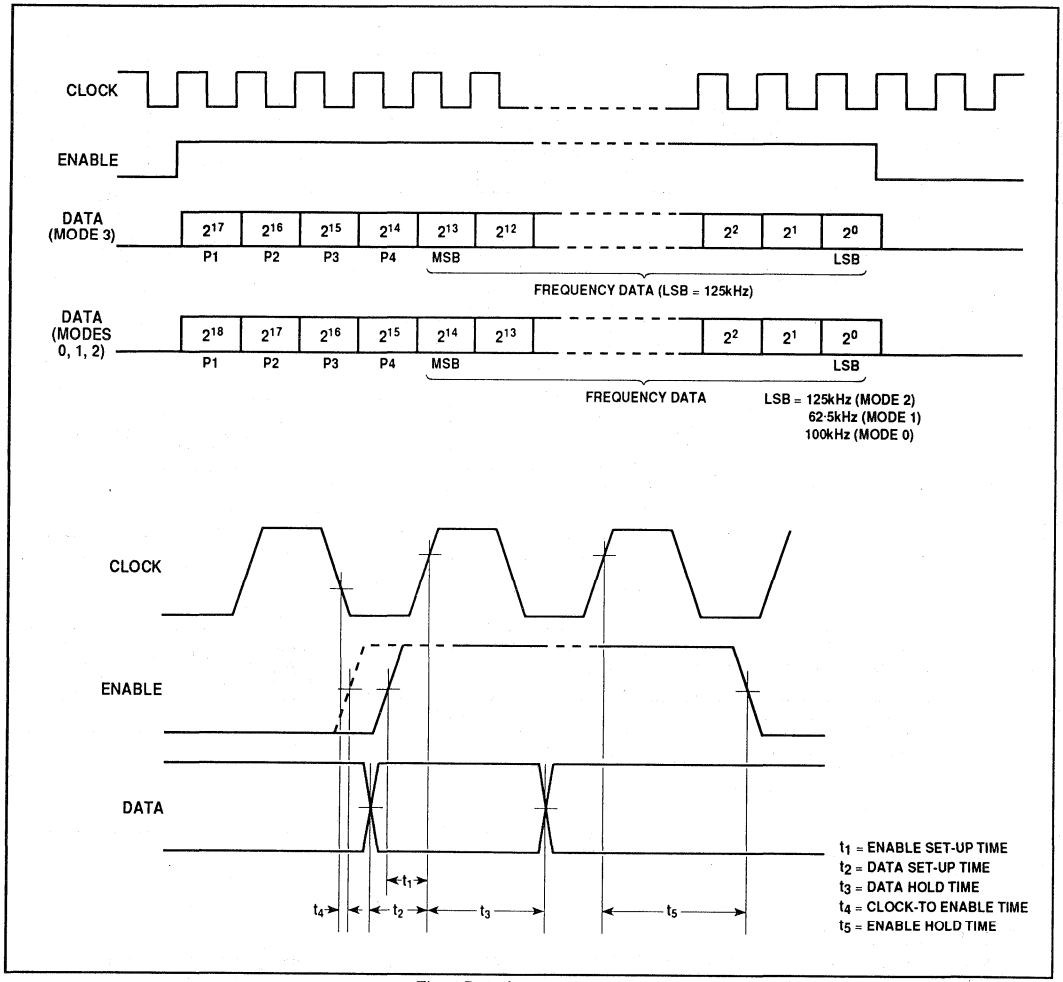


Fig. 4 Data format and timing

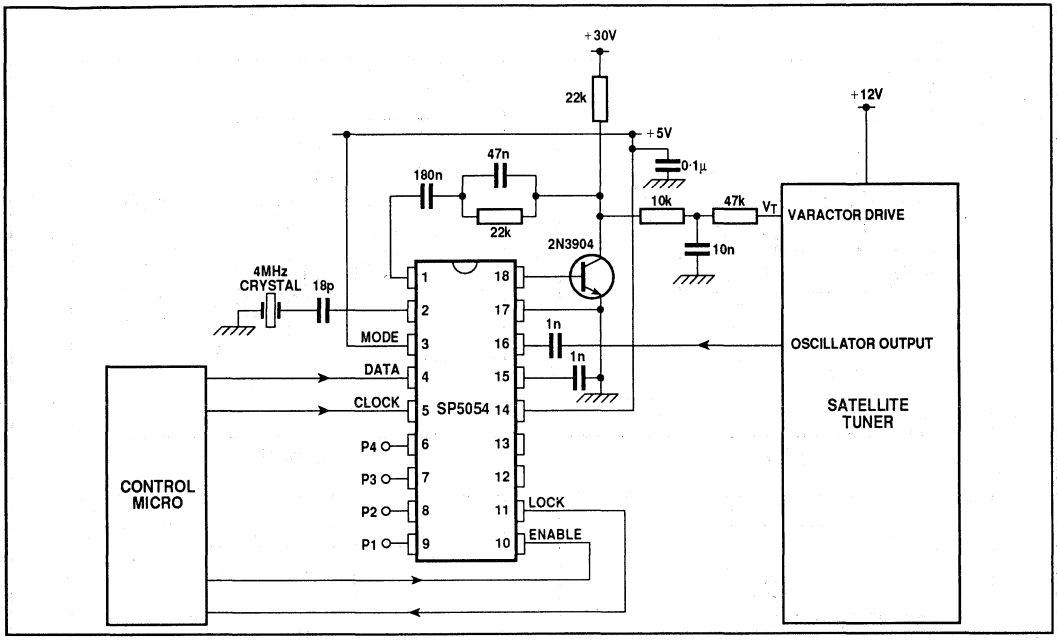


Fig. 5 Typical application (f_{STEP} = 125kHz)

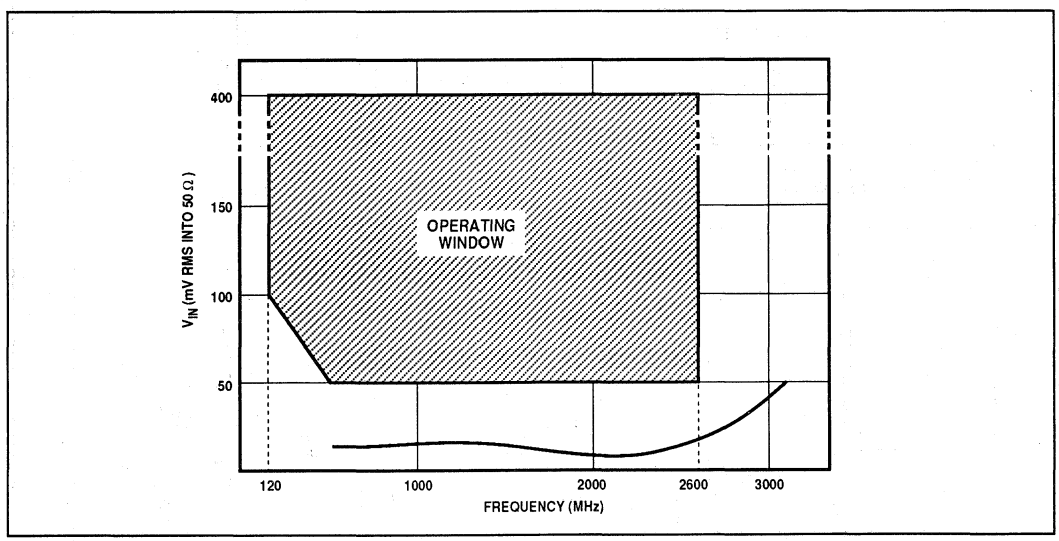


Fig. 6 Typical input sensitivity

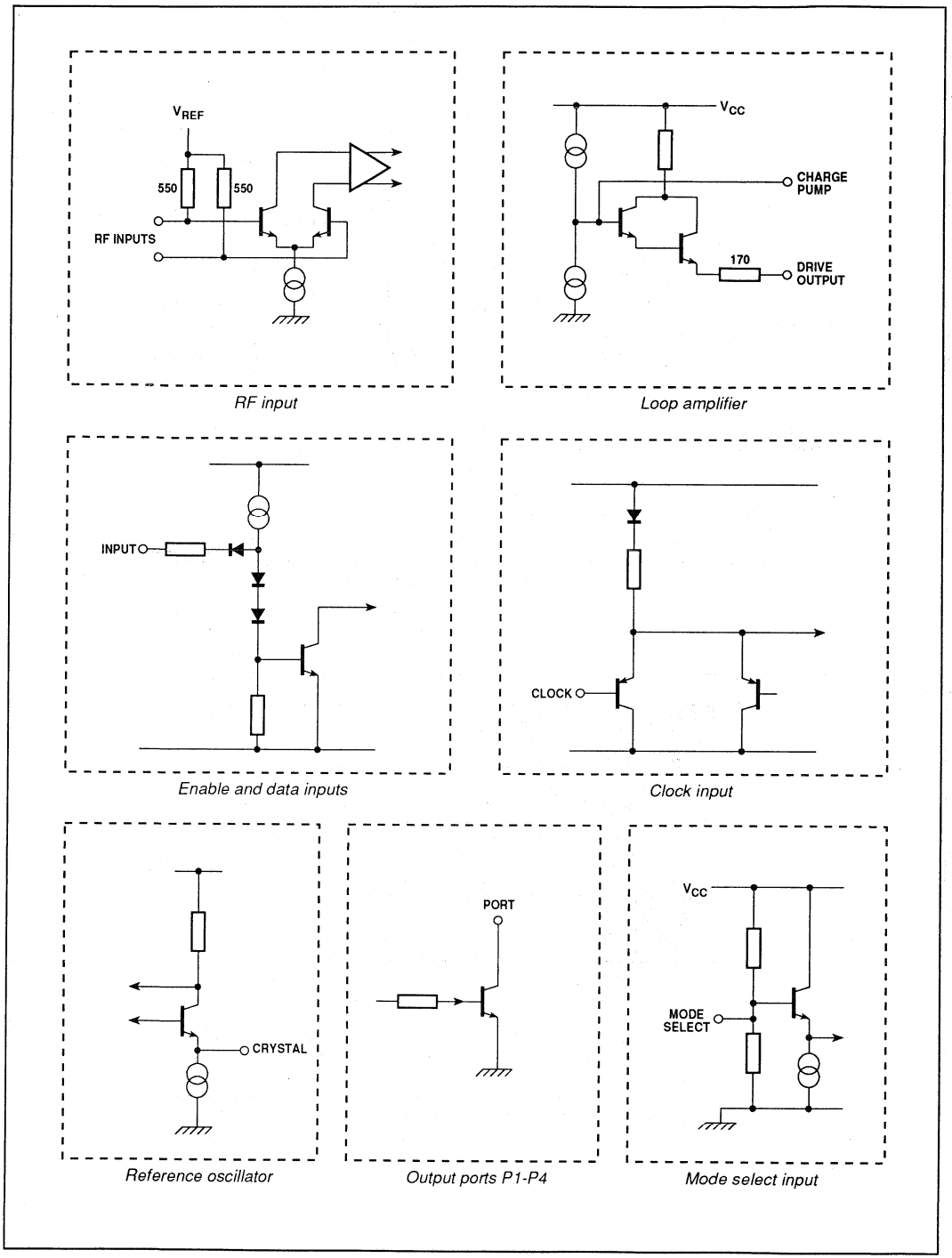


Fig. 7 SP5054 input/output interface circuits

SP5055

2.6 GHz BI-DIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

(Supersedes version in April 1994 Consumer IC Handbook, HB3120 - 2.0)

The SP5055 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 4 addressable current limited outputs and 4 addressable Bi-Directional open collector ports one of which is a 3 bit ADC. The information on these ports can be read via the I²C BUS. The device has one fixed I²C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables 2 or more synthesisers to be used in a system.

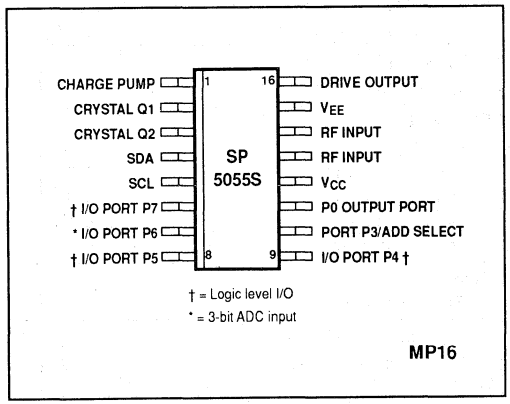


Fig. 1 Pin connections – top view

FEATURES

- Complete 2.6GHz Single Chip System
- Programmable via I²C BUS
- Low power consumption (5V 65mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 6 Controllable Outputs, 4 Bi-Directional
- 5 Level ADC
- Variable I²C BUS Address For Multi Tuner Applications
- Full ESD Protection*

* Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

ORDERING INFORMATION

SP5055S MP - (16 lead Miniature Plastic package)

ELECTRICAL CHARACTERISTICS

T_{amb} = -20°C to +80°C, V_{CC} = +4.7V to 5.3V.
These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated. Reference frequency = 4MHz unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	12		65	80	mA	V_{CC} = 5V
Prescaler input voltage	13, 14	50		300	mV_{RMS}	500MHz to 2.6GHz Sinewave
Prescaler input voltage	13, 14	100		300	mV_{RMS}	120MHz, see Fig. 5
Prescaler input impedance	13, 14		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4, 5	3		5.5	V	
Input low voltage	4, 5	0		1.5	V	
Input high current	4, 5			10	µA	Input voltage = V_{CC}
Input low current	4, 5			-10	µA	Input voltage = 0V
Leakage current	4, 5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0.4	V	I_{sink} = 3mA
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	16	500			µA	$V_{pin\ 16}$ = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	
Crystal oscillator drive level	2		80		mVp-p	
Crystal oscillator negative resistance	2	750			Ω	
Output Ports						
P0, P3 sink current	10, 11	0.7	1	1.5	mA	V_{OUT} = 12V
P0, P3 leakage current	10, 11			10	µA	V_{OUT} = 13·2V
P4-P7 sink current	9-6	10			mA	V_{OUT} = 0.7V
P4-P7 leakage current	9-6			10	µA	V_{OUT} = 13·2V
Input Ports						
P3 input current high	10			+10	µA	$V_{pin\ 10}$ = 13.2V
P3 input current low	10			-10	µA	$V_{pin\ 10}$ = 0V
P4,P5,P7 input voltage low	9,8,6			0.8	V	
P4,P5,P7 input voltage high	9,8,6	2.7			V	
P6 input current high	7			+10	µA	See Table 3 for ADC Levels
P6 input current low	7			-10	µA	

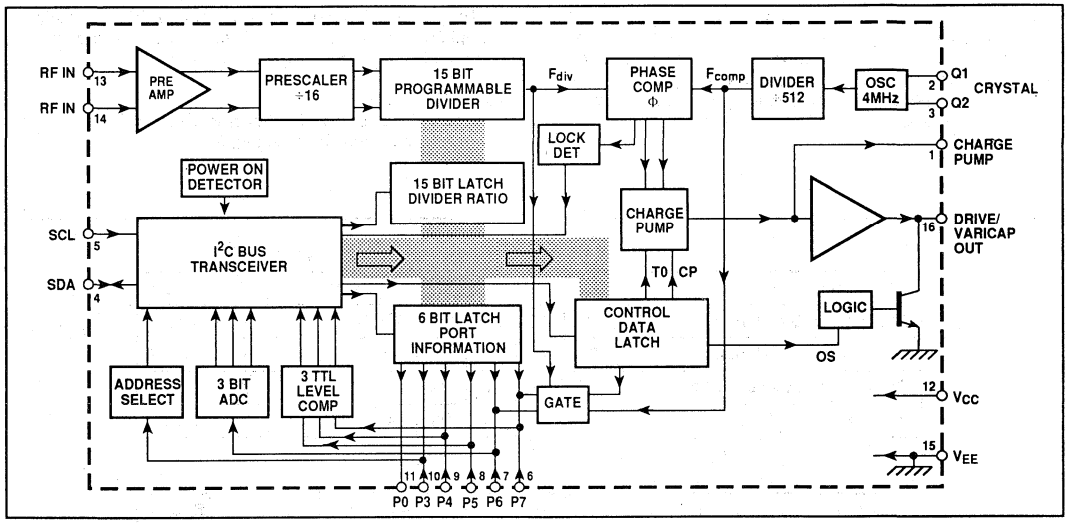


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The SP5055 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C BUS format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C Bus system. Table 4 shows how the address is selected by applying a voltage to P3. The last bit of the address byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5055 receives a correct address byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are programmed. When the SP5055 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2 + 3 select the synthesised frequency while bytes 4 + 5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that byte is interpreted as byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (i.e., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-16 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Fig 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 16 times the comparison frequency F_{comp}.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-board 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7·8125kHz when a 4MHz reference is used.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170μA and a logic 0 for ±50μA, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{comp} to P6 and F_{div} to P7.

Byte 5 programs the output ports P0 to P7; on a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power-on reset indicator and is set to a logic 1 if the power supply to the device has dropped below 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2,I1,I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5 level ADC.

The 5 level ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical Application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	P6	P5	P4	P3	X	X	P0	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	**Byte 2**

Table 2 Read data format (MSB is transmitted first)

A	:	Acknowledge bit
MA1, MA0	:	Variable address bits (see Table 4)
CP	:	Charge Pump current select
T1	:	Test mode selection
T0	:	Charge pump disable
OS	:	Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P0	:	Control output states
POR	:	Power On Reset indicator
FL	:	Phase lock detect flag
I2, I1, I0	:	Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0	:	5 Level ADC data from P6 (see Table 3)
X	:	Don't care

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0{\cdot}45V_{CC}$ to $0{\cdot}6V_{CC}$
0	1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}45V_{CC}$
0	0	1	$0{\cdot}15V_{CC}$ to $0{\cdot}3V_{CC}$
0	0	0	0 to $0.15V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	0V to $0{\cdot}2V_{CC}$
0	1	Always valid
1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}7V_{CC}$
1	1	$0{\cdot}8V_{CC}$ -13.2V

Table 4 Address selection

Fig. 3 Data formats

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

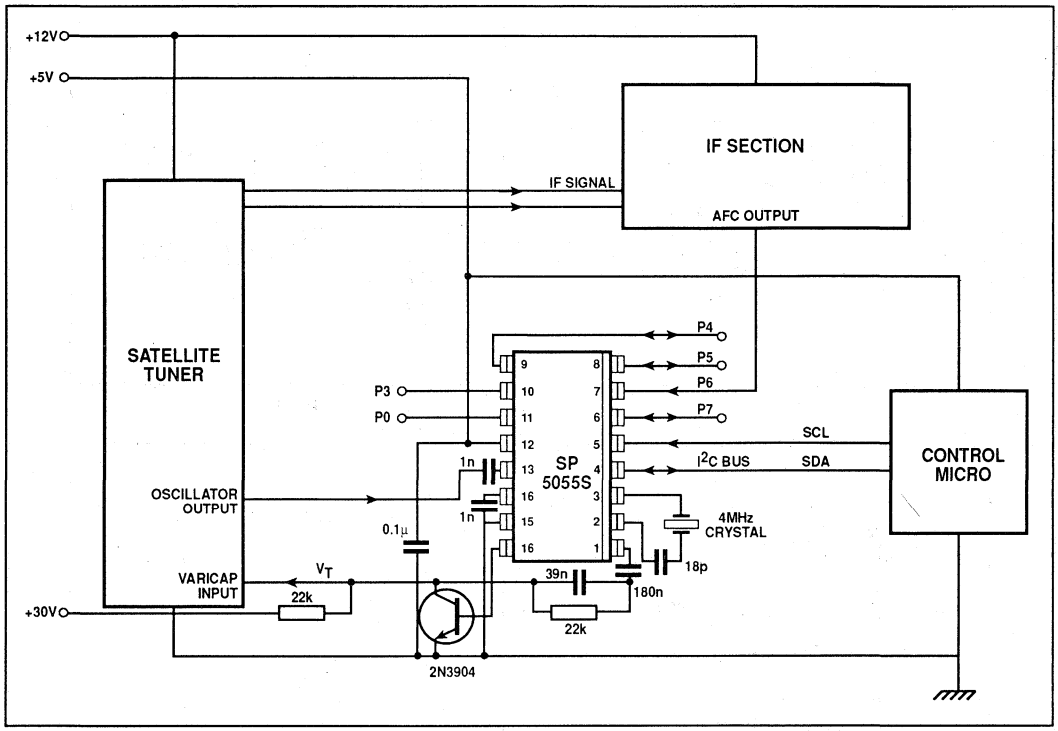


Fig. 4 Typical application

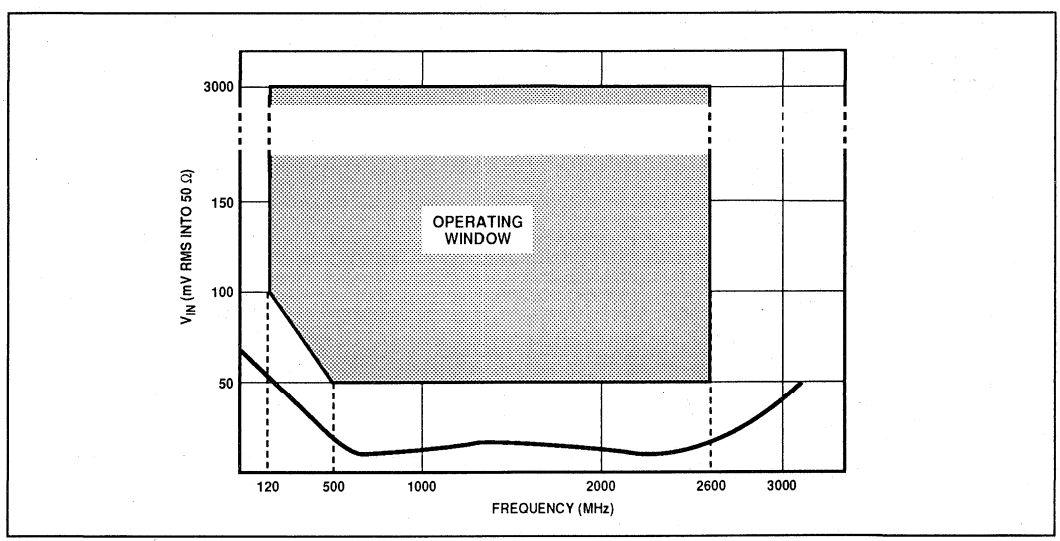


Fig. 5 Typical input sensitivity

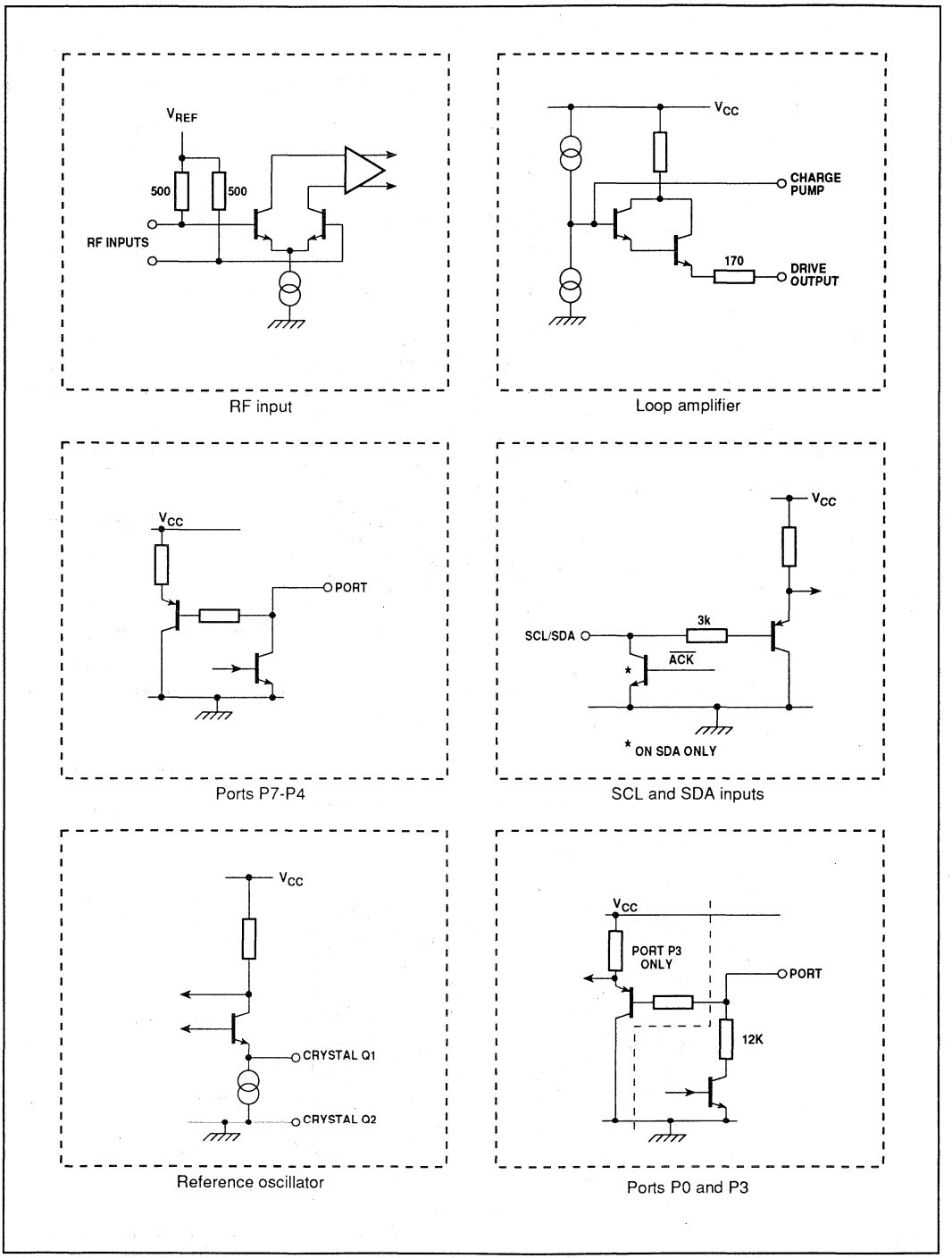


Fig. 6 SP5055 Input/output interface circuits

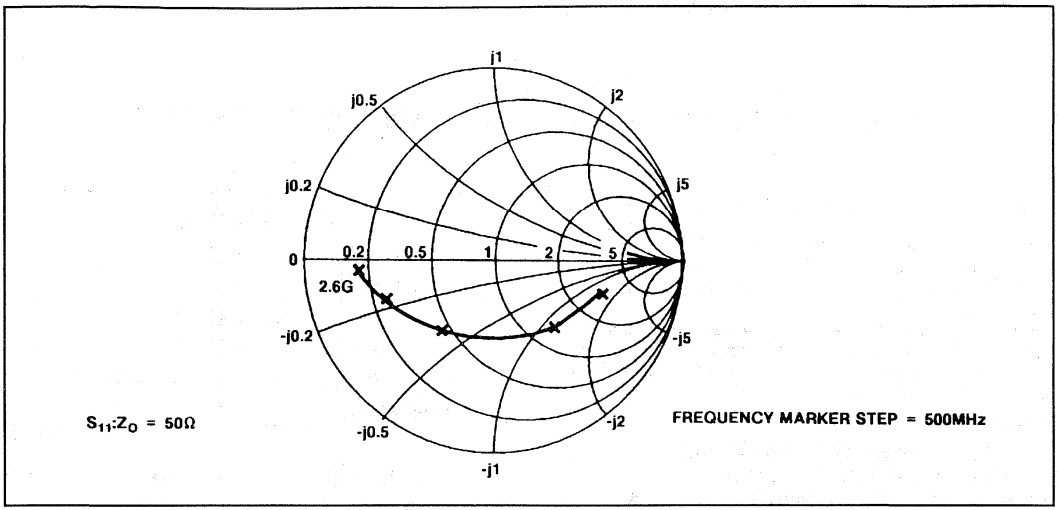


Fig. 7 Typical input impedance

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V

Parameter	Pin	Value		Units	Conditions
		Min.	Max.		
Supply voltage	12	-0.3	7	V	
RF input voltage	13, 14		2.5	Vp-p	
Port voltage	6-11	-0.3	14	V	Port in off state
	6-9	-0.3	6	V	Port in on state
	10, 11	-0.3	14	V	Port in on state
Total port output current	6-11		50	mA	
RF input DC offset	13, 14	-0.3	V_{CC}+0.3	V	
Charge pump DC offset	1	-0.3	V_{CC}+0.3	V	
Drive DC offset	16	-0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	-0.3	V_{CC}+0.3	V	
SDA, SCL input voltage	4, 5	-0.3	V_{CC}+0.3	V	With V_{CC} applied
		-0.3	5.5	V	V_{CC} not applied
Storage temperature		-55	+125	°C	
Junction temperature			+150	°C	
MP 16 Thermal resistance, chip-to-ambient			111	°C/W	
MP 16 Thermal resistance, chip-to-case			41	°C/W	
Power consumption at 5.5V			440	mW	All ports off

DS3966-2.2

SP5070

2.4GHz FIXED MODULUS FREQUENCY SYNTHESISER

The SP5070 is a single modulus frequency synthesiser for use in Satellite TV receivers and together with an appropriate voltage controlled oscillator (VCO), forms a complete phase locked loop (PLL) synthesiser. The circuit consists of a prescaler with preamplifier and a fixed modulus divider. The phase comparator is fed with a reference frequency derived from an external oscillator or crystal. The comparator has a charge pump output amplifier stage around which feedback may be applied. Only an external transistor is required for varicap line driving.

FEATURES

- Low Power Consumption (5V, 47mA typ.)
- Prescaler and Preamplifier Included
- Charge Pump Amplifier with Feedback Point
- Charge Pump Disable Facility
- Synthesises Frequencies up to 2.4GHz
- Pin and Function Compatible with SP5060 and SP5062
- Full ESD Protection*

  * Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems
- C-Band with Frequency Doubling Mixer

ORDERING INFORMATION

SP5070 DP - (14 Lead Plastic Package)
SP5070F MP - (14 Lead Miniature Plastic Package)

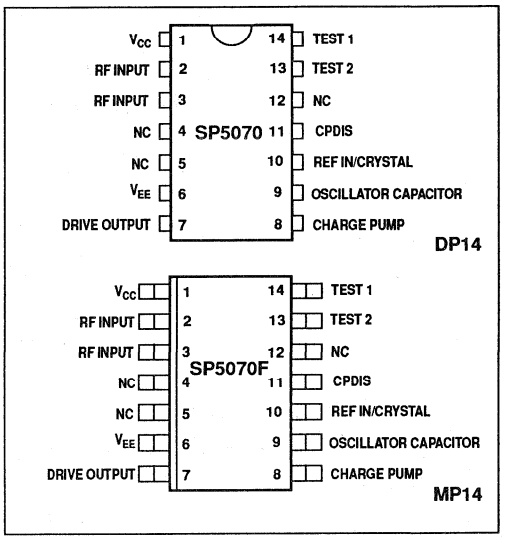


Fig.1 Pin connections - top view

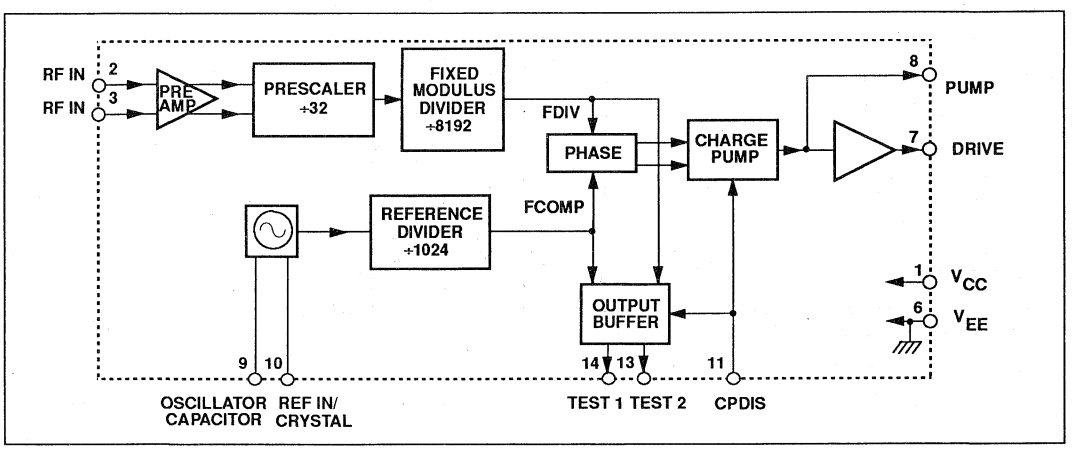


Fig.2 Block diagram of SP5070

ELECTRICAL CHARACTERISTICS

Tamb = -40°C to +85°C, VCC = +4.5V to +5.5V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	1	-	47	55	mA	V_{CC} = 5V
Prescaler input voltage Prescaler input voltage		2,3 2,3	50 100	-	300 300	mV_{RMS} mV_{RMS}	300MHz to 1.8GHz sinewave 2.4GHz, see Fig.5
Prescaler input impedance Input capacitance		2,3 2,3	- -	50 2	- -	Ω pF	
Charge pump output current Charge pump output leakage Drift due to leakage		8 8 -	- - -	±100 - -	- ±5 5	µA nA mV/s	V pin 8 = 2.0V V pin 8 = 2.0V At collector of External Varicap Drive transistor
Charge pump drive output current		7	1	-	-	mA	V pin 7 = 0.7V
Charge pump amplifier gain		-	-	6400	-	-	pin 7 current 100µa
Oscillator temperature stability Oscillator stability with supply voltage		9,10 9,10	- -	- -	2 2	ppm/°C ppm/V	
Reference clock frequency External reference amplitude		10 10	2 150	-	10 500	MHz mV_{RMS}	
Charge pump disable/TEST 1 and TEST 2/enable		11	-250	-	-500	µA	V_{IN}<0V
Charge pump disable leakage		11	-	-	10	µA	V pin 11= V_{CC}
TEST 1/TEST 2 sink current		13,14	1	-	-	mA	VOUT = 0.7V
TEST 1/TEST 2 leakage current		13,14	-	-	10	µA	VOUT = V_{CC}+0.3V
TEST 1/TEST 2 voltage		13,14	-	-	V_{CC}+0.3	V	

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} = 0V

Characteristics	Pin	Value		Units
		Min	Max	
Supply voltage	1	-0.3	7	V
RF input voltage	2,3	-	2.5	Vp-p
RF input DC offset	2,3	-0.3	V_{CC}+0.3	V
Charge pump DC offset	8	-0.3	V_{CC}+0.3	V
Charge pump disable	11	-0.7	V_{CC}+0.3	V
Drive DC offset	7	-0.3	V_{CC}+0.3	V
Crystal oscillator DC offset	9,10	-0.3	V_{CC}+0.3	V
TEST outputs	13,14	-0.3	V_{CC}+0.3	V
Storage temperature	-	-55	150	°C
Junction temperature	-	-	+150	°C
DP14 thermal resistance, chip-to-ambient	-	-	78	°C/W
DP14 thermal resistance, chip-to-case	-	-	30	°C/W
MP14 thermal resistance, chip-to-ambient	-	-	123	°C/W
MP14 thermal resistance, chip-to-case	-	-	45	°C/W
Power consumption at 5.5V	-	-	275	mW

FUNCTIONAL DESCRIPTION

The SP5070, when used with a voltage controlled oscillator, forms a complete phase locked loop frequency synthesiser.

The phase comparator comparison frequency is obtained by dividing the reference frequency. This may be generated on-chip by means of an external crystal, or from an external reference oscillator.

The output of the prescaler is divided by the fixed modulus divider, producing an output frequency which is phased locked to the comparison frequency.

The divider stages are arranged to give a fixed ratio between the synthesised frequency and the reference of 256:1. Any frequency within the range of 300MHz to 2.4GHz may be achieved by using the appropriate reference or crystal frequency.

A single external transistor, driven from the charge pump output, provides the output drive necessary for the oscillator varicap line.

A test facility which disables the charge pump is also provided. This is activated when a negative voltage is applied to pin 11, see electrical characteristics above. When the device is in this mode, F_{COMP} and F_{DIV} are also available at outputs TEST1 and TEST2 respectively. These are open collector outputs and are each capable of sinking a minimum of 1mA. In normal mode of operation these outputs are high impedance.

For compatibility with SP5060/SP5062, pin 11 may be connected to V_{CC}

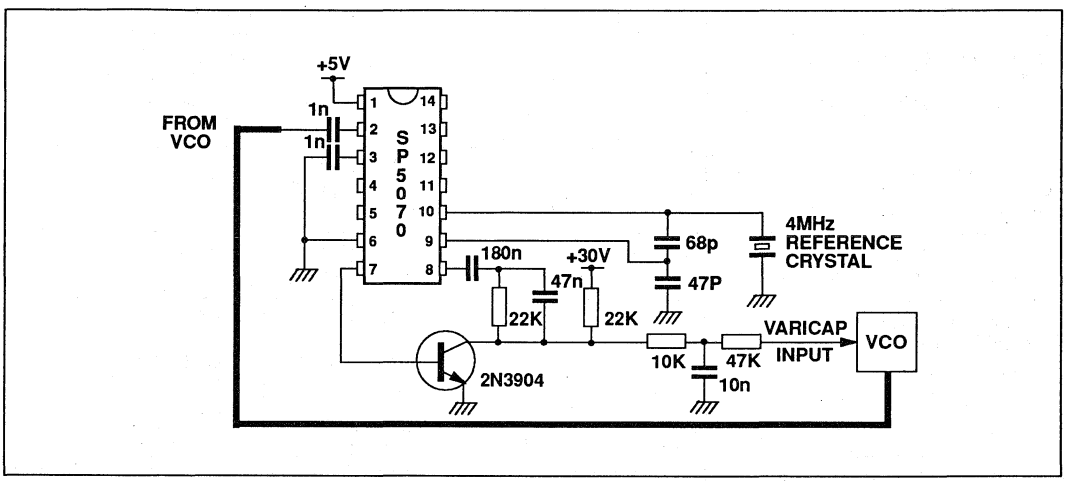


Fig.3 Typical application and test circuit (1024MHz with 4MHz reference crystal)

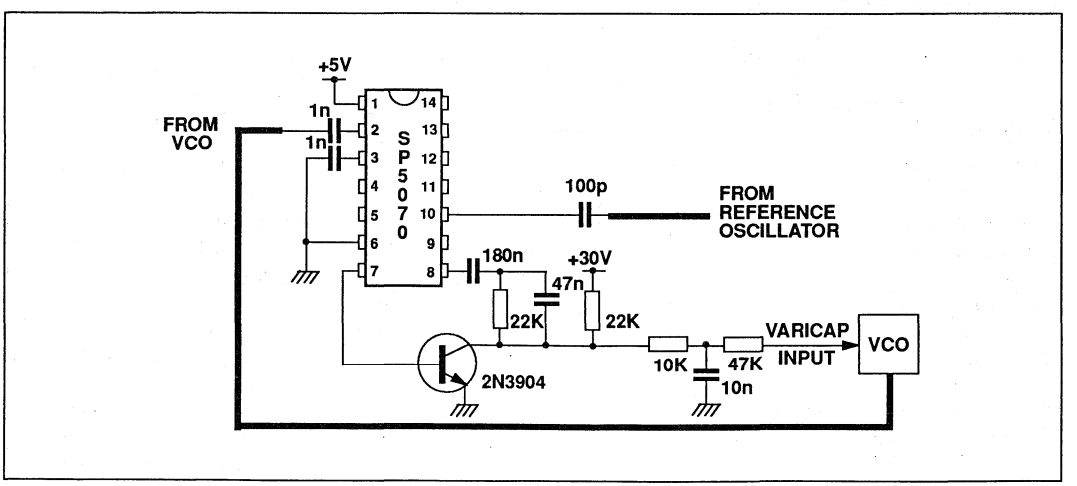


Fig.4 Application using external reference oscillator

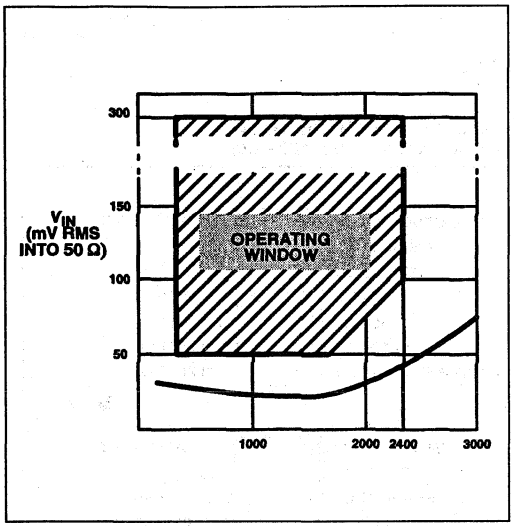


Fig.5 Typical input sensitivity

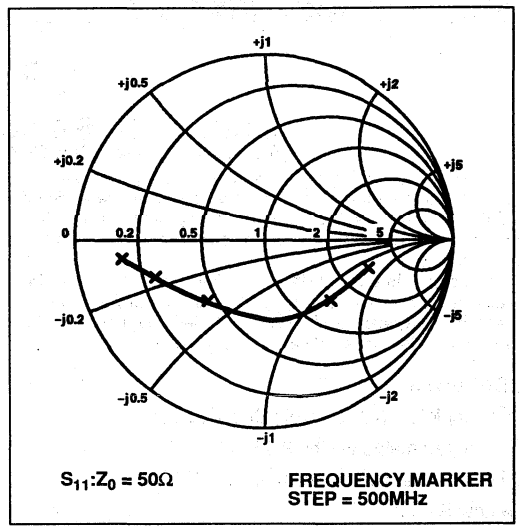


Fig.6 Typical input impedance

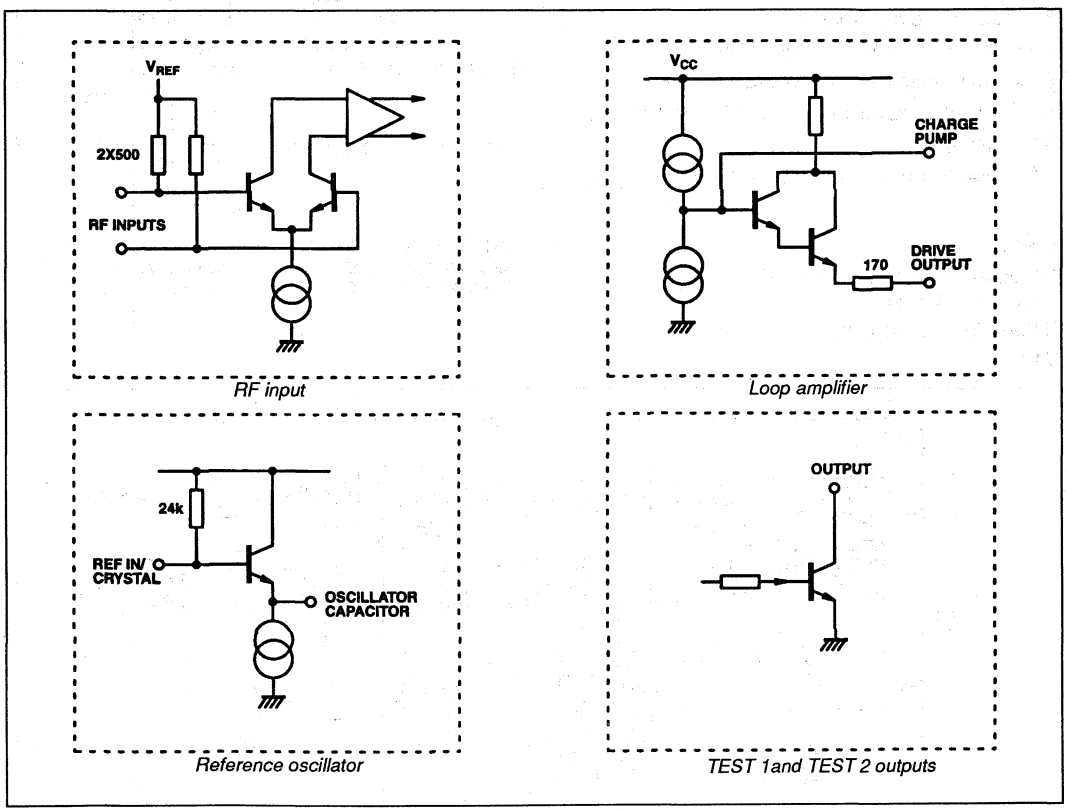


Fig.7 SP5070 input/output interface circuits

SP5502

1.3 GHz I²C BUS 4-ADDRESS SYNTHESISER

(Supersedes version in April 1994 Consumer IC Handbook, HB3120 - 2.0)

The SP5502 is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The SP5502 has four programmable I²C BUS addresses, which allows two or more synthesisers to be used in a system.

The device is available in two variants: the SP5502F in 14-lead miniature plastic package (MP14) and the SP5502S in 16-lead miniature plastic package (MP16). See Features below for functional differences between the devices.

FEATURES

- Complete 1·3GHz Single Chip System
- Programmable via the I²C BUS
- Low Power Consumption (240mW Typ.)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 5×20mA Controllable Outputs (SP5502S)
- 3×20mA Controllable Outputs (SP5502F)
- Variable I²C BUS Address for Multi-Tuner Applications
- ESD Protection *

* Normal ESD handling precautions should be observed.

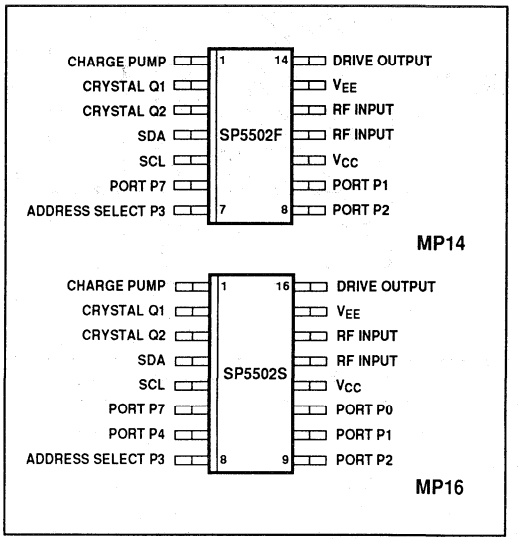


Fig. 1 Pin connections – top view

APPLICATIONS

- Satellite TV when Combined with SP4902 2·5GHz Prescaler
- Cable Tuning Systems
- VCRs

ORDERING INFORMATION

SP5502F KG MPAS (14-lead miniature plastic package)
SP5502S KG MPAS (16-lead miniature plastic package)

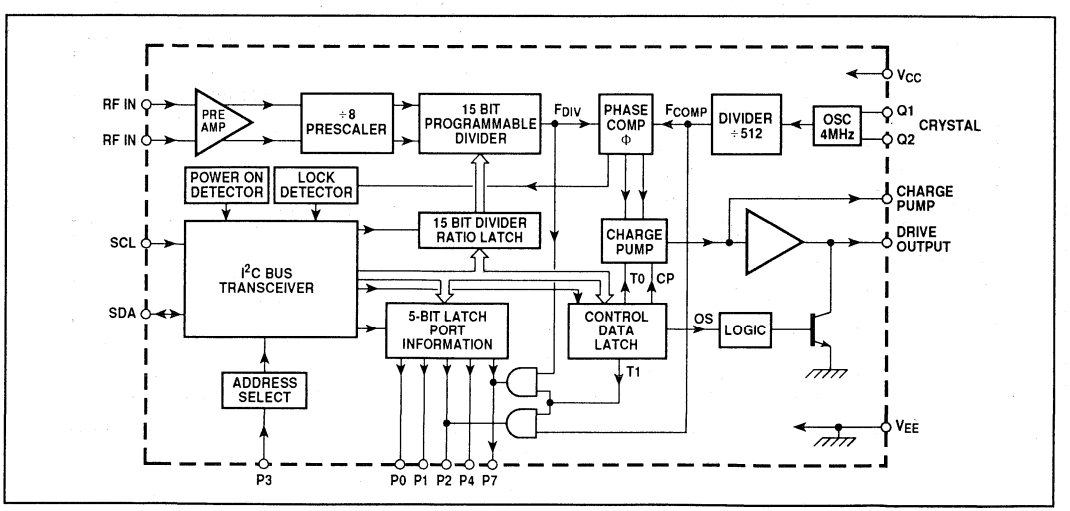


Fig. 2 Block diagram of SP5502S. (Ports P0 and P4 not present on SP5502F)

ELECTRICAL CHARACTERISTICS

T_{AMB} = −10°C to +80°C, V_{CC} = +4·5V to +5·5V. All pin references are to the SP5502S (MP16 package).
These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated. Reference frequency 4MHz unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	12		48	60	mA	V_{CC} = 5V
Prescaler input voltage	13,14	12·5		300	mVrms	80MHz to 1GHz
Prescaler input voltage		30		300	mVrms	1·3GHz, see Fig. 5
Prescaler input impedance	13,14		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4,5	3		V_{CC}	V	
Input low voltage	4,5	0		1·5	V	
Input high current	4,5			10	µA	Input voltage = V_{CC}
Input low current	4,5			−10	µA	Input voltage = 0V
Leakage current	4,5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0·4	V	Sink current = 3mA
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	16	500				V pin 16 = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 2)
Crystal oscillator drive level			40		mV p-p	
Crystal oscillator negative resistance	2	750			Ω	
Output Ports						
Sink current	6,7,9-11	20			mA	V_{OUT} = 0·7V (see note 1)
Leakage current	6,7,9-11			10	µA	V_{OUT} = 13·2V
Input Port						
P3 input current high	8			1	mA	V pin 8 = V_{CC}
P3 input current low	8			−0·5	mA	V pin 8 = 0V

NOTES
1. Source impedance between all output ports and ground is approximately 5Ω. This should be taken into account when calculating output port saturation voltages.
2. The maximum resistance quoted refers to all conditions, including start-up.

FUNCTIONAL DESCRIPTION (Except where otherwise indicated, 'SP5502' refers to both variants)

The SP5502 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C Bus system. Table 3 shows how the address is selected by applying a voltage to P3. The address input is shown in Fig. 6. The LSB of the address Byte (R/$\overline{W}$) sets the device into read mode if it is high and write mode if it is low. When the SP5502 receives a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed. When the SP5502 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status Byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that Byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data Bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (i.e., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Fig 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP}.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-chip 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7·8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170µA and a logic 0 for ±50µA, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P2 and P7, a logic 1 connects F_{COMP} to P2 and F_{DIV} to P7.

Byte 5 programs the output ports P0-P2, P4 and P7 on the SP5502S (P1, P2 and P7 only on SP5502F), a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2. Bit 1 (POR) is the power supply to the device has dropped below a nominal 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	X	X	P4*	X	P2	P1	P0*	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	N	N	N	N	N	N	A	**Byte 2**

Table 2 Read data format

MA1	MA0	Voltage input to P3
0	0	0V to 0·1V_{CC}
0	1	Open circuit
1	0	0·4V_{CC} to 0·6V_{CC}†
1	1	0·9V_{CC} to V_{CC}

Table 3 Address selection

A	:	Acknowledge bit
MA1, MA0	:	Variable address bits (see Table 3)
CP	:	Charge Pump current select
T1	:	Test mode selection
T0	:	Charge pump disable
OS	:	Varactor drive Output disable Switch
P7, P4*, P2, P1, P0*	:	Control output port states
POR	:	Power On Reset indicator
FL	:	Phase lock detect flag
X	:	Don't care
N	:	Not valid

NOTES

† Programmed by connecting a 15kΩ resistor between Address Select Port P3 and V_{CC}.

* Don't care condition on SP5502F.

Fig. 3 Data formats

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

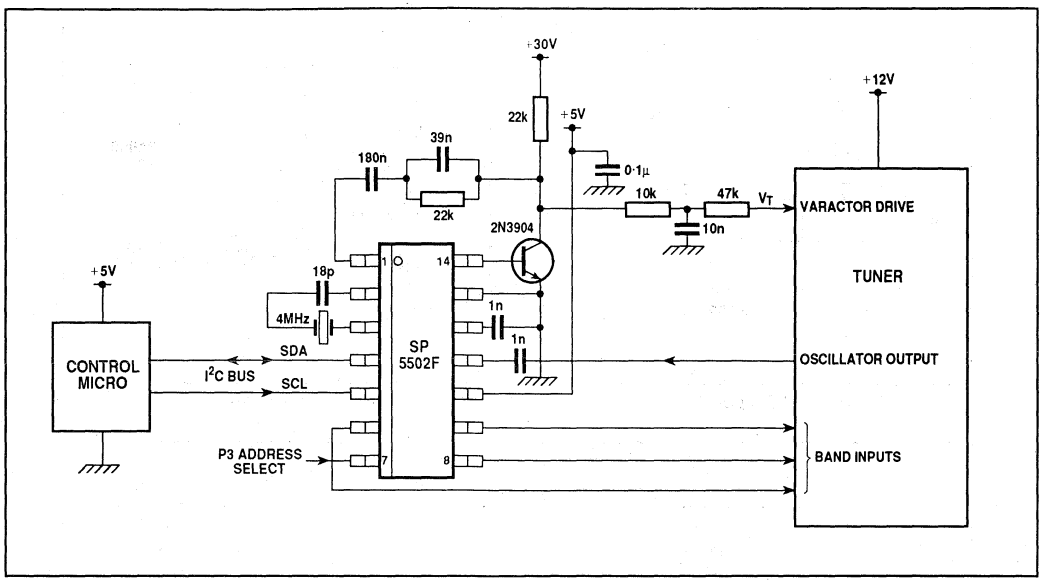


Fig. 4 Typical application

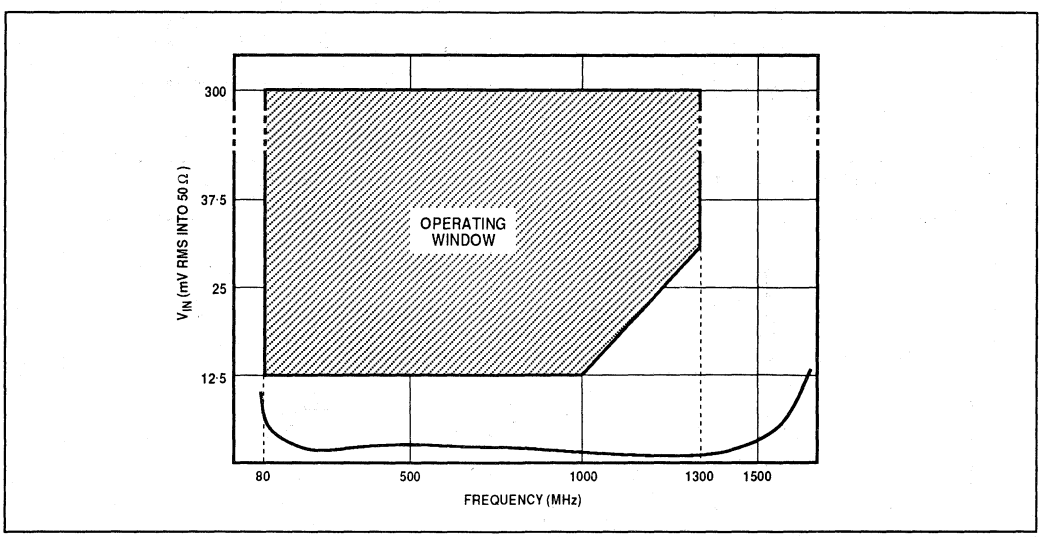
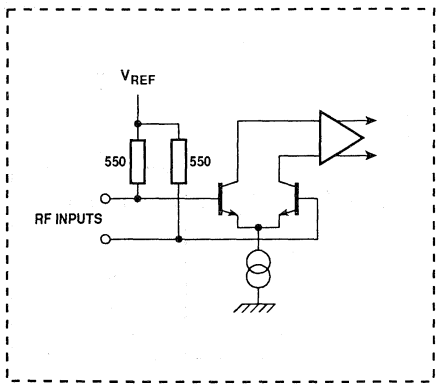
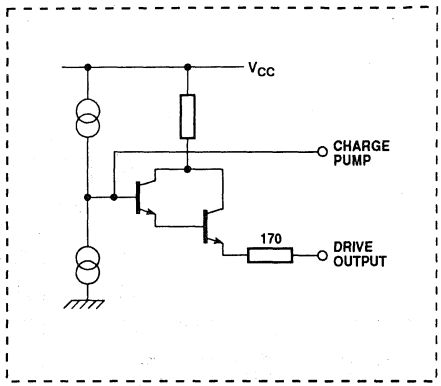


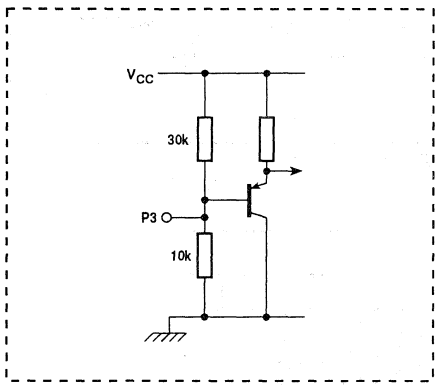
Fig. 5 Typical input sensitivity



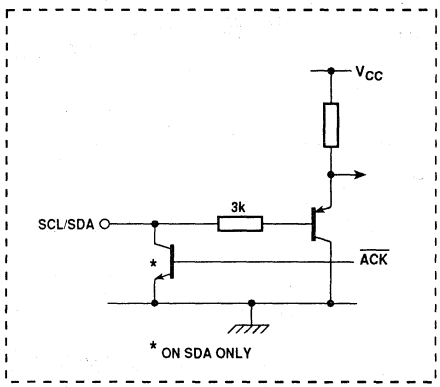
RF input



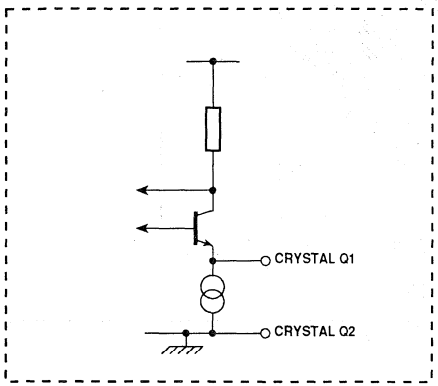
Loop amplifier



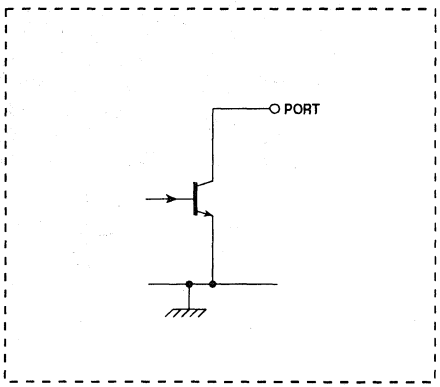
Address programming input



SCL and SDA inputs



Reference oscillator



Ports P0-P2, P4 and P7 (SP5502S).
Ports P1, P2, and P7 (SP5502F)

Fig. 6 SP5502 input/output interface circuits

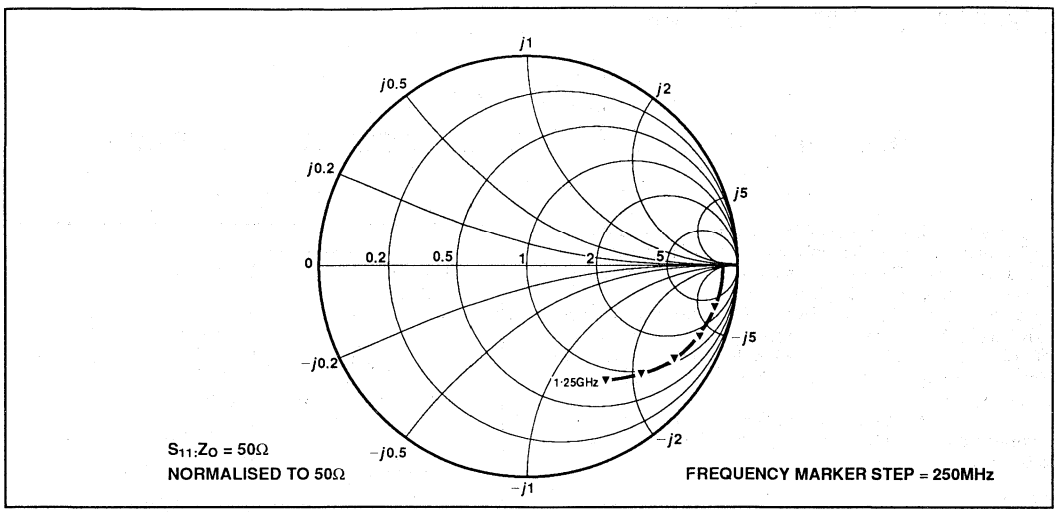


Fig. 7 Typical input impedance

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} = 0V

Parameter	Pin		Value		Units	Conditions
	SP5502S	SP5502F	Min.	Max.		
Supply voltage	12	10	−0·3	7	V	
RF input voltage	13,14	11,12		2·5	V p-p	
Port voltage	6,7, 9-11	6,8, 9	−0·3	14	V	Port in off state
	6,7, 9-11	6,8, 9	−0·3	6	V	Port in on state
	8	7	−0·3	V_{CC}+0·3	V	
Total port output current	6,7, 9-11	6,8, 9		50	mA	
RF input DC offset	13,14	11,12	−0·3	V_{CC}+0·3	V	
Charge pump DC offset	1	1	−0·3	V_{CC}+0·3	V	
Drive output DC offset	16	14	−0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	2	−0·3	V_{CC}+0·3	V	
SDA, SCL input voltage	4,5	4,5	−0·3	V_{CC}+0·3	V	With V_{CC} applied
			−0·3	5·5	V	V_{CC} not applied
Storage temperature			−55	+150	°C	
Junction temperature				+150	°C	
MP16 thermal resistance, chip-to-ambient				111	°C/W	
MP16 thermal resistance, chip-to-case				41	°C/W	
MP14 thermal resistance, chip-to-ambient				123	°C/W	
MP14 thermal resistance, chip-to-case				45	°C/W	
Power consumption at 5·5V				363	mW	

2184-3.3

SP5510

1·3 GHz BIDIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

(Supersedes version in April 1994 Consumer IC Handbook, HB3120 - 2.0)

The SP5510 is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device has four addressable current-limited output ports (P0-P3) and four bi-directional open-collector ports (P4-P7), one of which (P6) is also a 3-bit 5-level ADC input. The information on these ports can be read via the I²C BUS. The SP5510S is a variant in a 16-lead miniature plastic package, without P0-P2 but functionally identical in other respects.

Both variants have one fixed I²C BUS address and three programmable addresses, allowing two or more synthesisers to be used in a system.

FEATURES

- Complete 1·3GHz Single Chip System
- Programmable via the I²C BUS
- Low Power Consumption (215mW Typ.)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 8 Controllable Outputs, 4 Bi-directional(SP5510)
- 5 Controllable Outputs, 4 Bi-directional (SP5510S)
- 5-Level ADC
- Variable I²C BUS Address for Picture in Picture TV
- ESD Protection *

* Normal ESD handling precautions should be observed.

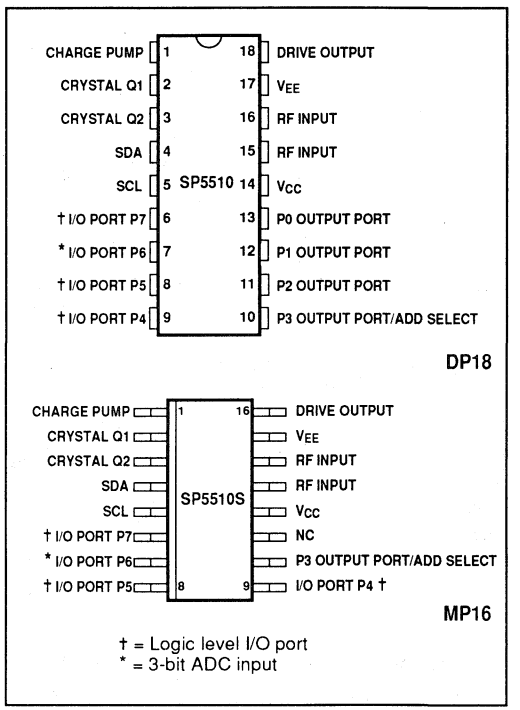


Fig. 1 Pin connections – top view

APPLICATIONS

- Satellite TV when Combined with SP4902 2·5GHz Prescaler
- Cable Tuning Systems
- VCRs

ORDERING INFORMATION

SP5510 NA DP (18-lead plastic package)
SP5510S NA MP (16-lead miniature plastic package)

ELECTRICAL CHARACTERISTICS

T_{AMB} = −10°C to +80°C, V_{CC} = +4·5V to +5·5V. All pin references are to the SP5510 (DP18 package).
These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated. Reference frequency 4MHz unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	14		43	53	mA	V_{CC} = 5V
Prescaler input voltage	15,16	12·5		300	mVrms	50MHz to 1GHz
Prescaler input voltage		30		300	mVrms	1·3GHz, see Fig. 5
Prescaler input impedance	15,16		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4,5	3		5·5	V	
Input low voltage	4,5	0		1·5	V	
Input high current	4,5			10	µA	Input voltage = V_{CC}
Input low current	4,5			−10	µA	Input voltage = 0V
Leakage current	4,5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0·4	V	Sink current = 3mA
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	18	500				V pin 18 = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 2)
Crystal oscillator drive level			40		mV p-p	
Crystal oscillator negative resistance	2	750			Ω	
Output Ports						
P0-P3 sink current (see note 1)	10-13	0·7	1	1·5	mA	V_{OUT} = 12V
P0-P3 leakage current (see note 1)	10-13			10	µA	V_{OUT} = 13·2V
P4-P7 sink current	6-9	10			mA	V_{OUT} = 0·7V
P4-P7 leakage current	6-9			10	µA	V_{OUT} = 13·2V
Input Ports						
P3 input current high	10			+10	µA	V pin 10 = 13·2V
P3 input current low	10			−10	µA	V pin 10 = 0V
P4, P5, P7 input voltage low	6,8,9			0·8	V	
P4, P5, P7 input voltage high	6,8,9	2·7			V	
P6 input current high	7			+10	µA	See Table 3 for ADC levels
P6 input current low	7			−10	µA	

NOTES
1. Ports P0-P2 not present on the SP5510S.
2. The maximum resistance quoted refers to all conditions, including start-up.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V. Pin references are for SP5510 (DP18 package)

Parameter	Pin	Value		Units	Conditions
		Min.	Max.		
Supply voltage	14	−0·3	7	V	
RF input voltage	15,16		2·5	V p-p	
Port voltage	6-13	−0·3	14	V	Port in off state
	6-9	−0·3	6	V	Port in on state
	10-13	−0·3	14	V	Port in on state
Total port output current	6-13		50	mA	
RF input DC offset	15-16	−0·3	V_{CC}+0·3	V	
Charge pump DC offset	1	−0·3	V_{CC}+0·3	V	
Drive output DC offset	18	−0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	−0·3	V_{CC}+0·3	V	
SDA, SCL input voltage	4,5	−0·3	V_{CC}+0·3	V	With V_{CC} applied
		−0·3	5·5	V	V_{CC} not applied
Storage temperature		−55	+150	°C	
Junction temperature			+150	°C	
DP18 thermal resistance, chip-to-ambient			78	°C/W	
DP18 thermal resistance, chip-to-case			24	°C/W	
MP16 thermal resistance, chip-to-ambient			111	°C/W	
MP16 thermal resistance, chip-to-case			41	°C/W	
Power consumption at 5·5V			321	mW	

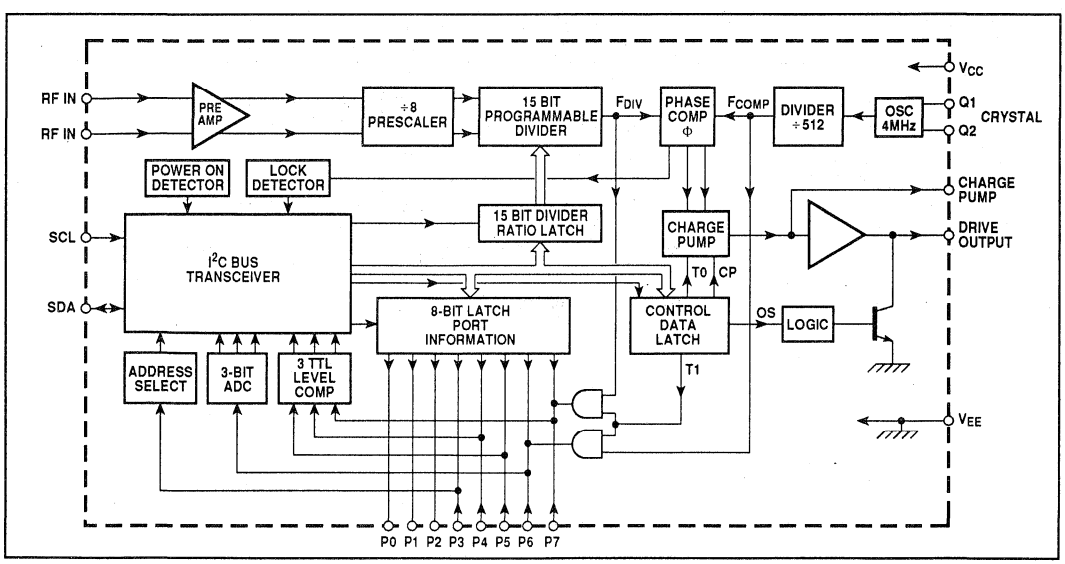


Fig. 2 Block diagram. (Ports P0-P2 not present on SP5510S)

FUNCTIONAL DESCRIPTION

The SP5510 is programmed from an I^2C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I^2C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I^2C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The LSB of the address Byte (R/$\overline{W}$) sets the device into read mode if it is high and write mode if it is low. When the SP5510 receives a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed. When the SP5510 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status Byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that Byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data Bytes can be entered without the need to re-address the device until an I^2C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (i.e., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Figs. 7 and 8.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP}.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-chip 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7·8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for $\pm 170\mu A$ and a logic 0 for $\pm 50\mu A$, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{COMP} to P6 and F_{DIV} to P7.

Byte 5 programs the output ports P0-P7, a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below a nominal 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic1). These inputs will then respond to data complying with standard TTL voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5-level ADC.

The 5-level ADC can be used to feed AFC information to the microprocessor from the IF section of the television, as illustrated in Fig. 4.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	P6	P5	P4	P3	P2*	P1*	P0*	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	**Byte 2**

Table 2 Read data format

A2	A1	A0	Voltage input to P6
1	0	0	$0{\cdot}6V_{CC}$ to 13·2V
0	1	1	$0{\cdot}45V_{CC}$ to $0{\cdot}6V_{CC}$
0	1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}45V_{CC}$
0	0	1	$0{\cdot}15V_{CC}$ to $0{\cdot}3V_{CC}$
0	0	0	0V to $0{\cdot}15V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	0V to $0{\cdot}2V_{CC}$
0	1	Always valid
1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}7V_{CC}$
1	1	$0{\cdot}8V_{CC}$ to 13·2V

Table 4 Address selection

A : Acknowledge bit
MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select
T1 : Test mode selection
T0 : Charge pump disable
OS : Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P2*, P1*, P0* : Control output port states
POR : Power On Reset indicator
FL : Phase lock detect flag
I2, I1, I0 : Digital information from ports P7, P5 and P4 respectively
A2, A1, A0 : 5-level ADC data from P6 (see Table 3)

NOTE
* Don't care condition on SP5510S.

Fig. 3 Data formats

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

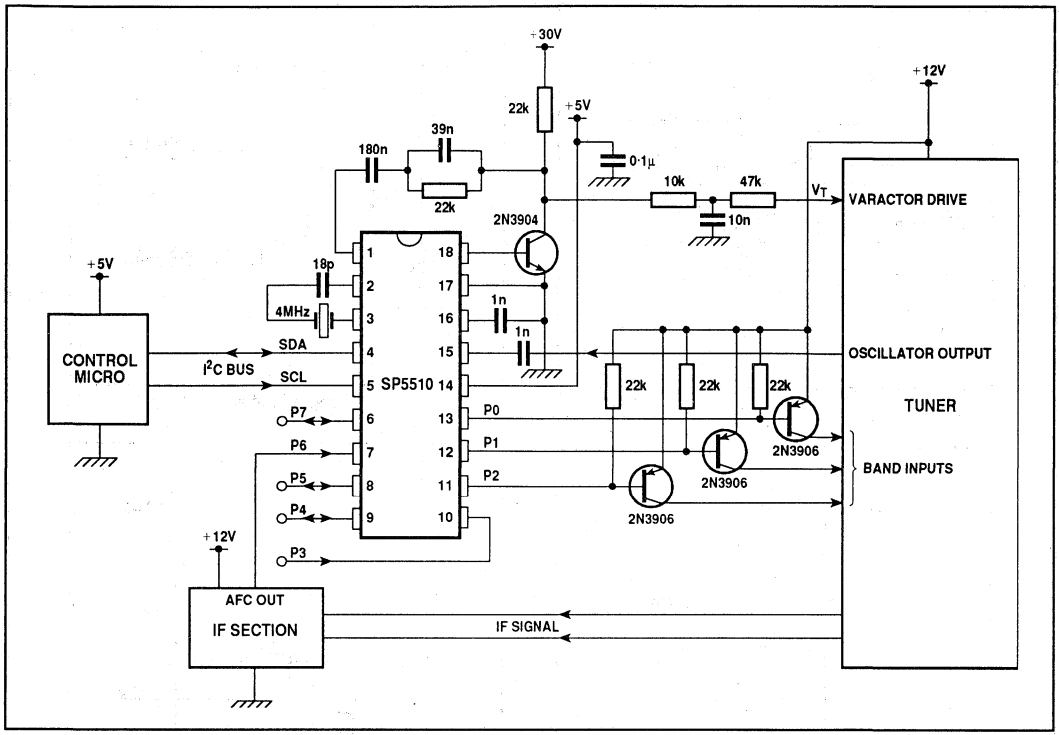


Fig. 4 Typical application

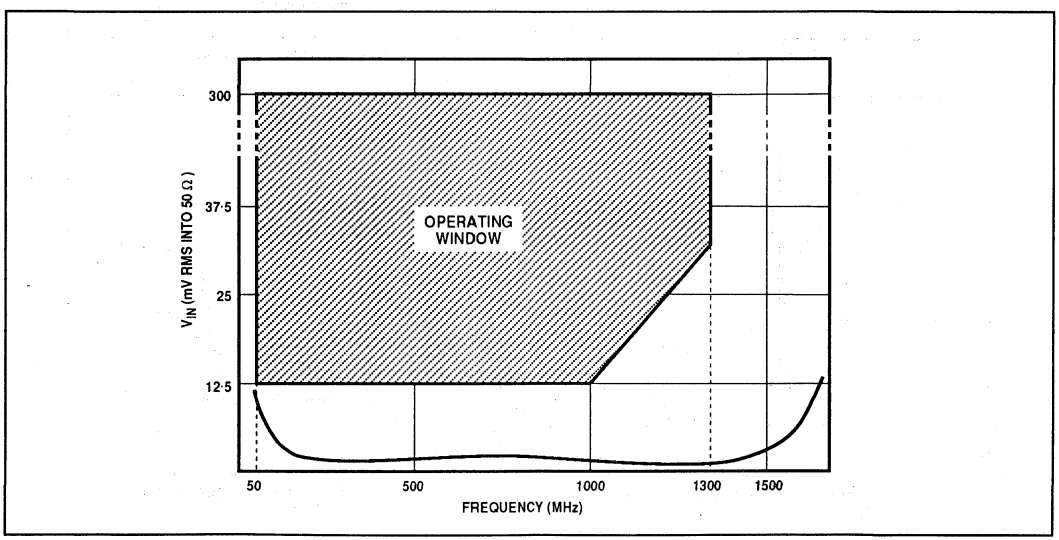


Fig. 5 Typical input sensitivity

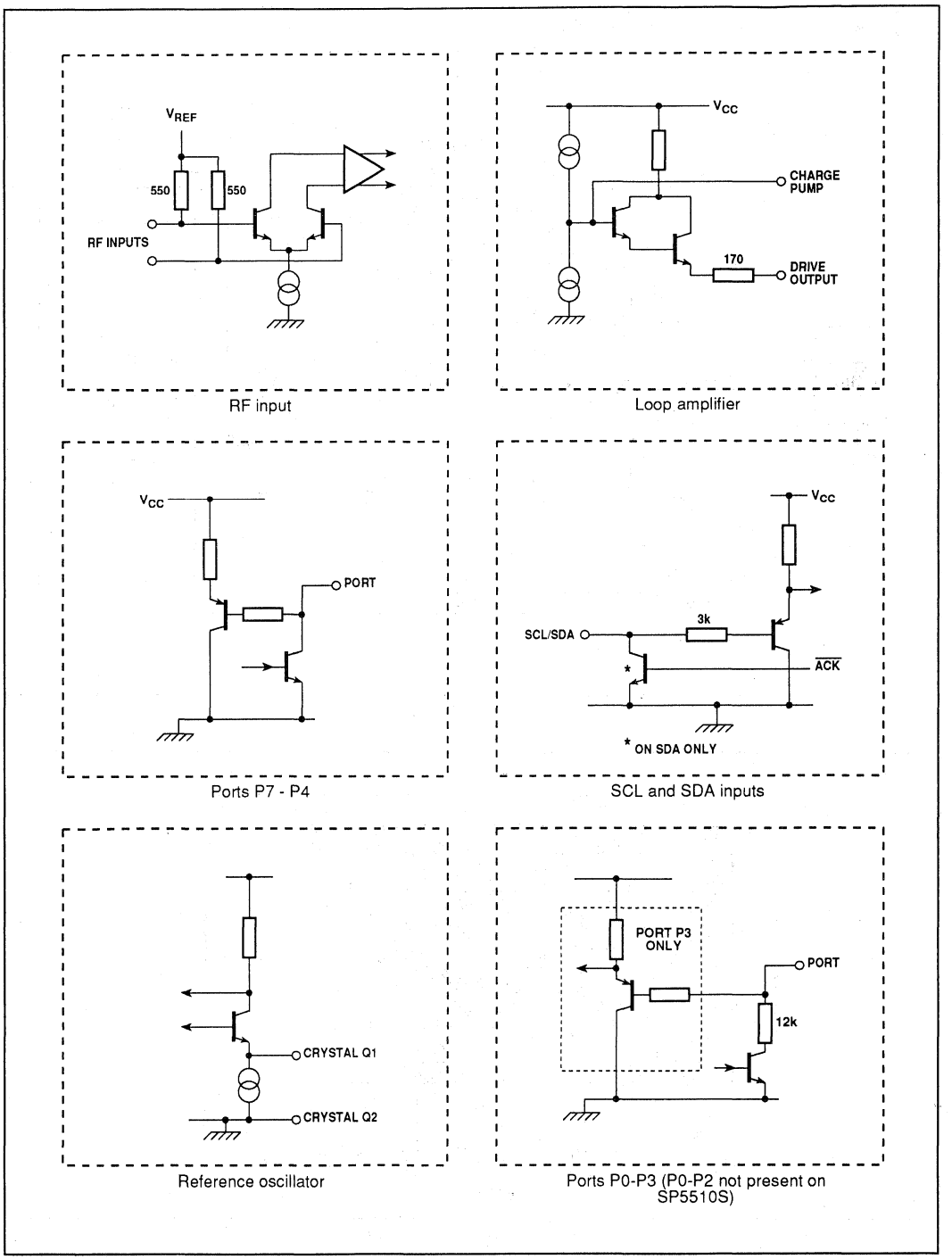


Fig. 6 SP5510 input/output interface circuits

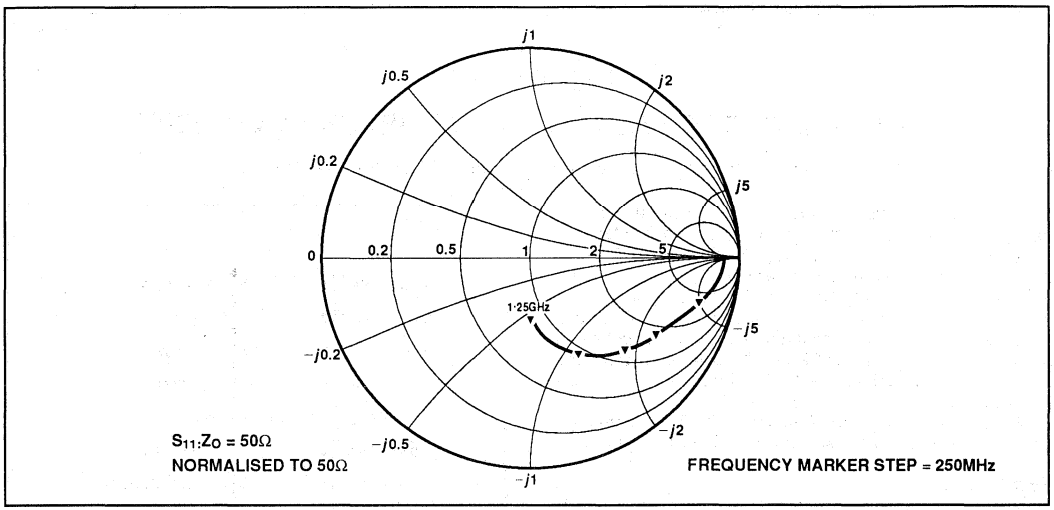


Fig. 7 Typical input impedance, SP5510

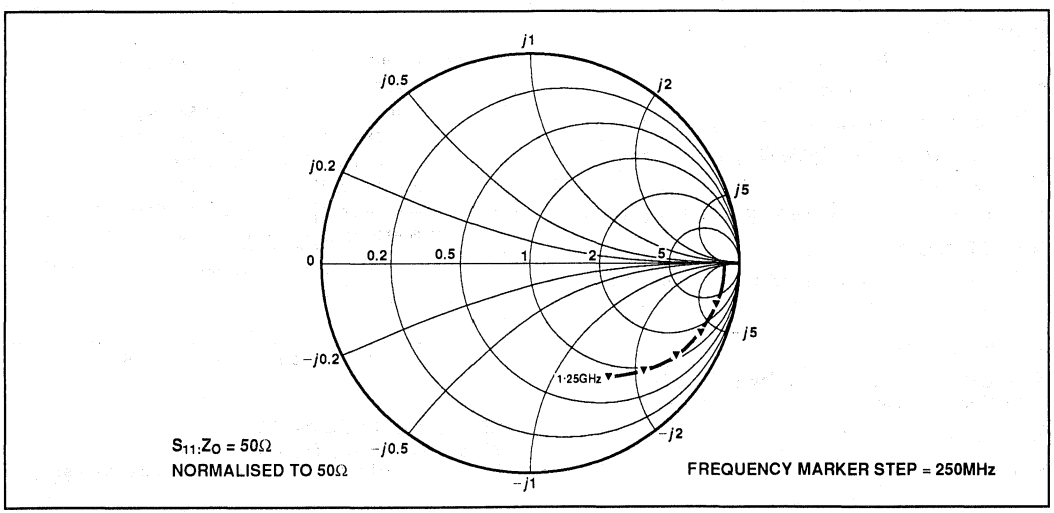


Fig. 8 Typical input impedance, SP5510S

SP5511

1.3 GHz BIDIRECTIONAL I²C BUS 4-ADDRESS SYNTHESISER

(Supersedes version in April 1994 Consumer IC Handbook, HB3120 - 2.0)

The SP5511 is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. In 18-lead plastic DIL package, the SP5511 has three addressable current-limited output ports (P0-P3) and four bi-directional output ports (P0-P2) and four addressable bi-directional open-collector ports (P4-P7) of which P6 is also a 3-bit 5-level ADC input. The information on these ports can be read via the I²C BUS. The SP5511S is a variant in a 16-lead miniature plastic package, without P0-P2 but functionally identical in other respects to the SP5511.

The device has four programmable I²C BUS addresses, allowing two or more synthesisers to be used in a system.

FEATURES

- Complete 1·3GHz Single Chip System
- Programmable via the I²C BUS
- Low Power Consumption (240mW Typ.)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 7 Controllable Outputs, 4 Bi-directional (SP5511)
- 4 Bi-directional Controllable Outputs (SP5511S)
- 5-Level ADC
- Variable I²C BUS Address for Picture in Picture TV
- ESD Protection *

* Normal ESD handling precautions should be observed.

APPLICATIONS

- Satellite TV when Combined with SP4902 2·5GHz Prescaler
- Cable Tuning Systems
- VCRs

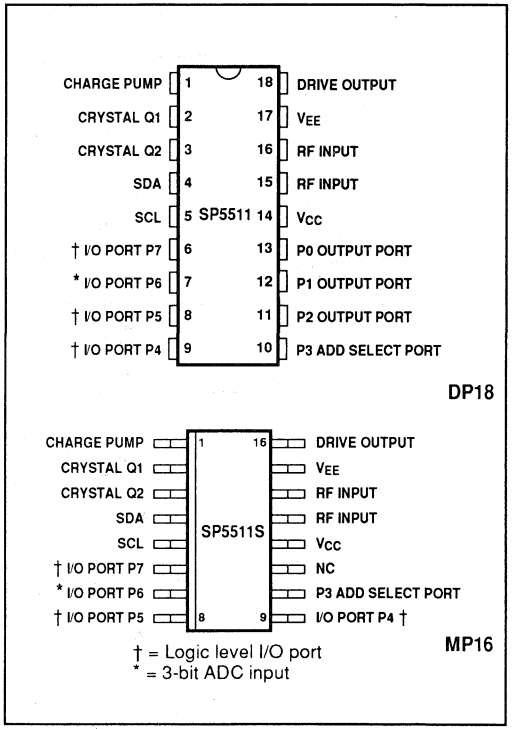


Fig. 1 Pin connections – top view

ORDERING INFORMATION

SP5511 NA DP (18-lead plastic package)
SP5511S NA MP (16-lead miniature plastic package)

ELECTRICAL CHARACTERISTICS

T_{AMB} = −10°C to +80°C, V_{CC} = +4·5V to +5·5V. All pin references are to the SP5511 (DP18 package).
These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated. Reference frequency 4MHz unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	14		48	60	mA	V_{CC} = 5V
Prescaler input voltage	15,16	12·5		300	mVrms	80MHz to 1GHz
		30		300	mVrms	1·3GHz, see Fig. 5
Prescaler input impedance	15,16		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4,5	3		5·5	V	
Input low voltage	4,5	0		1·5	V	
Input high current	4,5			10	µA	Input voltage = V_{CC}
Input low current	4,5			−10	µA	Input voltage = 0V
Leakage current	4,5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0·4	V	Sink current = 3mA
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	18	500				V pin 18 = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 2)
Crystal oscillator drive level			40		mV p-p	
Crystal oscillator negative resistance	2	750			Ω	
Output Ports						
P0-P2 sink current (see note 1)	11-13	0·7	1	1·5	mA	V_{OUT} = 12V
P0-P2 leakage current (see note 1)	11-13			10	µA	V_{OUT} = 13·2V
P4-P7 sink current	6-9	10			mA	V_{OUT} = 0·7V
P4-P7 leakage current	6-9			10	µA	V_{OUT} = 13·2V
Input Ports						
P3 input current high	10			1	mA	V pin 10 = 13·2V
P3 input current low	10			−0·5	mA	V pin 10 = 0V
P4, P5, P7 input voltage low	6,8,9			0·8	V	
P4, P5, P7 input voltage high	6,8,9	2·7			V	
P6 input current high	7			+10	µA	See Table 3 for ADC levels
P6 input current low	7			−10	µA	

NOTES
1. Ports P0-P2 not present on the SP5511S
2. The maximum resistance quoted refers to all conditions, including start-up.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V

Parameter	Pin		Value		Units	Conditions
	SP5511	SP5511S	Min.	Max.		
Supply voltage	14	12	−0·3	7	V	
RF input voltage	15,16	13,14		2·5	V p-p	
Port voltage	6-9,11-13	6-9	−0·3	14	V	Port in off state
	6-9	6-9	−0·3	6	V	Port in on state
	11-13		−0·3	14	V	Port in on state
	10	10	−0·3	V_{CC}+0·3	V	
Total port output current	6-9,11-13	6-9		50	mA	
RF input DC offset	15-16	13-14	−0·3	V_{CC}+0·3	V	
Charge pump DC offset	1	1	−0·3	V_{CC}+0·3	V	
Drive output DC offset	18	16	−0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	2	−0·3	V_{CC}+0·3	V	
SDA, SCL input voltage	4,5	4,5	−0·3	V_{CC}+0·3	V	With V_{CC} applied
			−0·3	5·5	V	V_{CC} not applied
Storage temperature			−55	+150	°C	
Junction temperature				+150	°C	
DP18 thermal resistance, chip-to-ambient				78	°C/W	
DP18 thermal resistance, chip-to-case				24	°C/W	
MP16 thermal resistance, chip-to-ambient				111	°C/W	
MP16 thermal resistance, chip-to-case				41	°C/W	
Power consumption at 5·5V				363	mW	

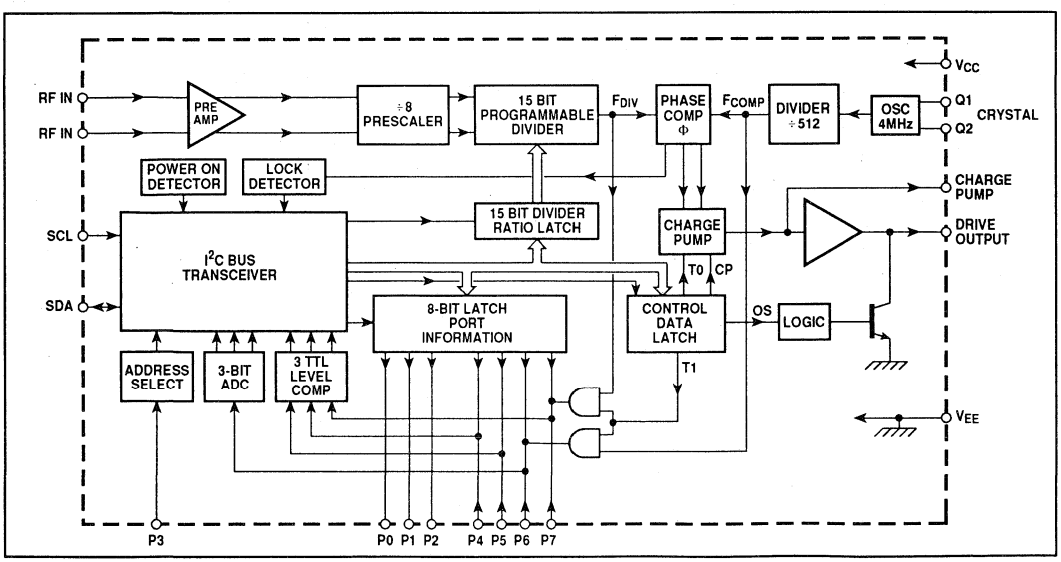


Fig. 2 Block diagram. (Ports P0-P2 not present on SP5511S)

FUNCTIONAL DESCRIPTION

The SP5511 is programmed from an I^2C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I^2C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I^2C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The address input circuit is shown in Fig.6.The LSB of the address Byte (R/$\overline{W}$) sets the device into read mode if it is high and write mode if it is low. When the SP5511 receives a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed. When the SP5511 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status Byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that Byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data Bytes can be entered without the need to re-address the device until an I^2C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (i.e., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Figs. 7 and 8.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP}.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-chip 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7·8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170μA and a logic 0 for ±50μA, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{COMP} to P6 and F_{DIV} to P7.

Byte 5 programs the output ports P0-P7, a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below a nominal 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic1). These inputs will then respond to data complying with standard TTL voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5-level ADC.

The 5-level ADC can be used to feed AFC information to the microprocessor from the IF section of the television, as illustrated in Fig. 4.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	P6	P5	P4	P3	P2*	P1*	P0*	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	**Byte 2**

Table 2 Read data format

A2	A1	A0	Voltage input to P6
1	0	0	$0{\cdot}6V_{CC}$ to $13{\cdot}2V$
0	1	1	$0{\cdot}45V_{CC}$ to $0{\cdot}6V_{CC}$
0	1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}45V_{CC}$
0	0	1	$0{\cdot}15V_{CC}$ to $0{\cdot}3V_{CC}$
0	0	0	0V to $0{\cdot}15V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	0V to $0{\cdot}1V_{CC}$
0	1	Open circuit
1	0	$0{\cdot}4V_{CC}$ to $0{\cdot}6V_{CC}$†
1	1	$0{\cdot}9V_{CC}$ to V_{CC}

Table 4 Address selection

A	:	Acknowledge bit
MA1, MA0	:	Variable address bits (see Table 4)
CP	:	Charge Pump current select
T1	:	Test mode selection
T0	:	Charge pump disable
OS	:	Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P2*, P1*, P0*	:	Control output port states
POR	:	Power On Reset indicator
FL	:	Phase lock detect flag
I2, I1, I0	:	Digital information from ports P7, P5 and P4 respectively
A2, A1, A0	:	5-level ADC data from P6 (see Table 3)

NOTE

† Programmed by connecting a 15kΩ resistor between pin 10 and V_{CC}

* Don't care condition on SP5511S.

Fig. 3 Data formats

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

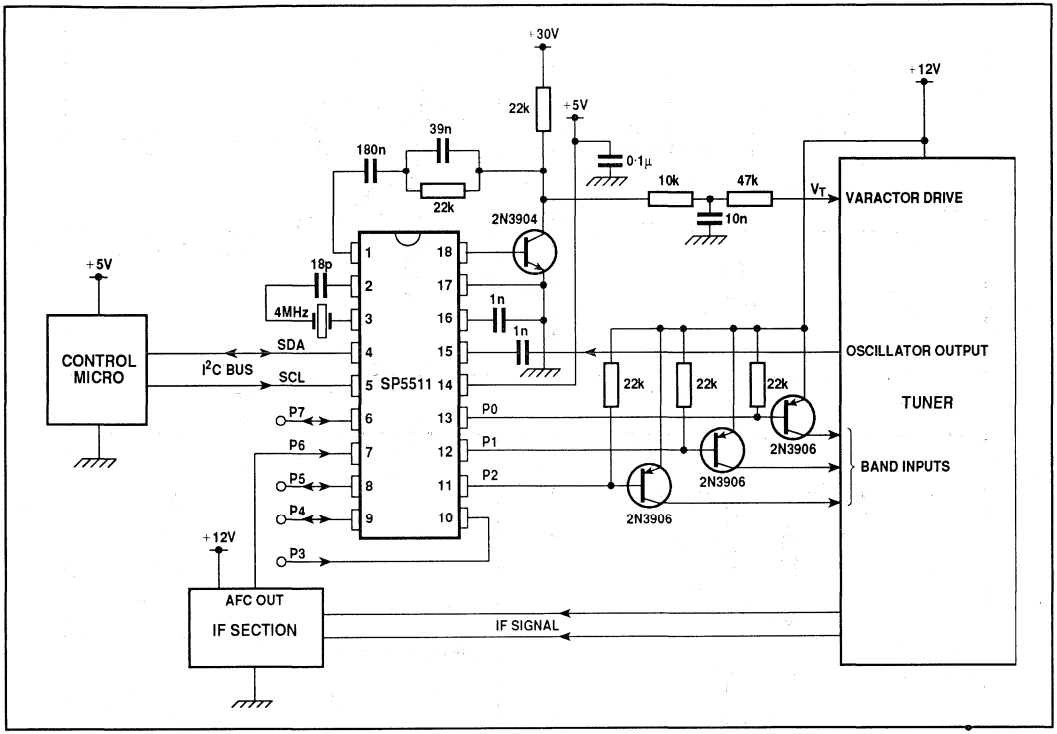


Fig. 4 Typical application

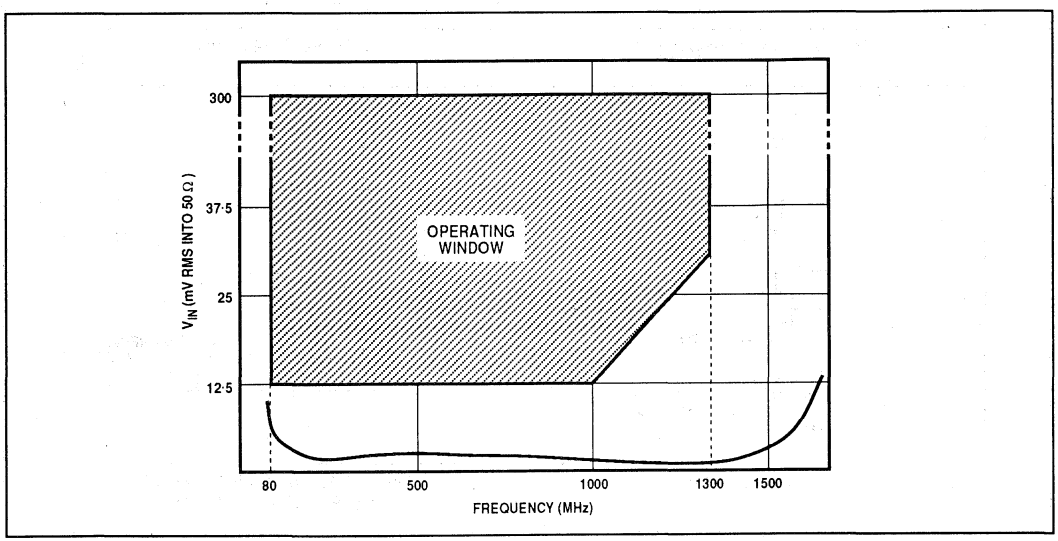
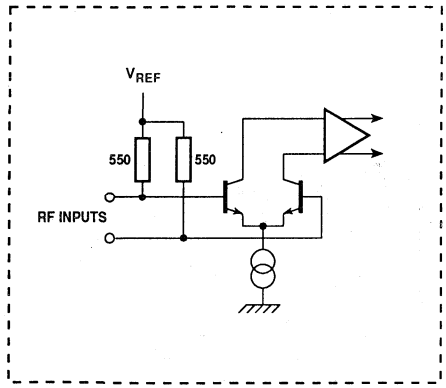
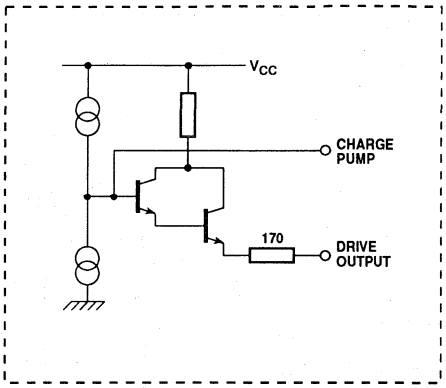


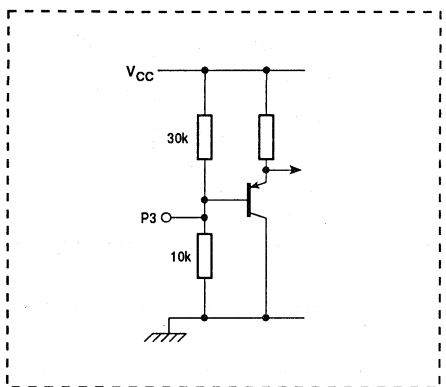
Fig. 5 Typical input sensitivity



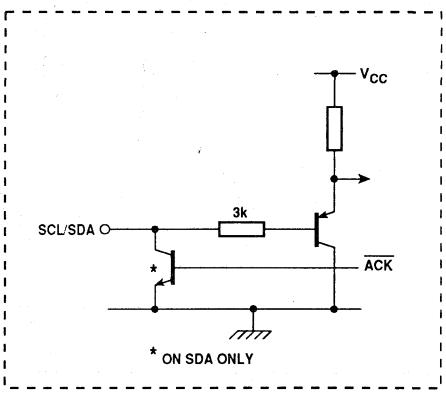
RF input



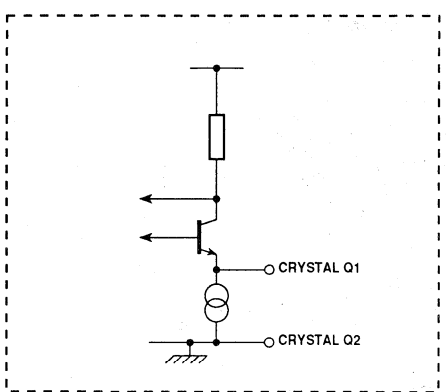
Loop amplifier



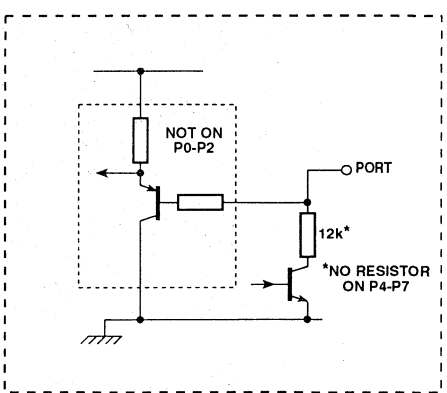
Address programming port



SCL and SDA inputs



Reference oscillator



Ports P0-P2 and P4-P7 (SP5511).
P4- P7 only on SP5511S

Fig. 6 SP5511 input/output interface circuits

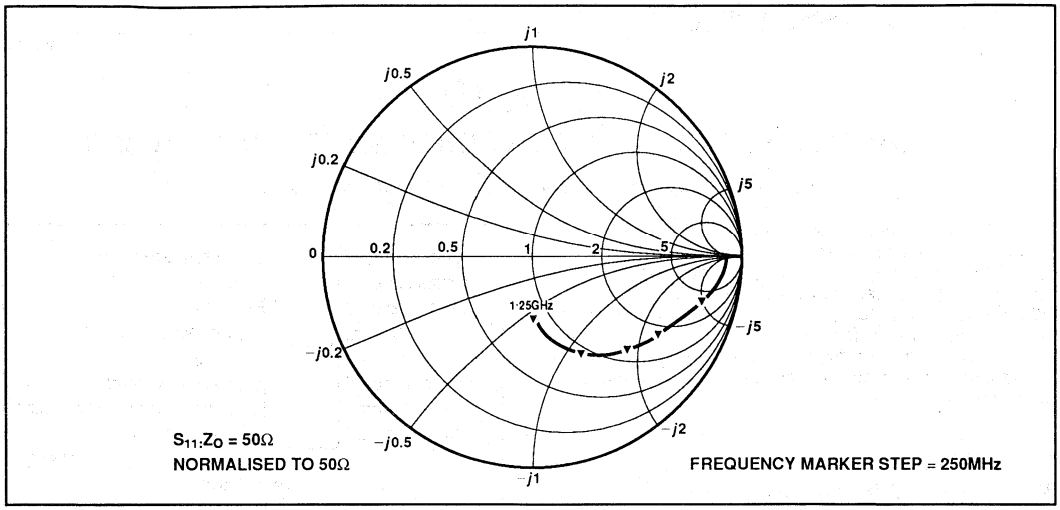


Fig. 7 Typical input impedance, SP5511

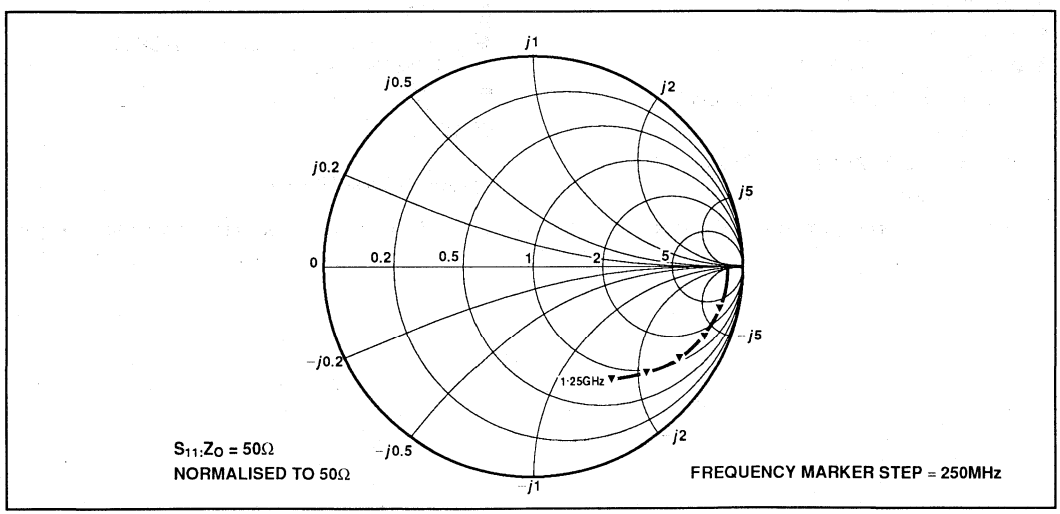


Fig. 8 Typical input impedance, SP5511S

2384-3.4

SP5512

1·3 GHz BIDIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

(Supersedes version in April 1994 Consumer IC Handbook, HB3120 - 2.0)

The SP5512 is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device has six controllable open-collector output ports (P2-P7), each capable of sinking 20mA. In addition, P6 is a 3-bit 5-level ADC input. The information on these ports can be read via the I²C BUS.

The device has one fixed I²C BUS address and three programmable addresses, allowing two or more synthesisers to be used in a system.

FEATURES

- Complete 1·3GHz Single Chip System
- Programmable via the I²C BUS
- Low Power Consumption (215mW Typ.)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 6 Controllable Outputs, 5 Bi-directional
- 5-Level ADC
- Variable I²C BUS Address for Picture in Picture TV
- ESD Protection *

* Normal ESD handling precautions should be observed.

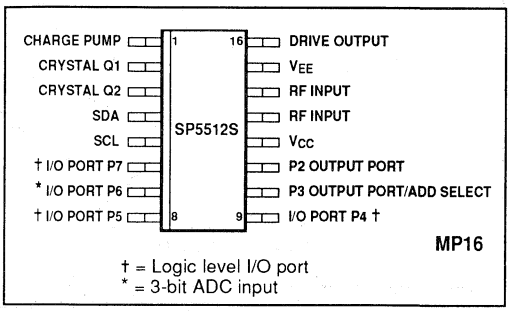


Fig. 1 Pin connections – top view

APPLICATIONS

- Satellite TV when Combined with SP4902 2·5GHz Prescaler
- Cable Tuning Systems
- VCRs

ORDERING INFORMATION

SP5512S KG MPAS (16-lead miniature plastic package)

ELECTRICAL CHARACTERISTICS

T_{AMB} = −10°C to +80°C, V_{CC} = +4·5V to +5·5V.
These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated. Reference frequency 4MHz unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	12		43	53	mA	V_{CC} = 5V
Prescaler input voltage	13,14	12·5		300	mVrms	50MHz to 1GHz
		30		300	mVrms	1·3GHz, see Fig. 5
Prescaler input impedance	13,14		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4,5	3		5·5	V	
Input low voltage	4,5	0		1·5	V	
Input high current	4,5			10	µA	Input voltage = V_{CC}
Input low current	4,5			−10	µA	Input voltage = 0V
Leakage current	4,5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0·4	V	Sink current = 3mA
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	16	500				V pin 16 = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 2)
Crystal oscillator drive level			40		mV p-p	
Crystal oscillator negative resistance	2	750			Ω	
Output Ports						
P2-P7 sink current (see note 1)	6-11	20			mA	V_{OUT} = 0·7V, see note 1
P2-P7 leakage current (see note 1)	6-11			10	µA	V_{OUT} = 13·2V
Input Ports						
P3 input current high	10			+10	µA	V pin 10 = 13·2V
P3 input current low	10			−10	µA	V pin 10 = 0V
P4, P5, P7 input voltage low	6,8,9			0·8	V	
P4, P5, P7 input voltage high	6,8,9	2·7			V	
P6 input current high	7			+10	µA	See Table 3 for ADC levels
P6 input current low	7			−10	µA	

NOTES
1. Source impedance between all output ports and ground is approximately 5Ω. This should be taken into account when calculating output port saturation voltages.
2. The recommended crystal series resistance quoted refers to all conditions including start-up.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V.

Parameter	Pin	Value		Units	Conditions
		Min.	Max.		
Supply voltage	12	−0·3	7	V	
RF input voltage	13,14		2·5	V p-p	
Port voltage	6-11	−0·3	14	V	Port in off state
	6-11	−0·3	6	V	Port in on state
Total port output current	6-11		50	mA	
RF input DC offset	13-14	−0·3	V_{CC}+0·3	V	
Charge pump DC offset	1	−0·3	V_{CC}+0·3	V	
Drive output DC offset	16	−0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	−0·3	V_{CC}+0·3	V	
SDA, SCL input voltage	4,5	−0·3	V_{CC}+0·3	V	With V_{CC} applied
		−0·3	5·5	V	V_{CC} not applied
Storage temperature		−55	+150	°C	
Junction temperature			+150	°C	
MP16 thermal resistance, chip-to-ambient			111	°C/W	
MP16 thermal resistance, chip-to-case			41	°C/W	
Power consumption at 5·5V			321	mW	

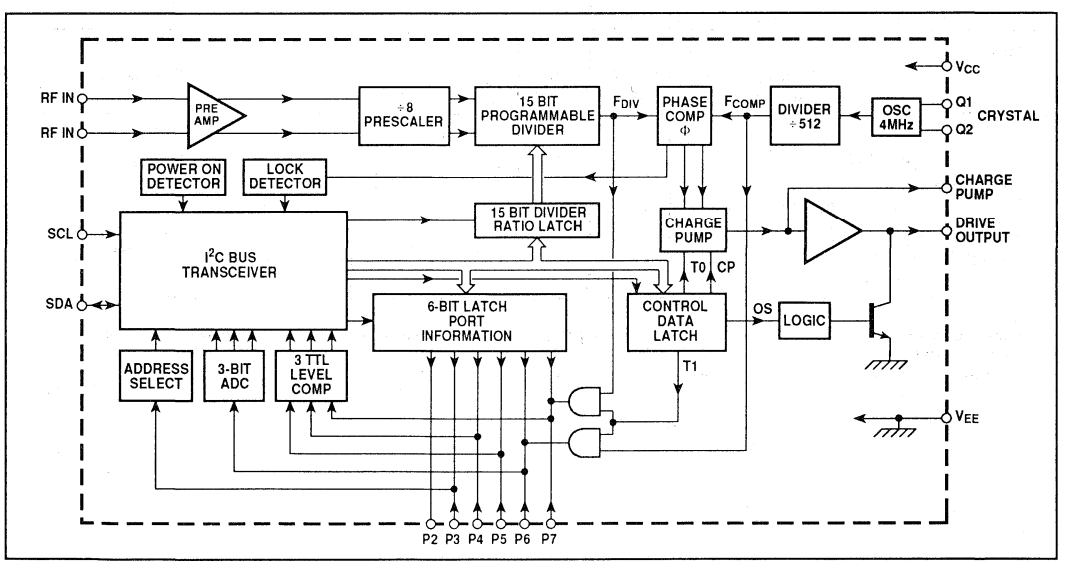


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The SP5512 is programmed from an I^2C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I^2C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I^2C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The LSB of the address byte (R/$\overline{W}$) sets the device into read mode if it is high and write mode if it is low. When the SP5512 receives a correct address byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are programmed. When the SP5512 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first bit of the next byte determines whether that byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data bytes can be entered without the need to re-address the device until an I^2C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (e.g., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Fig. 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP}.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-chip 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7·8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170µA and a logic 0 for ±50µA, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{COMP} to P6 and F_{DIV} to P7.

Byte 5 programs the output ports P2-P7, a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below a nominal 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic1). These inputs will then respond to data complying with standard TTL voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5-level ADC.

The 5-level ADC can be used to feed AFC information to the microprocessor from the IF section of the television, as illustrated in Fig. 4.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	P6	P5	P4	P3	P2	X	X	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	**Byte 2**

Table 2 Read data format

A2	A1	A0	Voltage input to P6
1	0	0	$0{\cdot}6V_{CC}$ to 13·2V
0	1	1	$0{\cdot}45V_{CC}$ to $0{\cdot}6V_{CC}$
0	1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}45V_{CC}$
0	0	1	$0{\cdot}15V_{CC}$ to $0{\cdot}3V_{CC}$
0	0	0	0V to $0{\cdot}15V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	0V to $0{\cdot}2V_{CC}$
0	1	Always valid
1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}7V_{CC}$
1	1	$0{\cdot}8V_{CC}$ to 13·2V

Table 4 Address selection

A : Acknowledge bit
MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select
T1 : Test mode selection
T0 : Charge pump disable
OS : Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P2 : Control output port states
POR : Power On Reset indicator
FL : Phase lock detect flag
I2, I1, I0 : Digital information from ports P7, P5 and P4 respectively
A2, A1, A0 : 5-level ADC data from P6 (see Table 3)
X : Don't care

Fig. 3 Data formats

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

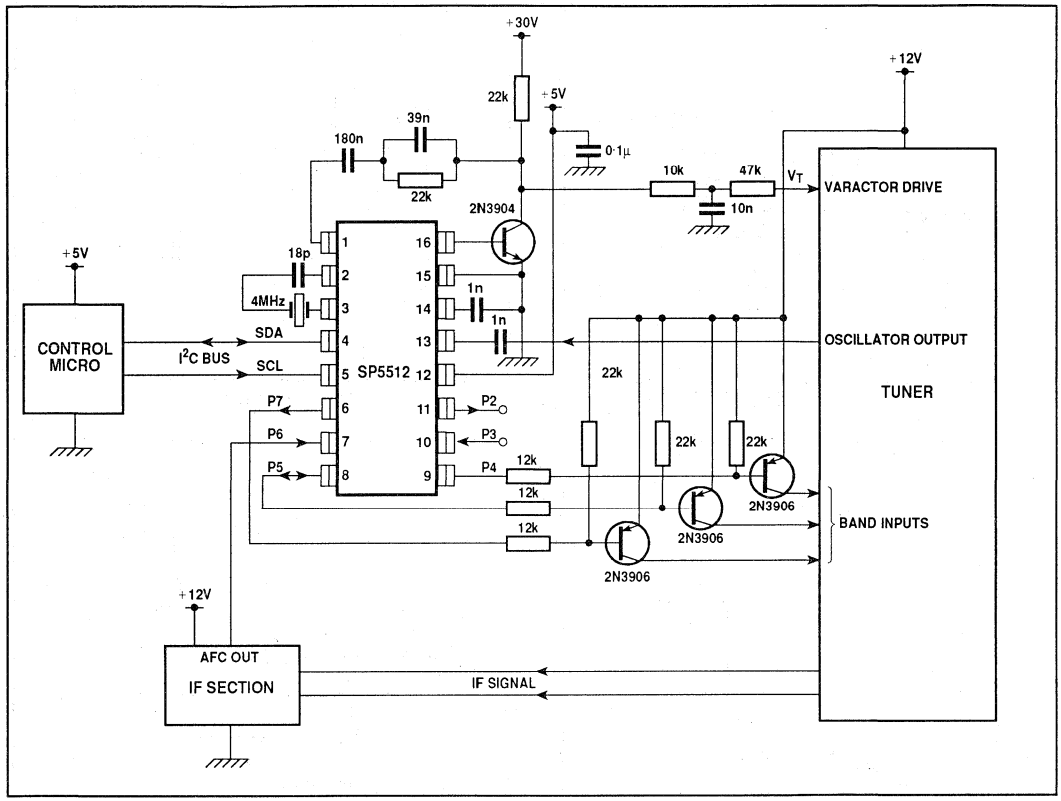


Fig. 4 Typical application

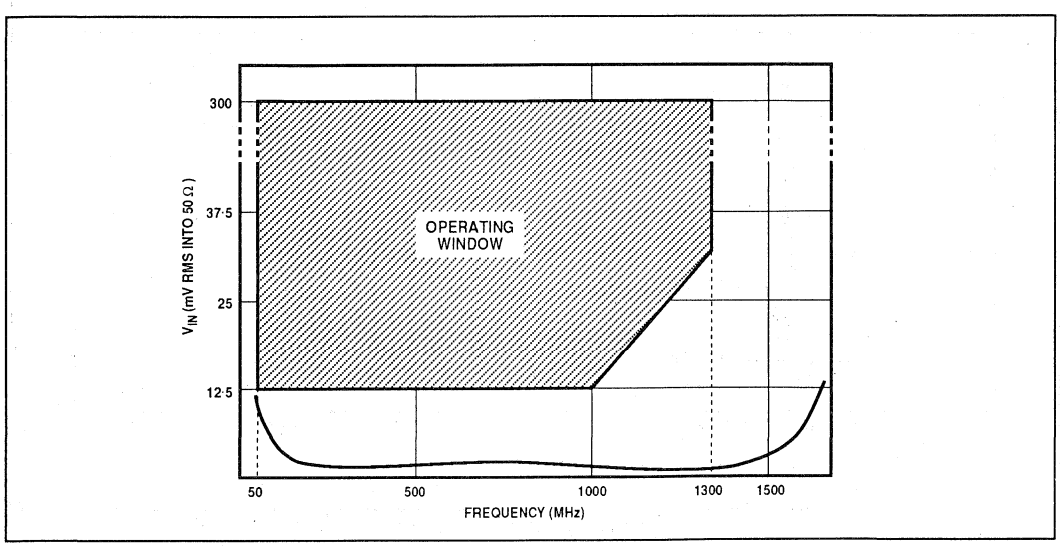


Fig. 5 Typical input sensitivity

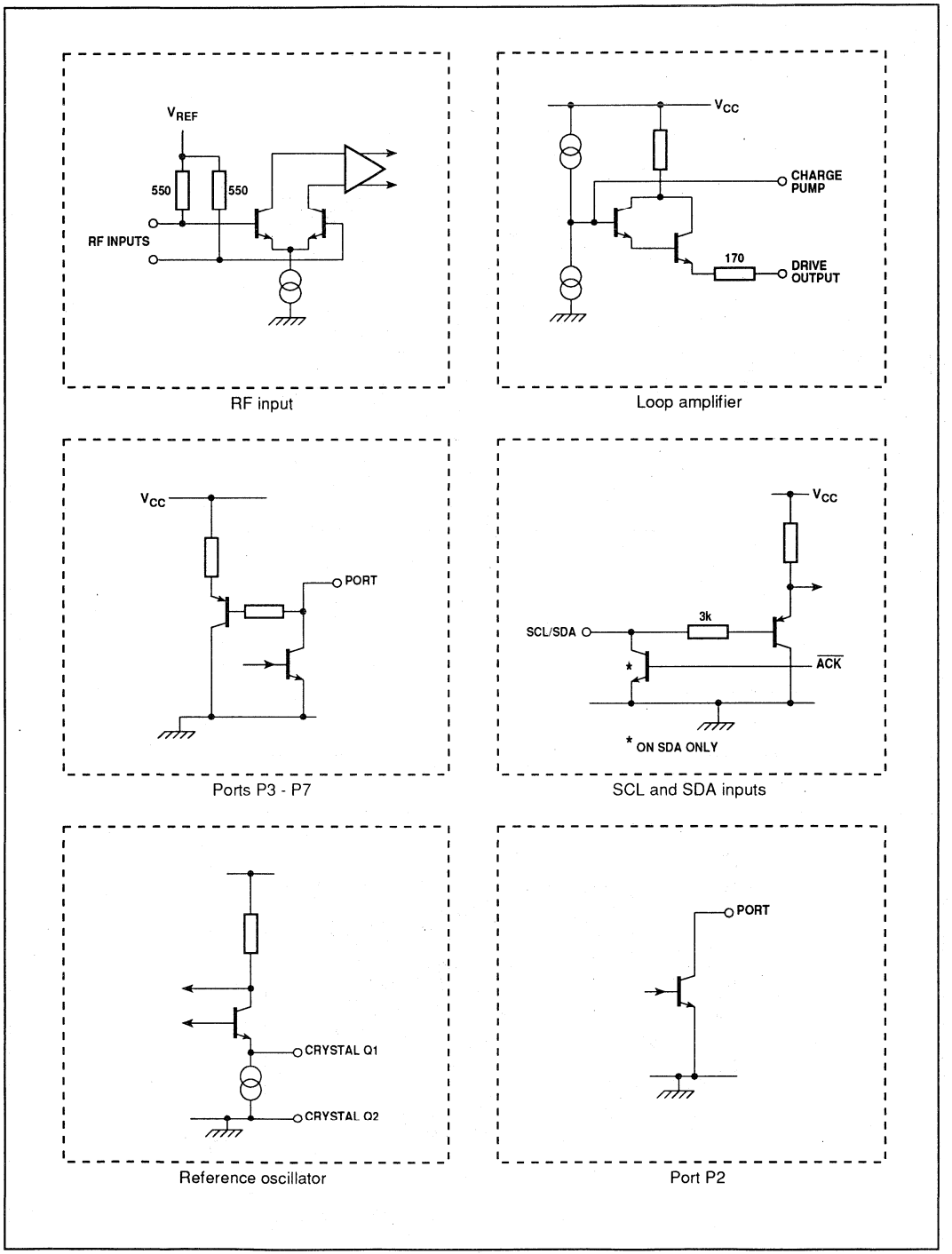


Fig. 6 Input/output interface circuits

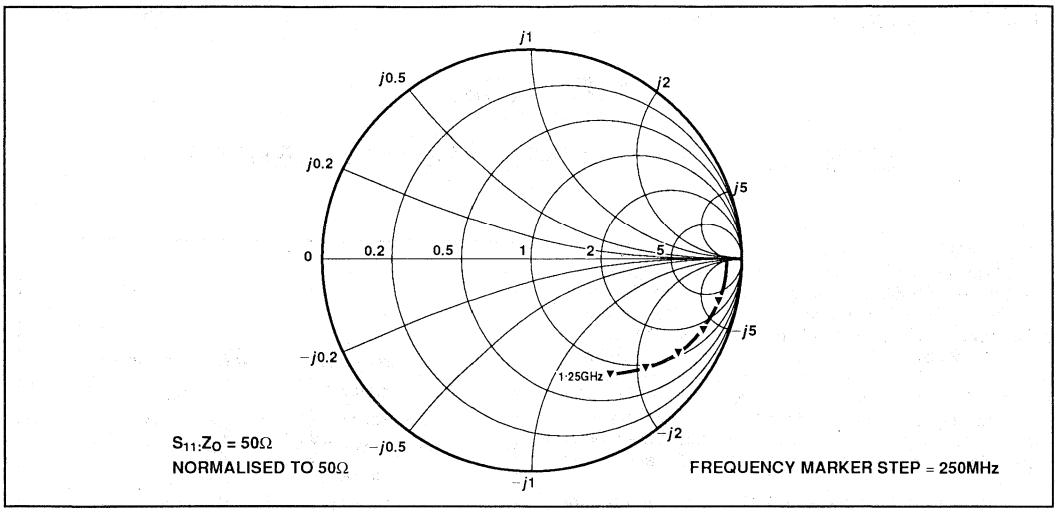


Fig. 7 Typical input impedance

SP5654

2.7GHz 3–WIRE BUS CONTROLLED SYNTHESISER

The SP5654 is a single chip frequency synthesiser designed for satellite TV tuning systems. It is a programming variant of the SP5655 allowing the design of one tuner with either I^2C bus or a 3–wire bus format depending on which device is inserted. The device when used with a varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide–by–16 prescaler with its own preamplifier and a 14/15 bit programmable divider controlled by a serially loaded data register. Four independently programmable open collector outputs are included. The device contains five modes of operation each compatible with Toshiba 18 and 19 bit software.

The comparison frequencies are obtained from a crystal controlled on–chip oscillator typically operating at 4MHz. The comparator has a charge pump output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

FEATURES

- Complete 2.7GHz Single Chip System
- High Sensitivity RF Input
- Low power Consumption (5V, 30mA)
- On–Chip Oscillator with 1kΩ negative resistance
- On chip oscillator start–up circuit
- Programming Compatible with Toshiba TD6380, TD6381 and TD6382#
- Pin compatible with SP5655#
- 5 Modes of Operation with different step sizes, see Table 1; each selectable with 18 or 19 bit transmission length.
- Single Port 18/19 Bit Serial Data Entry
- Auto select for Data transmission length, 18 or 19
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- Charge Pump Disable
- Four Controllable Outputs
- ESD Protection †

See notes on pin and programming compatibility

† Normal ESD handling procedures should be observed.

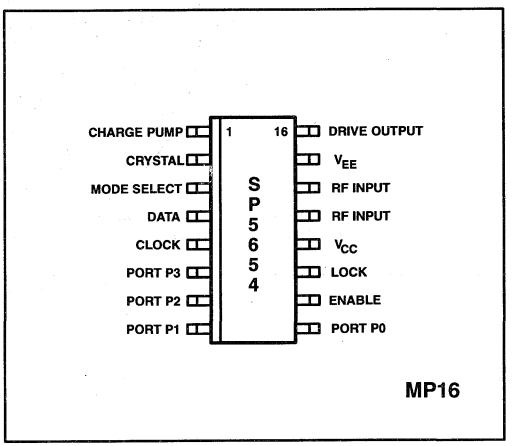


Fig. 1 Pin connections – top view

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

ORDERING INFORMATION

SP5654/KG/MPAS (Tubes)
SP5654/KG/MPAD (Tape and Reel)

ELECTRICAL CHARACTERISTICS

T_{amb}= −20°C to +80°C, V_{CC}=+4.5V to +5.5V. Reference frequency =4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	12		30	40	mA	Typical applies to V_{CC} = 5V
Prescaler Input Voltage		13, 14	12.5		300	mV_{rms}	300MHz to 2GHz sinewave.
			40		300	mV_{rms}	120MHz & 2.7GHz See Fig.6.
Prescaler Input Impedance Input Capacitance		13, 14		50 2		Ω pF	
Data Clock and Enable							
High Level Input Voltage		4, 5, 10	3		V_{CC}	V	
Low Level Input Voltage		4, 5, 10	0		1.5	V	
High Level Input Current		4, 5, 10			10	µA	V_{IN}=5.5V V_{CC}=5.5V
Low Level Input Current		4, 5, 10			−10	µA	V_{IN}=0V V_{CC}=5.5V
Input Hysteresis		4, 5, 10		0.8		V	
Clock Rate		5			500	kHz	
Timing Information							
Data Setup Time	t_{SU}	4	300			ns	See Fig.4
Data Hold Time	t_{HD}	4	600			ns	See Fig. 4
Enable Setup time	t_{ES}	10	300			ns	See Fig. 4
Enable Hold Time	t_{EH}	10	600			ns	See Fig. 4
Clock–to–Enable Time	t_{CE}	10	300			ns	See Fig. 4
Clock Low Period	t_{LO}	5	600			ns	See Fig. 4
Clock High Period	t_{HI}	5	600			ns	See Fig. 4
Mode Select							
High Level Input Current		3			700	µA	V_{IN}=5.5V V_{CC}=5.5V
Low Level Input Current		3			−700	µA	V_{IN}=0V V_{CC}=5.5V
Charge Pump Output Current		1		±150		µA	V pin 1 = 2.0V, device 'out of lock'
Charge Pump Output Current		1		±50		µA	V pin 1 = 2.0V, device 'locked'
Charge Pump Output Leakage Current		1			±5	nA	V pin 1 = 2.0V, charge pump disabled
Charge Pump Drive Output Current		16	1			mA	V pin 16 = 0.7V
Charge Pump Amplifier Gain				6400			Pin 18 Current = 100µA
Oscillator Temperature Stability					2	ppm/°C	
Oscillator Stability with Supply Voltage					2	ppm/V	
Recommended Crystal Series Resistance			10		200	Ω	"Parallel resonant crystal." Figure quoted is under all conditions including start up.
Crystal Oscillator Drive Level		2		80		mV p–p	
Crystal Oscillator Negative Resistance		2	750			Ω	Includes temperature and process tolerances
Reference Crystal Frequency		2	4		8	MHz	
External Reference input Frequency		2	2		16	MHz	AC coupled sinewave
External Reference input Amplitude		2	400		1000	mV_{p-p}	AC coupled sinewave

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb}= –20°C to +80°C, V_{CC}= +4.5V to +5.5V. Reference frequency =4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Ports and Lock output							
Sink Current		6–9, 11	10			mA	V_{out}=0.7V
Lock Leakage Current		11			10	µA	V_{out}=V_{CC}
Port Leakage Current		6–9			10	µA	V_{out}=13.2V
Varactor Drive Amp Disable		10	–50			µA	V_{pin} 10 < 0V. Current sourced from device
Charge Pump Disable		4	–50			µA	V_{pin} 4 < 0V. Current sourced from device
Test Mode Enable		5	–50			µA	V_{pin} 5 < 0V. Current sourced from device. See Table 2

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE}=0V

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Supply voltage	12	–0.3	7	V	
Prescaler input voltage	13, 14		2.5	Vp–p	
Prescaler DC offset	13, 14	–0.3	V_{CC}+0.3	V	
Port voltage	6–9	–0.3	14	V	Port in off state
		–0.3	6	V	Port in on state
Total port output current	6–9		50	mA	
Loop amplifier DC offset	1, 16	–0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	–0.3	V_{CC}+0.3	V	
3–wire bus inputs	4, 5, 10	–0.7	6	V	
Mode select input	3	–0.3	V_{CC}+0.3	V	
Lock output voltage	11	–0.3	V_{CC}+0.3	V	
Lock output current	11		15	mA	
Storage temperature		–55	+150	°C	
Junction temperature			+150	°C	
MP16 thermal resistance, chip–to–ambient			111	°C/W	
MP16 thermal resistance, chip–to–case			41	°C/W	
Power consumption			220	mW	All ports off
ESD protection	All	4		kV	MIL STD 883 TM 3015

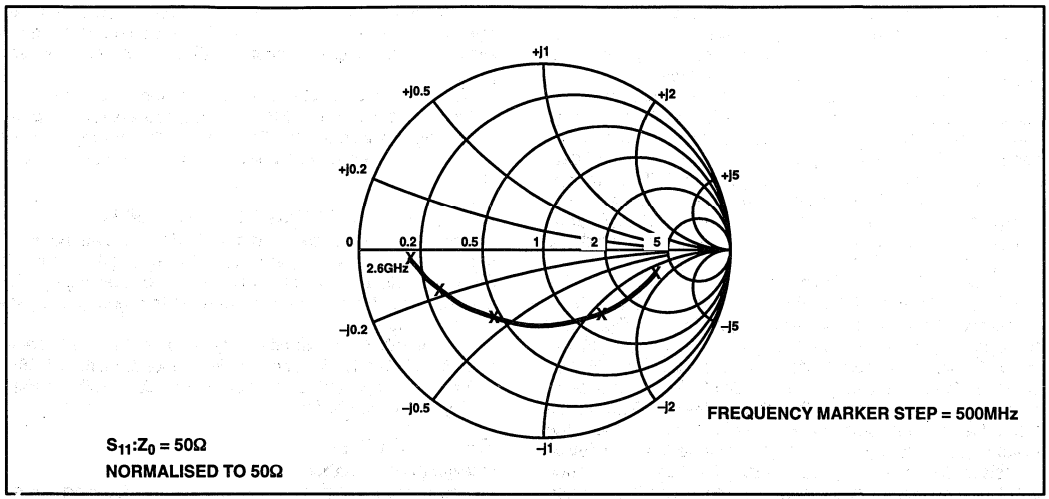


Fig. 2 Typical input impedance

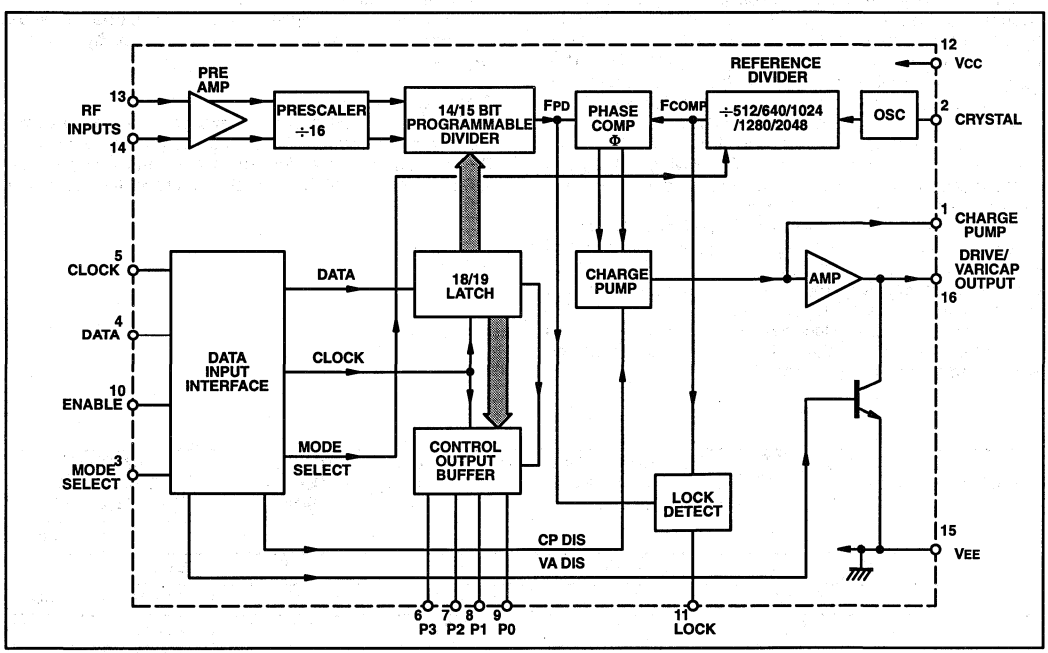


Fig. 3 Block diagram

FUNCTIONAL DESCRIPTION

The SP5654 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor, to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard data, clock and enable three–wire bus. The data load consists of a single word, which contains the frequency and port information, and is only transferred to the internal data shift register during an enable high period. The clock is disabled during low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable, so giving improved fine tuning facility for digital AFC etc.

The device has 5 modes of operation, as defined in Table 1, and each of these modes can accept either 18–bit or 19–bit data entry. The format of the data entry is shown in Fig. 4, and consists of 4–bits for port switching, plus 14/15 bits to control the 15–bit programmable divider. For 18–bit data entry (4+14), the MSB of the 15–bit programmable divider is internally set to logic '0' effectively making the divider 14–bits. The device recognises the data entry as 18–bit when a falling edge at the enable input occurs during the 18th clock period. The device associates falling enable edges during the 19th clock period with 19–bit data entry. A falling edge at the enable input before the 18th clock period constitutes invalid data entry to the device.

The frequency is set by first selecting the required mode of operation as detailed in Table 1, and then by loading the programmable divider with the required 14/15–bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator where it is compared in phase and frequency to the internally generated comparison frequency, F_{COMP}.

The comparison frequency F_{COMP} is obtained by dividing the output of the on–chip crystal controlled oscillator. The crystal frequency generally used is 4MHz, giving an F_{COMP} of 7.8125kHz in mode 4, which when multiplied back up to the LO gives a minimum step size of 125kHz.

The programmable divider is preceded by an input RF preamplifier and high speed low radiation prescaler. The preamplifier is arranged to be self oscillating, so giving excellent input sensitivity. The input impedance and sensitivity are shown in Fig. 2 and 6 respectively.

The device contains a lock detect circuit which generates a flag when the loop has attained lock. The 'in lock' condition is indicated by a high impedance state.

The charge pump current is initially set to ±150μA. When the device attains frequency lock, the charge pump current is switched to ±50μA, so improving the local oscillator short term jitter.

The device also contains four general purpose open collector output ports P0–P3. These outputs are each capable of sinking a minimum of 10mA, when the appropriate bits P0–P3 of the programming data, see Fig. 4 are set to a logic '1'.

PIN and PROGRAMMING COMPATIBILITY

The SP5654 may be used in SP5655 applications which require 3–wire bus as opposed to I^2C bus data format. In SP5655 applications where the reference crystal is grounded to pin 3, a small modification is required to ground the crystal as shown in Fig. 5.

Appropriate connections must also be to the mode select input (see Table 1). For each mode of operation, the SP5654 is programming and step size compatible with Toshiba devices as shown in Table 3.

TEST FEATURES

Charge pump disable

The charge pump may be disabled by sourcing current from the data input, i.e. by forcing a negative input voltage.

Varactor line disable

The charge pump amplifier drive output may be disabled by sourcing current from the enable input, i.e. by forcing a negative voltage.

Device test mode

Further test modes can be invoked by sourcing current from the clock input, i.e. by forcing a negative input voltage. These test modes when invoked are determined by the data held in the P1, P2 and P3 internal registers as detailed in Table 2.

MODE	'MODE SELECT' INPUT VOLTAGE	PROGRAMMABLE DIVIDER BIT LENGTH	REFERENCE DIVIDER RATIO	*FREQUENCY STEP SIZE (kHz)	*MAXIMUM OPERATING FREQUENCY (GHz)	
					14 bit	15 bit
4	0.85 V_{CC} – V_{CC}	14/15	512	125	2.0479	2.7000
3	0.65 V_{CC} – 0.75V_{CC} #	14/15	1280	50	0.8191	1.6383
2	OPEN CIRCUIT	14/15	1024	62.5	1.0239	2.0479
1	0.25 V_{CC} – 0.35V_{CC} †	14/15	2048	31.25	0.5119	1.0239
0	0 – 0.15 V_{CC}	14/15	640	100	1.6383	2.7000

*When used with a 4MHz crystal

Selected by connecting a 15kΩ resistor to V_{CC}

† Selected by connecting a 15kΩ resistor to V_{EE}

Table 1. Modes of operation

Test Mode	P1	P2	P3	Test Mode Description
0	0	0	0	Charge pump down 170µA
1	0	0	1	Charge pump up 170µA
2	1	0	0	Charge pump down 50µA
3	1	0	1	Charge pump up 50µA
4	d	1	0	F_{COMP} to P2; $F_{PD}/2$ to P3; Lock output switched to out of lock condition
5	d	1	1	Lock output switched to inlock condition

These test modes are invoked by taking the clock input below V_{EE}
d=don't care

Table 2 Test mode options

MODE	COMPATIBILITY	
	18 Bit Data entry	19 Bit Data entry
4	TD6380 plus ÷2 prescaler	TD6382 plus ÷4 prescaler
3	None	TD6381
2	TD6380	TD6382 plus ÷2 prescaler
1	None	TD6382
0	None	TD6381 plus ÷2 prescaler

Table 3. Programming compatibilities

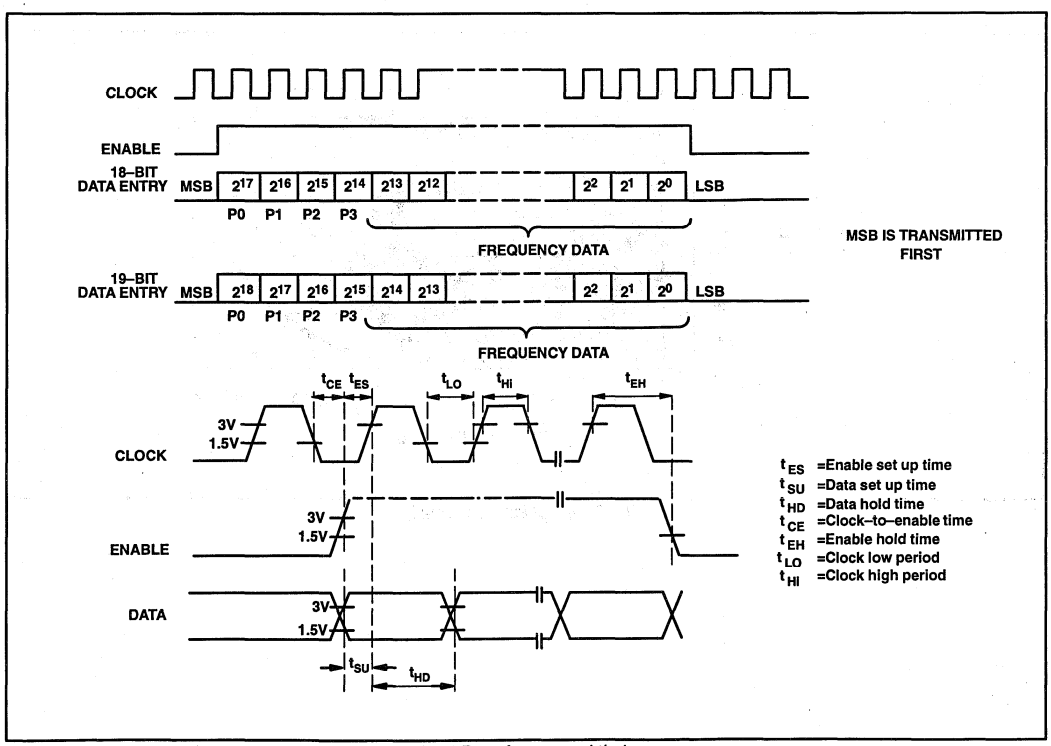


Fig. 4 Data format and timing

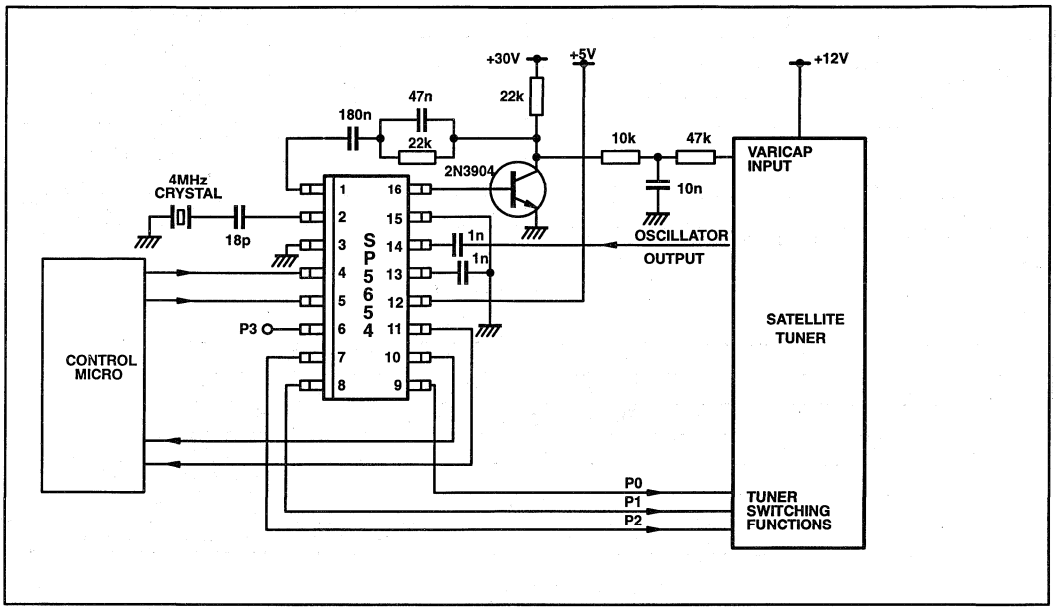


Fig. 5 Typical application (step size = 100kHz)

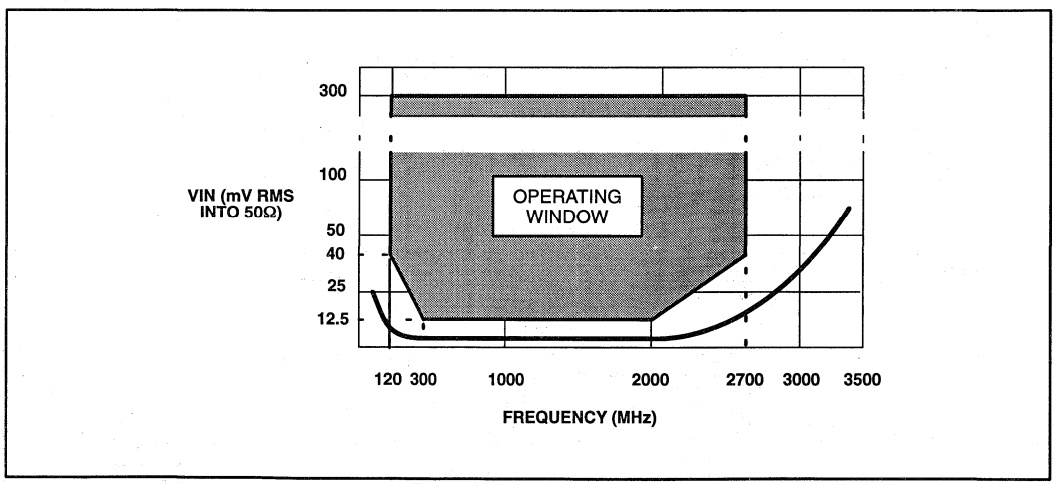
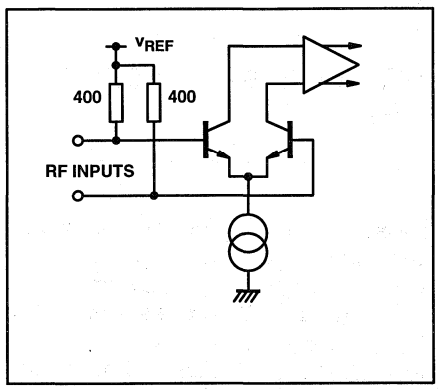
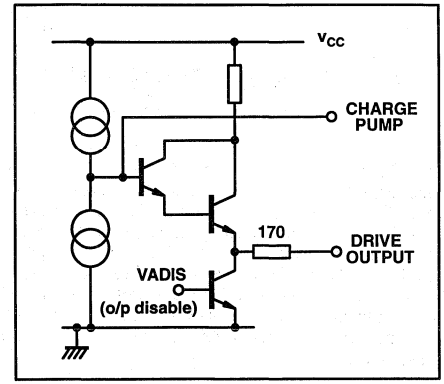


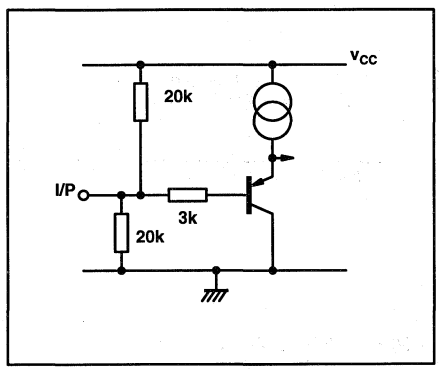
Fig. 6 Typical input sensitivity



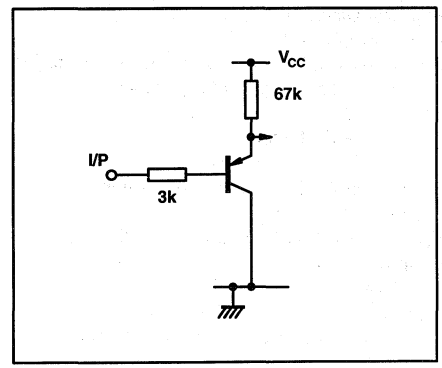
RF inputs



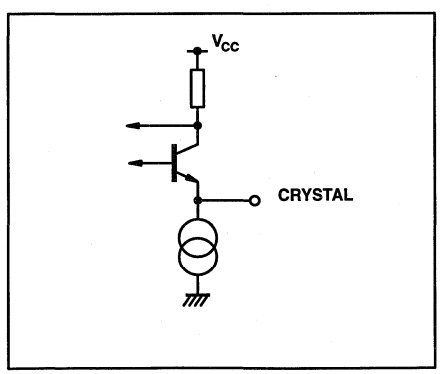
Loop amplifier



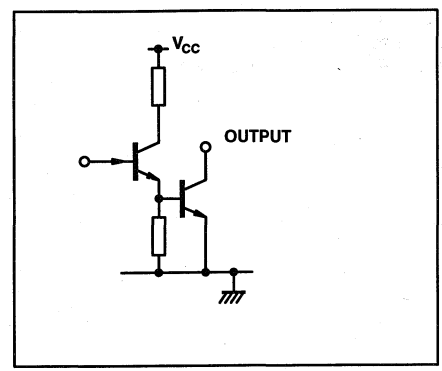
Mode select input



Data, Clock, Enable inputs



Reference oscillator



Output ports P0–P3 and lock output

Fig. 7. Input/Output interface circuits

SP5655

2.7GHz BI–DIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

(Supersedes edition in 1995 Media IC Handbook)

The SP5655 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 2 addressable current limited outputs and 4 addressable bi–directional open collector ports one of which is a 3 bit ADC. The information on these ports can be read via the I²C BUS. The device has one fixed I²C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables 2 or more synthesisers to be used in a system.

FEATURES

- Complete 2.7GHz Single chip System
- High Sensitivity RF Inputs
- Programmable via I²C Bus
- On Chip oscillator with 1kΩ negative resistance
- Low power consumption (5V 30mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 6 Controllable Outputs, 4 Bi–Directional
- 5 Level ADC
- Variable I²C BUS Address For Multi Tuner Applications
- ESD Protection *
- Switchable ÷512/1024 Reference Divider
- Pin and Function Compatible with SP5055S †

* Normal ESD handling procedures should be observed.

† The SP5055S does not have a switchable reference division ratio.

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

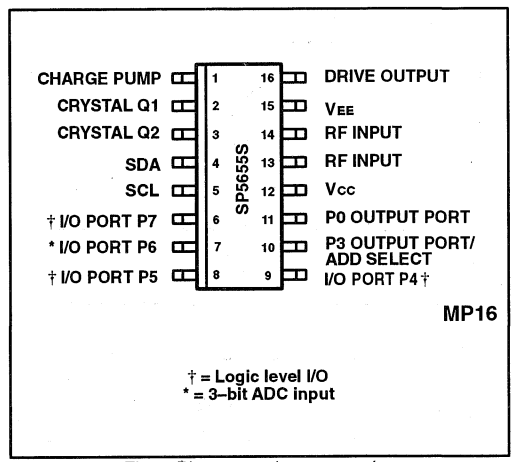


Fig. 1 Pin connections – top view

ORDERING INFORMATION

SP5655S/KG/MPAS (Tubes)
SP5655S/KG/MPAD (Tape and Reel)

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +80°C, V_{CC}= +4.5V to +5.5V. Reference frequency = 4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	12		30	40	mA	V_{CC} = 4.5V to 5.5V
Prescaler Input Voltage	13, 14	50		300	mV_{RMS}	120MHz to 2.7GHz sinewave See Fig. 5.
Prescaler Input Impedance Input Capacitance	13, 14		50 2		Ω pF	
SDA, SCL Input High Voltage Input Low Voltage Input High Current Input Low Current Leakage Current	4, 5 4, 5 4, 5 4, 5 4, 5	3 0		5.5 1.5 10 –10 10	V V µA µA µA	 Input Voltage = V_{CC} Input Voltage = 0V When V_{CC} = 0V
SDA Output Voltage	4			0.4	V	I_{sink} = 3mA
Charge Pump Current Low	1		±50		µA	Byte 4 Bit 2 = 0, Pin 1 = 2V
Charge Pump Current High	1		±170		µA	Byte 4 Bit 2 = 1, Pin 1 = 2V
Charge Pump Output Leakage Current	1			±5	nA	Byte 4 Bit 4 = 1, Pin 1 = 2V
Charge Pump Drive Output Current	16	500			µA	$V_{pin\ 16}$ = 0.7V
Charge Pump Amplifier Gain			6400			
Recommended Crystal series Resistance		10		200	Ω	"Parallel Resonant" crystal. Resistance specified is max under all conditions
Crystal Oscillator Drive Level			80		mVp–p	
Crystal Oscillator Negative Resistance	2	750	1000		Ω	
External Reference Input Frequency	2	2		8	MHz	AC coupled sinewave
External Reference Input amplitude	2	70		200	mVrms	AC coupled sinewave
Output Ports						
P0–P3 Sink Current	11 – 10	0.7	1	1.5	mA	V_{out} = 12V
P0–P3 Leakage Current	11 – 10			10	µA	V_{out} = 13.2V
P4–P7 Sink Current	9–6	10			mA	V_{out} = 0.7V
P4–P7 Leakage Current	9–6			10	µA	V_{out} = 13.2V
Input Ports						
P3 Input Current High	10			+10	µA	$V_{pin\ 10}$ = 13.2V
P3 Input Current Low	10			–10	µA	$V_{pin\ 10}$ = 0V
P4,P5,P7 Input Voltage Low	9,8,6			0.8	V	
P4,P5,P7 Input Voltage High	9,8,6	2.7			V	
P6 Input Current High	7			+10	µA	See Table 3 for ADC Levels
P6 Input Current Low	7			–10	µA	

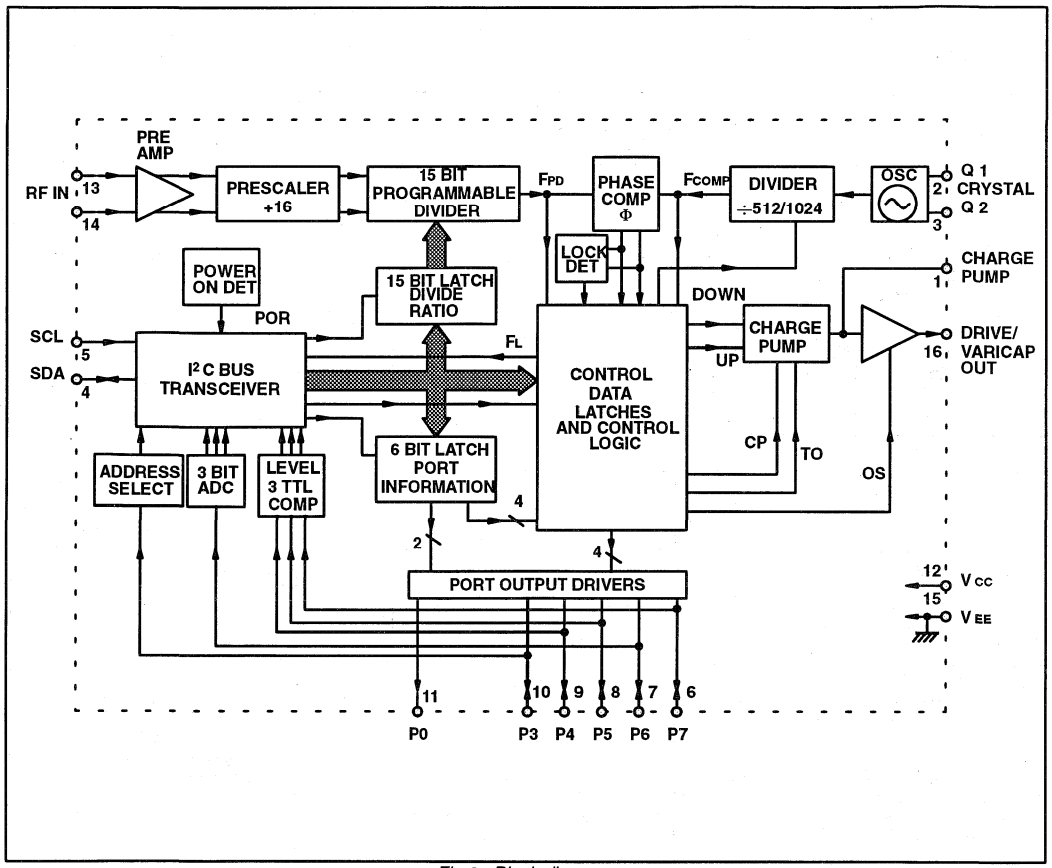


Fig 2. Block diagram

FUNCTIONAL DESCRIPTION

The SP5655 is programmed from an I²C Bus. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low and read mode if it is high. The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C Bus system. Table 4 shows how the address is selected by applying a voltage to P3. When the device receives a correct address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are programmed. When the device is programmed into the read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

WRITE MODE (Frequency Synthesis)

When the device is in write mode bytes 2+3 select the synthesised frequency, while bytes 4+5 control the output port states, charge pump, reference divider ratio and various test modes.

Once the correct address is received and acknowledged, the first bit of the next byte determines whether that byte is interpreted as byte 2 or 4; a logic 0 for frequency information and a logic 1 for control and output port information. When byte 2 is received the device always expects byte 3 next. Similarly, when byte 4 is received the device expects byte 5 next. Additional data bytes can be entered without the need to re–address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid–byte (e.g. by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 is stored in a 15–bit register and is used to control the division ratio of the 15–bit programmable divider. This is preceded by a divide–by–16 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is shown in Fig. 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 16 times the comparison frequency F_{COMP}.

When frequency data is entered, the phase comparator, via a charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phased locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2, or provided by an on–board crystal controlled oscillator. The comparison frequency F_{COMP} is derived from the reference frequency via the reference divider. The reference divider division ratio is switchable from 512 to 1024, and is controlled by bit 7 of byte 4 (TS0); a logic 1 for 512; a logic 0 for 1024. The SP5655 differs from the SP5055 in this respect, only 512 being available on the SP5055. Note, the comparison frequency is 7.8125kHz when a 4MHz reference is used, and divide by 512 is selected.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for $\pm 170\mu A$ and a logic 0 for $\pm 50\mu A$ allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. When the device is 'frequency locked' the charge pump current is internally set to $\pm 50\mu A$ regardless of CP.

Bit 4 of byte 4 (T0) disables the charge pump when it is set to a logic 1.

Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1.

Bit 3 of byte 4 (T1) enables various test modes when set high. These modes are selected by bits 5, 6, 7 of byte 4 (TS2, TS1, TS0) as detailed in Table 5. When T1 is set low, TS2, TS1 are assigned a 'don't care' condition, and TS0 selects the reference divider ratio as previously described.

Byte 5 programs the output ports P0, P3 to P7; a logic 0 for a high impedance output and a logic 1 for low impedance (on).

READ MODE

When the device is in read mode the status byte read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power–on reset indicator and is set to a logic 1 if the V_{CC} supply to the device has dropped below 3V (at 25°C), e.g. when the device is initially turned on. The POR is reset to 0 when the read sequence is terminated by a stop command. When POR is set high (at low V_{CC}), the programmed information is lost and the output ports are all set to high impedance.

Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked, and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels.

Bits 6, 7 and 8 (A2, A1, A0) combine to give the output of the 5 level ADC. The ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6. The SP5655 is function and pin equivalent to the SP5055 device apart from the switchable reference divider, and has much lower power dissipation, improved RF sensitivity and better ESD performance.

MSB								LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	Byte 1
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	Byte 2
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	Byte 3
CONTROL DATA	1	CP	T1	T0	TS2	TS1	TS0	OS	A	Byte 4
IO PORT CONTROL DATA	P7	P6	P5	P4	P3	X	X	P0	A	Byte 5

Table 1 Write data format (MSB is transmitted first)

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	Byte 1
STATUS BYTE	POR	FL	I2	I1	I0	A2	A1	A0	A	Byte 2

Table 2 Read data format (MSB is transmitted first)

A:	Acknowledge bit
MA1, MA0:	Variable address bits (see Table 4)
CP:	Charge pump current select
T1:	Test mode enable
T0:	Charge pump disable
TS2, TS1, TS0:	Operation mode control bits (see Table 5)
OS:	Varactor drive Output disable Switch
P7,P6,P5,P4,P3,P0:	Control output states
POR:	Power On Reset indicator
FL:	Phase Lock detect Flag
I2, I1, I0:	Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0:	5 Level ADC data from P6 (see Table 3)
X:	Don't care

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0.45V_{CC}$ to $0.6V_{CC}$
0	1	0	$0.3V_{CC}$ to $0.45V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.3V_{CC}$
0	0	0	0 to $0.15V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	$0 - 0.2V_{CC}$
0	1	ALWAYS VALID
1	0	$0.3V_{CC} - 0.7V_{CC}$
1	1	$0.8V_{CC}$ – 13.2V

Table 4 Address selection

T1	TS2	TS1	TS0	OPERATION MODE DESCRIPTION
0	X	X	0	Normal operation, test modes disabled, reference divider ratio=1024
0	X	X	1	Normal operation, test modes disabled, reference divider ratio=512
1	0	0	X	Charge pump source (down). Status byte bit FL set to 0
1	0	1	X	Charge pump sink (up). Status byte bit FL set to 1
1	1	0	0	Ports P4,P5,P6,P7 set to state X
1	1	0	1	Port P7=$F_{PD}/2$; P4,P5,P6 set to state X
1	1	1	X	Port P7=F_{PD}; P6=F_{COMP}; P4, P5 set to state X

X=don't care

(For further details of test modes see Table 6).

Table 5 Operation modes

Fig. 3 Data formats

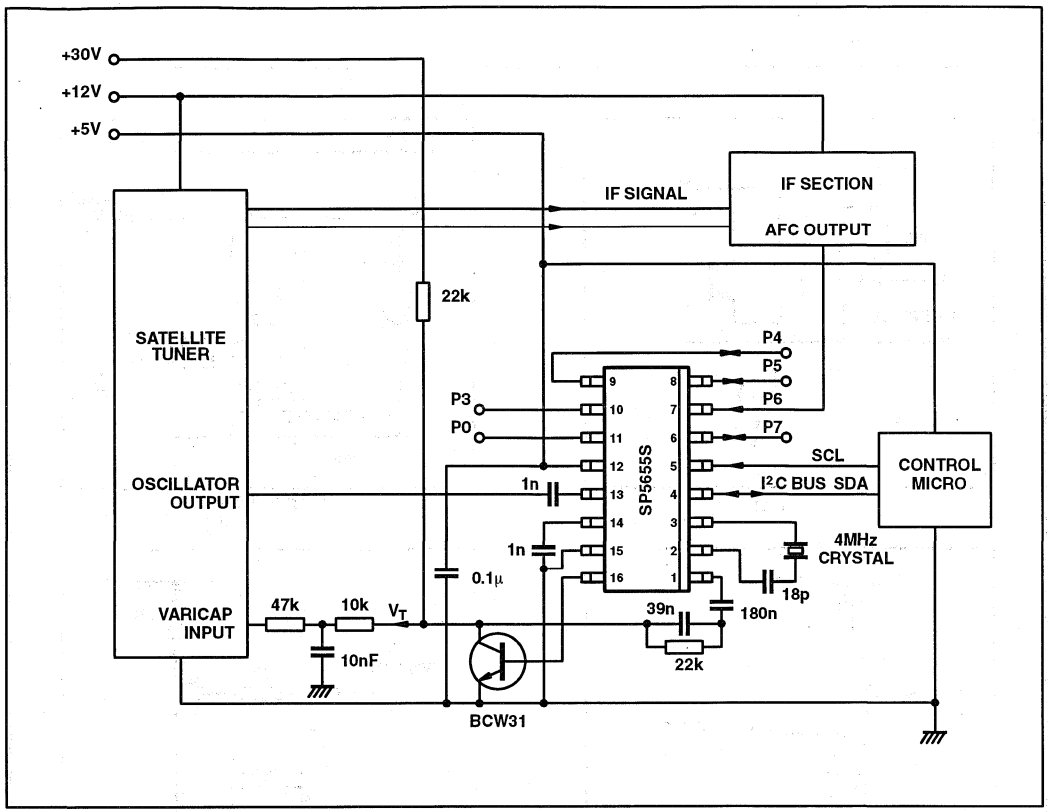


Fig. 4 Typical application

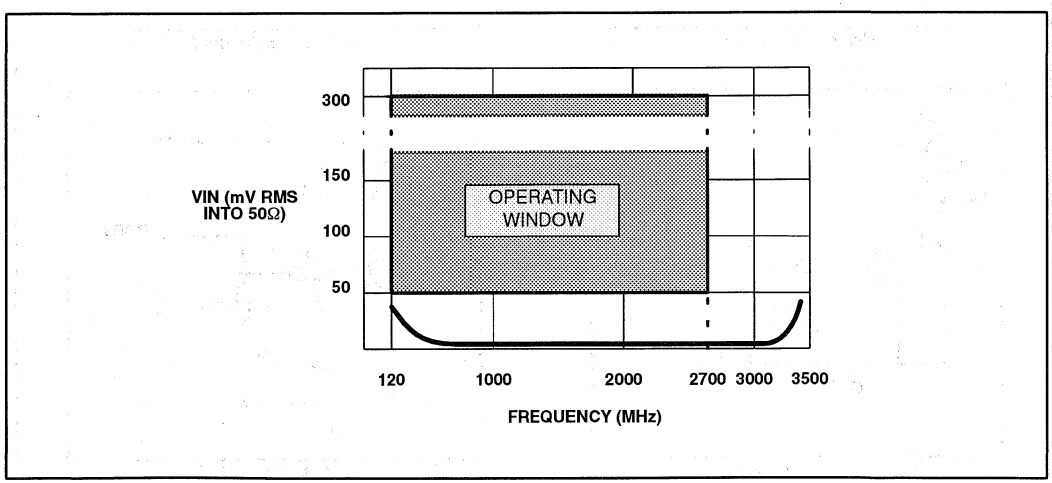


Fig. 5 Typical input sensitivity

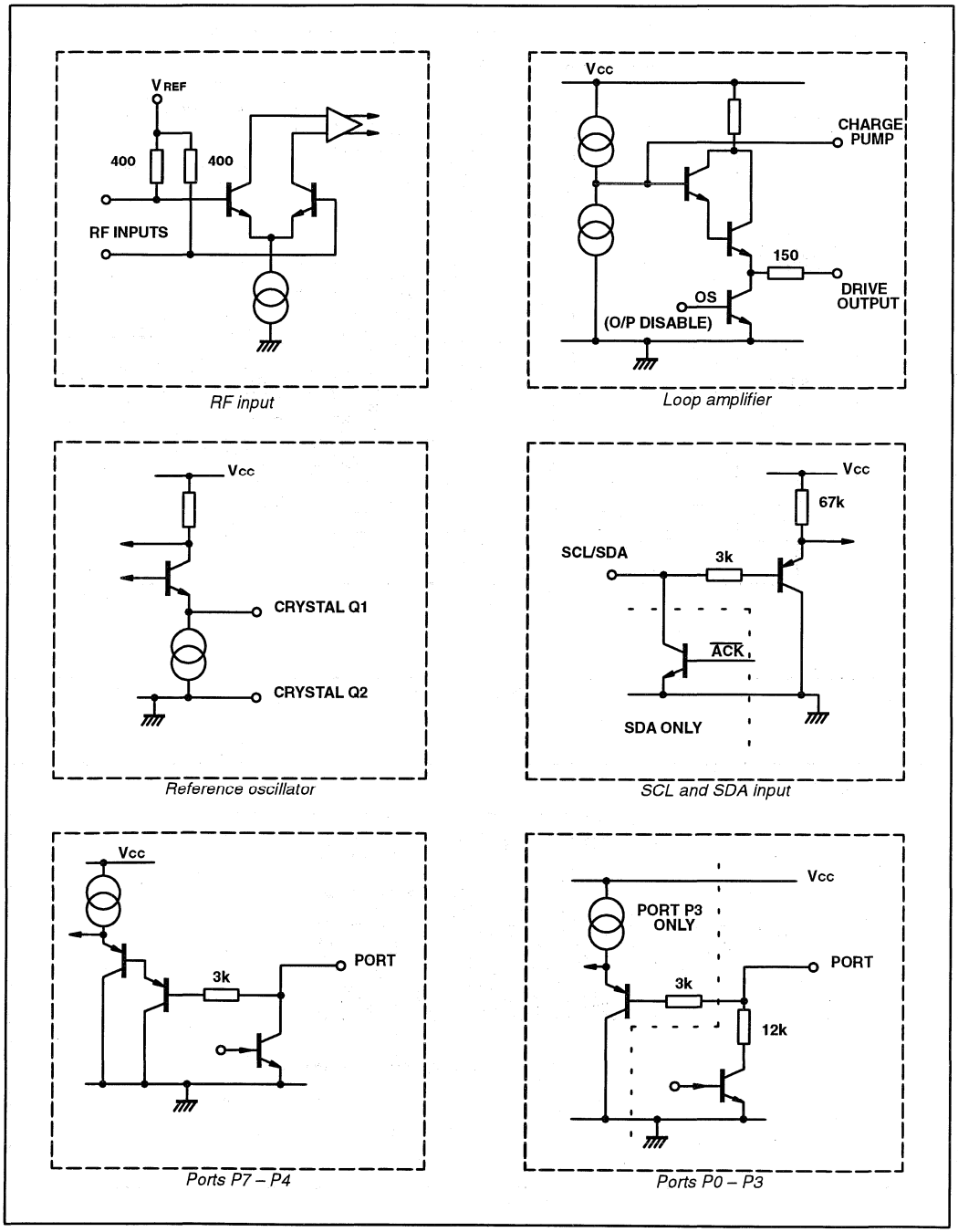


Fig. 6 Input/output interface circuits

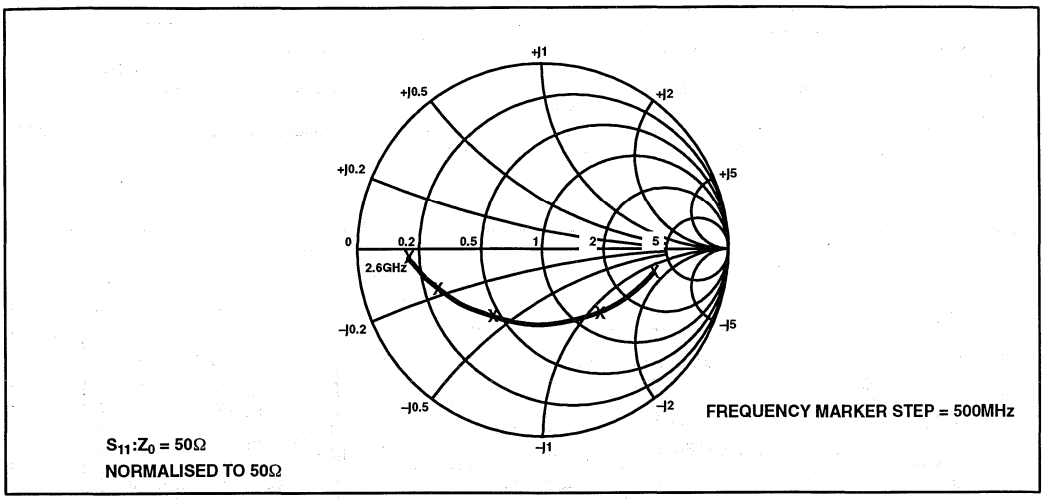


Fig. 7 Typical input impedance

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V.

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Supply voltage	12	– 0.3	7	V	
RF input voltage	13, 14		2.5	Vp–p	
Port voltage	6–11 6–9 10, 11	– 0.3 – 0.3 – 0.3	14 6 14	V V V	Port in off state Port in on state Port in on state
Total port output current	6–11		50	mA	
RF input DC offset	13, 14	– 0.3	V_{CC} +0.3	V	
Charge Pump DC offset	1	– 0.3	V_{CC}+0.3	V	
Drive DC offset	16	– 0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	– 0.3	V_{CC}+0.3	V	
SDA,SCL input voltage	4, 5	– 0.3	6	V	
Storage temperature		– 55	+150	°C	
Junction temperature			+150	°C	
MP16 thermal resistance, chip–to–ambient			111	°C/W	
MP16 thermal resistance, chip–to–case			41	°C/W	
Power consumption at 5.5V			220	mW	All ports off
ESD protection	ALL	4		kV	MIL STD 883C TM 3015

APPLICATION NOTES

A generic set of application notes AN168 for designing with synthesisers such as the SP5655 has been written. This covers aspects such as loop filter design, decoupling and I^2C bus radiation problems.

This application note is featured in the Media October 1995 IC Handbook. A generic test/demo board has been produced which can be used for the SP5655. A circuit diagram and layout for the board is shown in Figs. 8 and 9.

The board can be used for the following purposes:

(A) Measuring RF sensitivity performance.
(B) Indicating port function.
(C) Synthesising a voltage controlled oscillator.
(D) Testing of external reference sources.

The programming codes relevant to these tests are shown in Table 6.

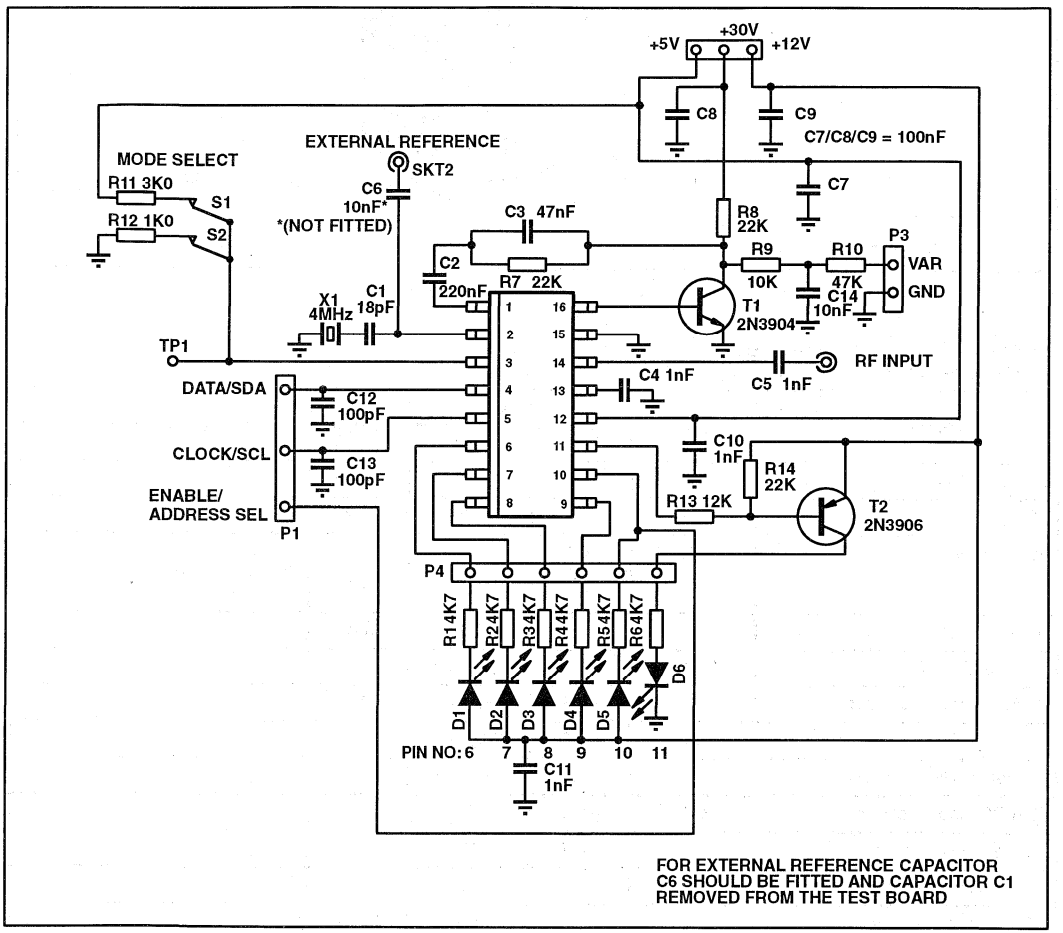
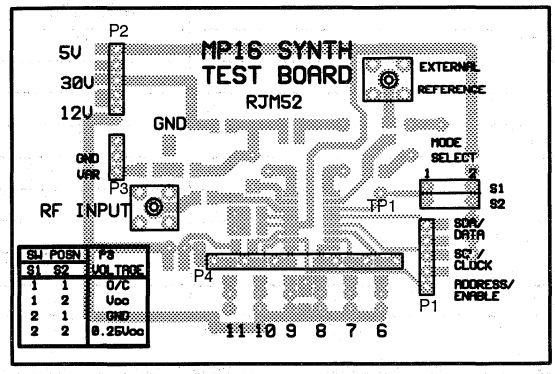
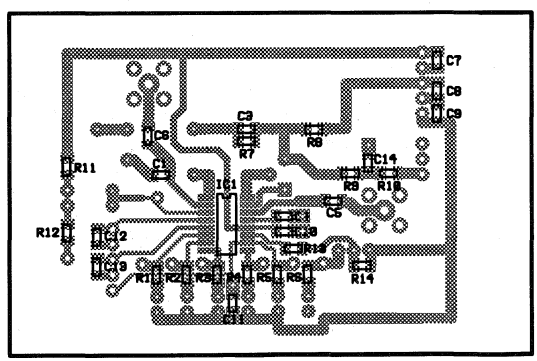


Fig. 8 Test board



TP1 = PIN 3 DC BIAS

Top view (Ground plane)



Underside (surface mount components side)

NOTES:
CIRCUIT SCHEMATIC IS SHOWN IN FIG. 8.

ALL SURFACE MOUNT COMPONENTS MOUNTED ON UNDERSIDE OF BOARD

Fig. 9 Test board (layout)

TEST MODES

As explained earlier in the data sheet, the device can be programmed into a number of test modes. These are invoked by programming the following HEX codes into Byte 4. The most commonly used codes are shown in Table 6

DESCRIPTION	HEX CODE (BYTE 4)	
	CP HI MODE	CP LO MODE
Normal operation, REF DIV =1024	CC	8C
Normal operation, REF DIV = 512	CE	8E
Charge Pump Source (Down), FL SET to 0	E2	A2
Charge Pump Sink (up), FL SET to 1	E6	A6
Port P7 = $F_{PD}/2$	EA	AA
Port P7 = F_{PD}; P6 = F_{COMP}	EE	AE
Charge Pump Disable, REF DIV ÷ 512	DE	9E
Varactor Line Disable, REF DIV ÷ 512	CF	8F
Charge Pump and Varactor Line Disable, REF DIV ÷ 512	DF	9F

Table 6 Useful test modes.

Other codes will also apply due to 'Don't Care' conditions, which are assumed to be 1 in the above Table.

NOTE:

When looking at F_{PD} or F_{COMP} signals from Ports P7 and P6, Byte 4 should be sent twice, firstly to set the desired reference divider ratio, (see Table 6) then secondly to switch on the chosen test mode.

The pulses can then be measured by simply connecting an oscilloscope or counter to the relevant output pin on the test board.

SP5657

2.7GHz 3–WIRE BUS CONTROLLED SYNTHESISER

The SP5657 is a single chip frequency synthesiser designed for satellite TV tuning systems. The device when used with a satellite TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide–by–16 prescaler with its own preamplifier and a 14–bit programmable divider controlled by a serially loaded data register. Four independently programmable open collector outputs are included. The device has eight modes of operation, selected by the 'div2 bypass' input, and bits R1, R0 of the programming data. These modes are summarised in Table 1.

The comparison frequencies are obtained from a crystal controlled on–chip oscillator typically operating at 4MHz. The comparator has a charge pump output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

FEATURES

- Complete 2.7GHz Single Chip System
- High Sensitivity RF Inputs
- Low Power Consumption (5V 30mA)
- On chip oscillator with 1kΩ negative resistance
- On chip oscillator start–up circuit
- Programming Compatible with Sanyo LC7215, LC7215F, LC7215FM plus ÷128/256 prescaler #
- Pin Compatible with SP5054
- 8 Modes of operation with different step sizes, see Table 1
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- Charge Pump Disable
- Single Port 20–Bit Serial Data Entry
- Four Controllable Outputs
- ESD Protection †

See notes on programming compatibility

†Normal ESD handling procedures should be observed

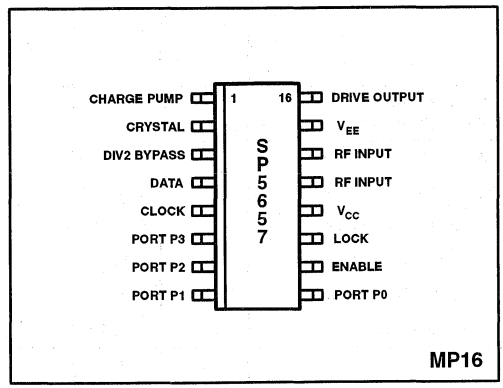


Fig. 1 Pin connections – top view

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems
- Combined Satellite and Terrestrial tuners

ORDERING INFORMATION

SP5657/KG/MPAS (Tubes)
SP5657/KG/MPAD (Tape & Reel)

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +80°C, V_{CC}=+4.5V to +5.5V. Reference frequency =4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	12		30	40	mA	Typical applies to V_{CC} = 5V
Prescaler Input Voltage		13, 14	12.5		300	mV_{rms}	300MHz to 2GHz sinewave.
			40		300	mV_{rms}	120MHz & 2.7GHz See Fig. 6
Prescaler Input Impedance Input Capacitance		13, 14		50 2		Ω pF	
Data Clock and Enable							
High Level Input Voltage		4, 5, 10	3		V_{CC}	V	
Low Level Input Voltage		4, 5, 10	0		1.5	V	
High Level Input Current		4, 5, 10			10	µA	V_{IN}=5.5V V_{CC}=5.5V
Low Level Input Current		4, 5, 10			–10	µA	V_{IN}=0V V_{CC}=5.5V
Input Hysteresis		4, 5, 10		0.8		V	
Clock Rate		5			500	kHz	
Timing Information							
Data Setup Time	t_{SU}	4	300			ns	See Fig.4
Data Hold Time	t_{HD}	4	600			ns	See Fig. 4
Enable Setup time	t_{ES}	10	300			ns	See Fig. 4
Enable Hold Time	t_{EH}	10	600			ns	See Fig. 4
Clock–to–Enable Time	t_{CE}	10	300			ns	See Fig. 4
Clock Low Period	t_{LO}	5	600			ns	See Fig. 4
Clock High Period	t_{HI}	5	600			ns	See Fig. 4
Div2 Bypass							
High Level Input Voltage		3	3		V_{CC}	V	
Low Level Input Voltage		3	0		1.5	V	
High Level Input Current		3			300	µA	V_{IN}=5.5V V_{CC}=5.5V
Low Level Input Current		3			–10	µA	V_{IN}=0V V_{CC}=5.5V
Charge Pump Output Current		1		±150		µA	V pin 1 = 2.0V device 'out of lock
Charge Pump Output Current		1		±50		µA	V pin 1=2.0V, device 'locked'
Charge Pump Output Leakage Current		1			±5	nA	V pin 1 = 2.0V, charge pump disabled
Charge Pump Drive Output Current		16	1			mA	V pin 16 = 0.7V
Charge Pump Amplifier Gain				6400			Pin 18 Current = 100µA
Oscillator Temperature Stability					2	ppm/°C	
Oscillator Stability with Supply Voltage					2	ppm/V	
Recommended Crystal Series Resistance			10		200	Ω	"Parallel resonant crystal." Figure quoted is under all conditions including start up.
Crystal Oscillator Drive Level		2		80		mV p–p	

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +80°C, V_{CC}=+4.5V to +5.5V. Reference frequency =4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Crystal Oscillator negative resistance		2	750			Ω	Includes temperature and process tolerances
Reference Crystal Frequency		2	4		8	MHz	
External Reference input Frequency		2	2		16	MHz	AC coupled sinewave
External Reference input Amplitude		2	400		1000	mV_{p-p}	AC coupled sinewave
Comparison Frequency (at phase detector)					160	kHz	
Ports and Lock output							
Sink Current		6–9, 11	10			mA	V_{out}=0.7V
Lock Leakage Current		11			10	µA	$V_{out}=V_{CC}$
Port Leakage Current		6–9			10	µA	V_{out}=13.2V
Varactor Drive Amp Disable		10	–50			µA	V_{pin} 10 < 0V. Current sourced from device
Charge Pump Disable		4	–50			µA	V_{pin} 4 < 0V. Current sourced from device
Test Mode Enable		5	–50			µA	V_{pin} 5 < 0V. Current sourced from device. See Table 2

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE}=0V

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Supply voltage	12	–0.3	7	V	
Prescaler input voltage	13, 14		2.5	Vp–p	
Prescaler DC offset	13, 14	–0.3	V_{CC}+0.3	V	
Port voltage	6–9	–0.3	14	V	Port in off state
		–0.3	6	V	Port in on state
Total port output current	6–9		50	mA	
Loop amplifier DC offset	1, 16	–0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	–0.3	V_{CC}+0.3	V	
3–wire bus inputs	4, 5, 10	–0.7	6	V	
Div2 bypass input	3	–0.3	V_{CC}+0.3	V	
Lock output voltage	11	–0.3	V_{CC}+0.3	V	
Lock output current	11		15	mA	
Storage temperature		–55	+150	°C	
Junction temperature			+150	°C	
MP16 thermal resistance, chip–to–ambient			111	°C/W	
MP16 thermal resistance, chip–to–case			41	°C/W	

ABSOLUTE MAXIMUM RATINGS (cont.)

All voltages are referred to V_{EE}=0V

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Power consumption			220	mW	All ports off
ESD protection	All	4		kV	MIL STD 883 TM 3015

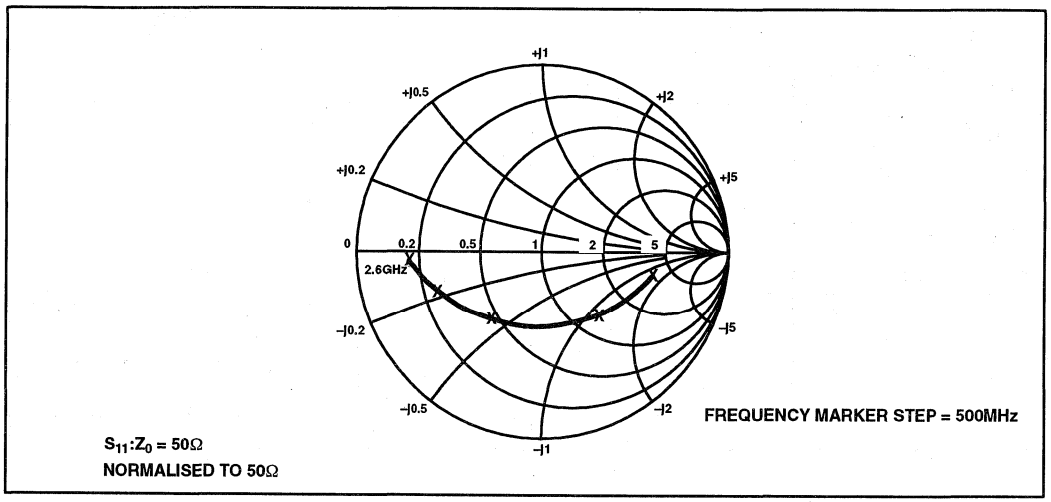


Fig. 2 Typical input impedance

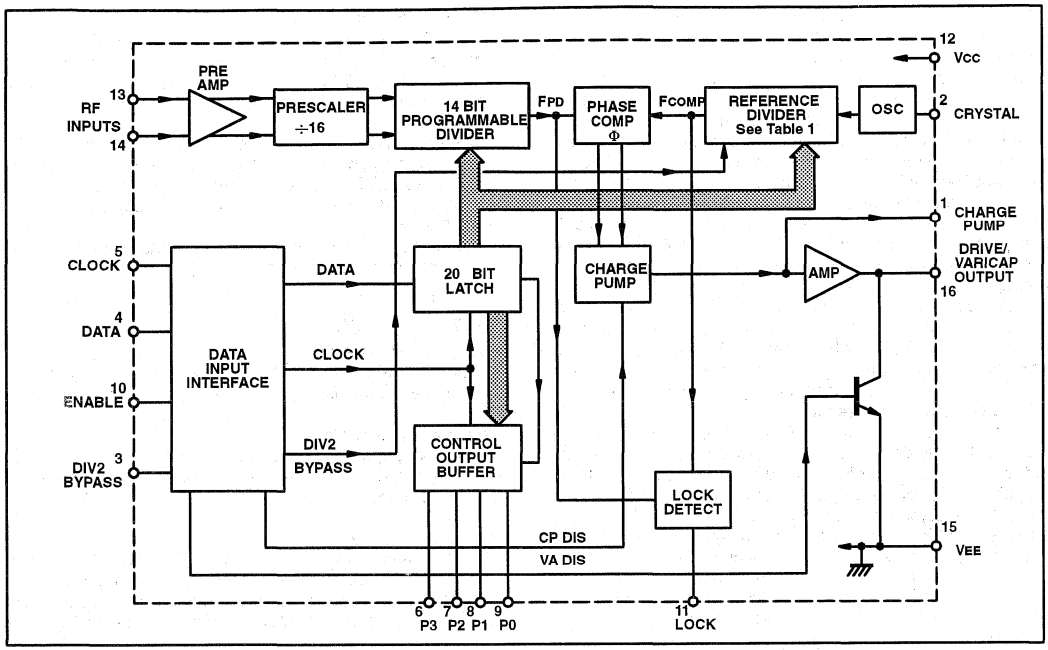


Fig. 3 Block diagram

FUNCTIONAL DESCRIPTION

The SP5657 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor, to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard data, clock and enable three–wire bus. The data load consists of a single word, which contains frequency, reference ratio and port information, and is only transferred to the internal data shift register during an enable high period. The clock is disabled during low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable, so giving improved fine tuning facility for digital AFC etc.

The frequency is set by first selecting the required mode of operation as detailed in Table 1, and then by loading the programmable divider with the required 14–bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator where it is compared in phase and frequency to the internally generated comparison frequency, F_{COMP}.

The comparison frequency F_{COMP} is obtained by dividing the output of the on–chip crystal controlled oscillator. The ratio of the reference divider is selected by the 'div2 bypass' input and bits R1, R0 of the programming data word as detailed in Table 1. The crystal frequency generally used is 4MHz, giving an F_{COMP} of 8kHz in mode 2, which when multiplied back up to the LO gives a minimum step size of 128kHz.

The programmable divider is preceded by an input RF preamplifier and high speed low radiation prescaler. The preamplifier is arranged to be self oscillating, so giving excellent input sensitivity. The input impedance and sensitivity are shown in Fig. 2 and 6 respectively.

The charge contains a lock detect circuit which generates a flag when the loop has attained lock. The 'out of lock' condition is indicated by a high impedance state.

The charge pump current is initially set to ±150μA. When the device attains frequency lock, the charge pump current is switched to ±50μA, so improving the local oscillator short term jitter.

The device also contains four general purpose open collector output ports P0–P3. These outputs are each capable of sinking at least 10mA, when the appropriate bits P0–P3 of the programming data, see Fig. 4 are set to a logic '1'.

PROGRAMMING COMPATIBILITY

With the 'div2 bypass' input low, modes 1–3, the SP5657 is programming and frequency step size compatible with the Sanyo LC7215/LC7215F/LC7215FM device combined with a ÷128 prescaler and gives step sizes of 1280kHz, 128kHz and 640kHz.

With the 'div2 bypass' input high, modes 5–7, the SP5657 is programming and frequency step size compatible with the Sanyo LC7215/LC7215F/LC7215FM device combined with a ÷256 prescaler and gives step sizes of 2560kHz, 256kHz and1280kHz.

For modes 0 and 4, programming compatibility, but not step size compatibility, is retained.

TEST FEATURES

Charge pump disable

The charge pump may be disabled by sourcing current from the data input, i.e. by forcing a negative input voltage.

Varactor line disable

The charge pump amplifier drive output may be disabled by sourcing current from the enable input, i.e. by forcing a negative voltage.

Device test mode

Further test modes can be invoked by sourcing current from the clock input, i.e. by forcing a negative input voltage. These test modes when invoked are determined by the data held in the P1, P2 and P3 internal registers as detailed in Table 2.

MODE	DIV2 BYPASS INPUT (ACTIVE HIGH)	R0	R1	REFERENCE DIVIDER RATIO	LO FREQUENCY STEP SIZE (kHz)*	*MAX OPERATING FREQUENCY (GHz)
0	LOW	0	0	280	228.57	2.7
1	LOW	0	1	50	1280	2.7
2	LOW	1	0	500	128	2.0970
3	LOW	1	1	100	640	2.7
4	HIGH	0	0	140	457.14	2.7
5	HIGH	0	1	25	2560	2.7
6	HIGH	1	0	250	256	2.7
7	HIGH	1	1	50	1280	2.7

*When used with a 4MHz crystal

Table 1. Modes of operation

Test Mode	P1	P2	P3	Test Mode Description
0	0	0	0	Charge pump down 170μA
1	0	0	1	Charge pump up 170μA
2	1	0	0	Charge pump down 50μA
3	1	0	1	Charge pump up 50μA
4	d	1	0	F_{COMP} to P2; $F_{PD}/2$ to P3; Lock output switched to out of lock condition
5	d	1	1	Lock output switched to inlock condition

These test modes are invoked by taking the clock input below V_{EE}.
d=don't care

Table 2 Test mode options

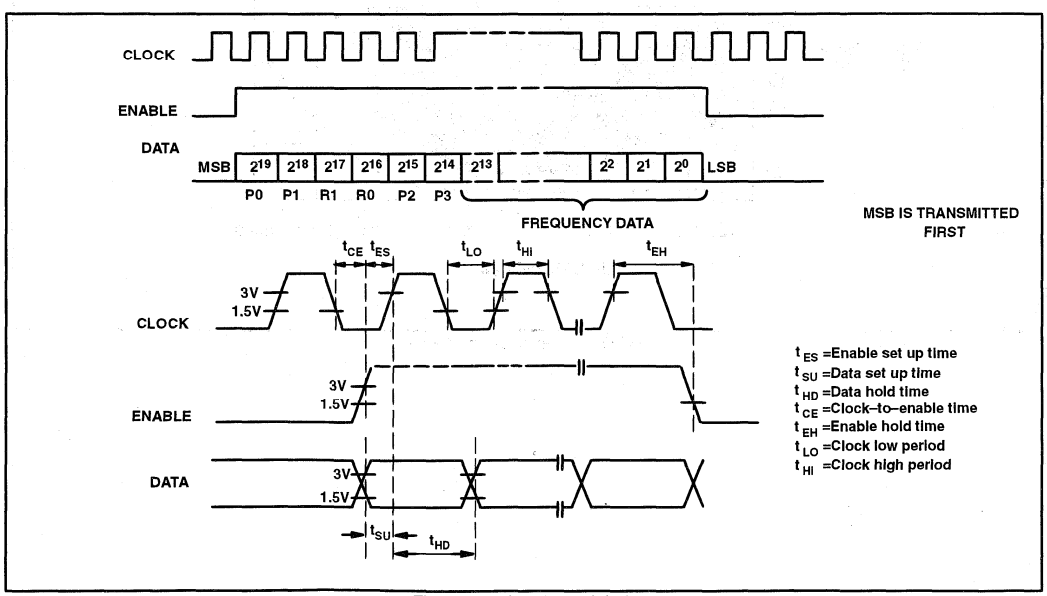


Fig. 4 Data format and timing

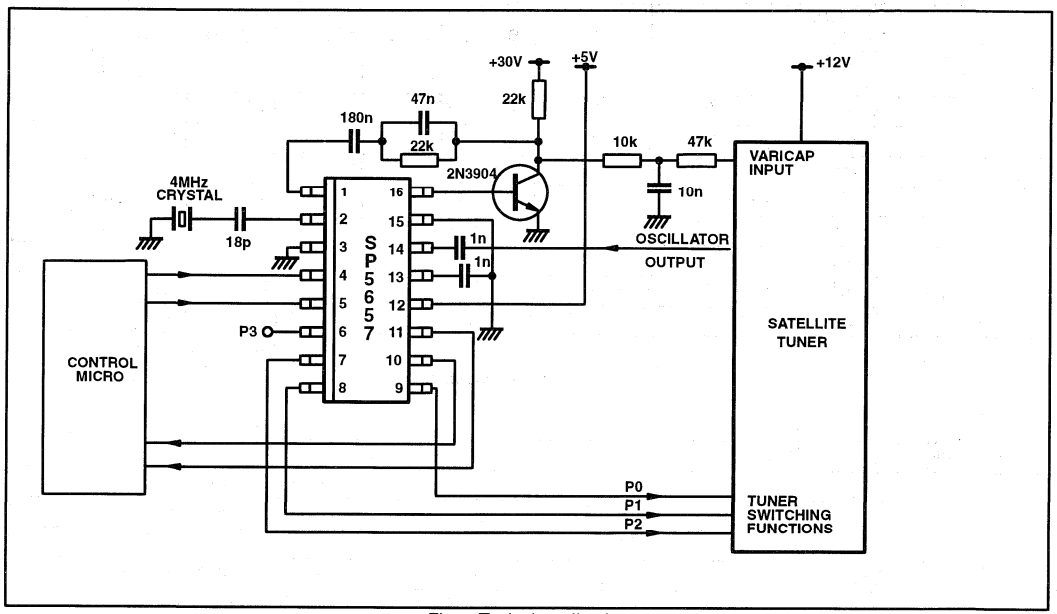


Fig. 5 Typical application

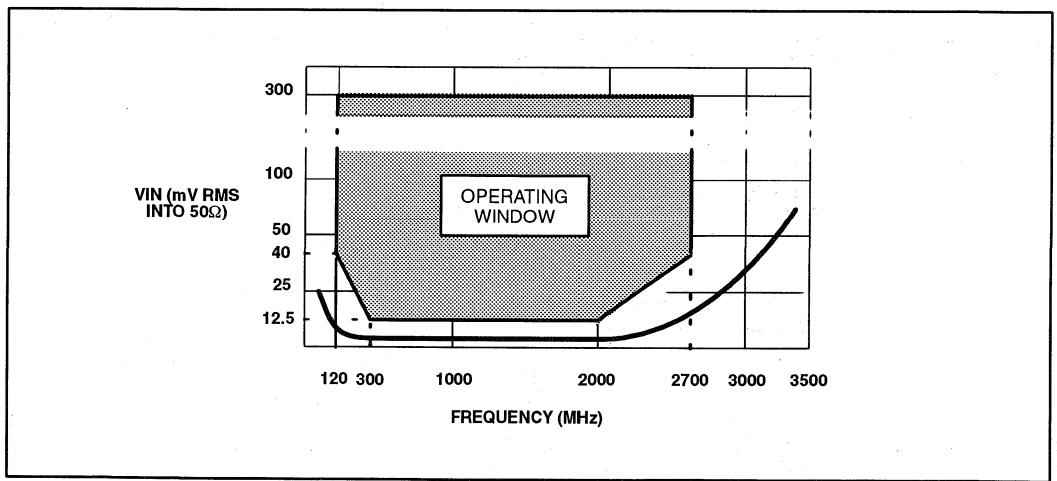
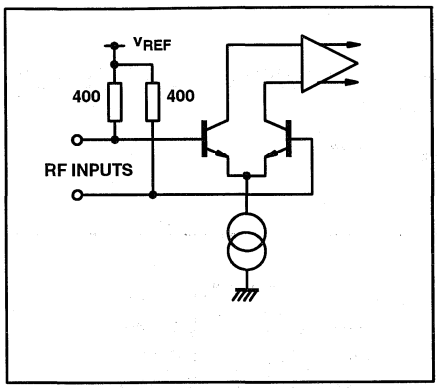
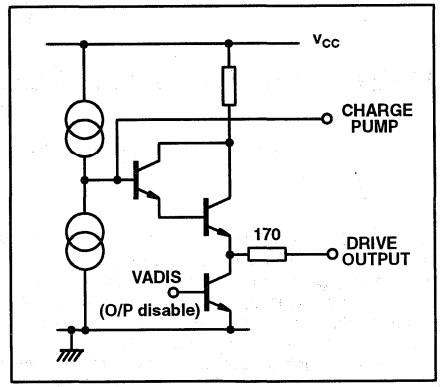


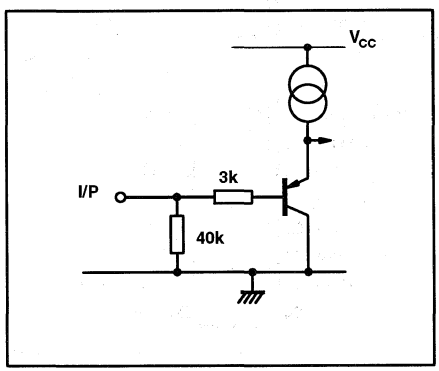
Fig. 6 Typical input sensitivity



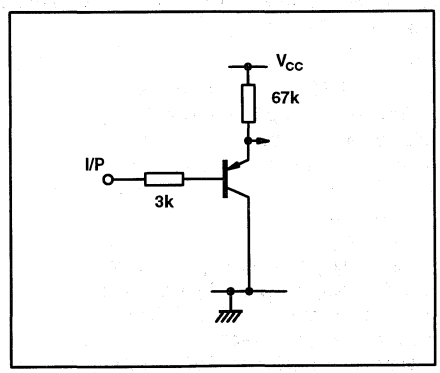
RF inputs



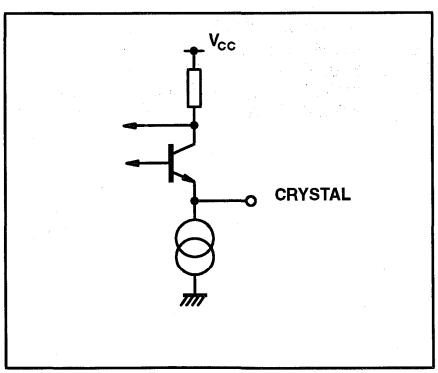
Loop amplifier



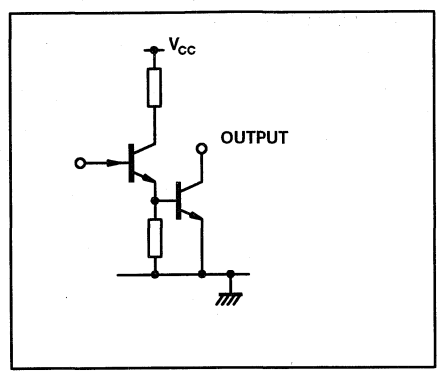
Div2 bypass input



Data, Clock, Enable inputs



Reference oscillator



Output ports P0–P3 and lock output

Fig. 7. Input/Output interface circuits

SP5658

2.7GHz 3–WIRE BUS CONTROLLED LOW PHASE NOISE FREQUENCY SYNTHESISER

(Supersedes version in October 1995 Media IC Handbook, HB3120–3)

The SP5658 is a single chip frequency synthesiser designed for tuning systems up to 2.7GHz.

The RF preamplifer contains a divide by two prescaler which can be disabled for applications up to 2GHz so enabling a step size equal to the comparison frequency up to 2GHz and twice the comparison frequency up to 2.7GHz.

Comparison frequencies are obtained either from a crystal controlled on–chip oscillator or from an external source.

The device contains two switching ports, in the 14 pin version and four in the 16 pin, together with an "in–lock" flag output. The device also contains a varactor line disable and charge pump disable facility.

FEATURES

- Complete 2.7GHz single chip system
- Optimised for low phase noise
- Selectable divide by two prescaler
- Selectable reference division ratio
- Charge pump disable
- Varactor line disable
- 'In–lock' flag
- Two switching ports in 14 pin version
- Four switching ports in 16 pin version
- Pin compatible with SP5659 I²C bus low phase noise synthesiser
- ESD protection (Normal ESD handling procedures should be observed)

APPLICATIONS

- SAT, TV, VCR and Cable tuning systems
- Communications systems

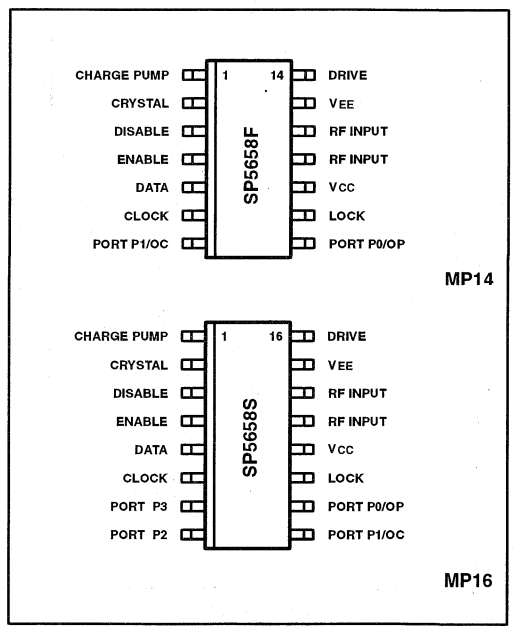


Fig. 1 Pin connections – top view

ORDERING INFORMATION

SP5658F/KG/MP1S (Tubes, 14 lead SO)
SP5658S/KG/MP2S (Tubes, 16 lead SO)
SP5658F/KG/MP1T (Tape and Reel)
SP5658S/KG/MP2T (Tape and Reel)

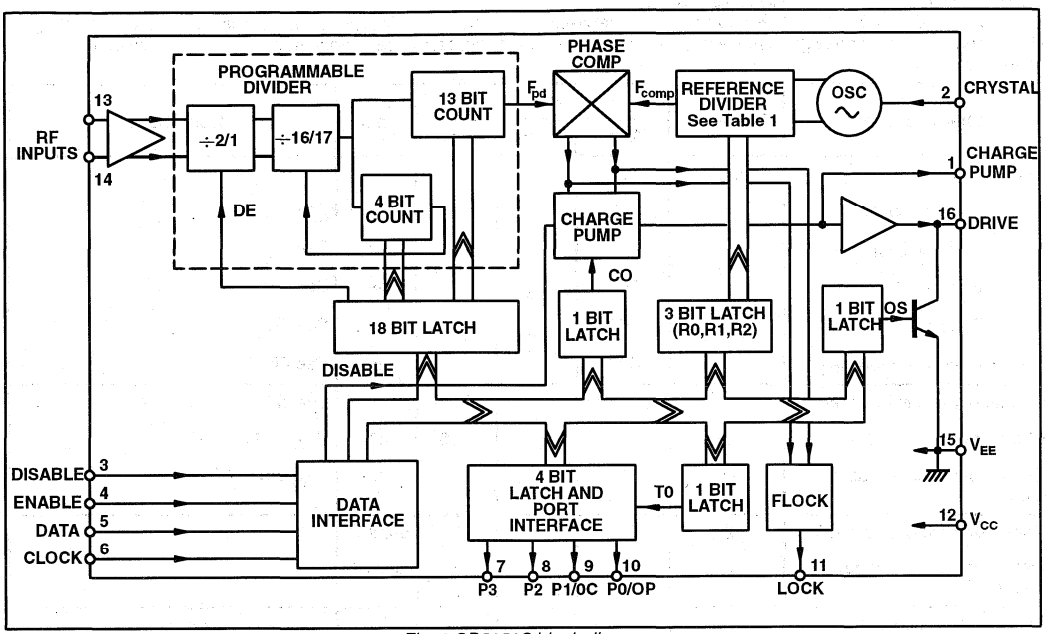


Fig. 2 SP5658S block diagram

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +80°C, V_{CC}= +4.5V to +5.5V. Reference frequency = 4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin (SP5658S)	Value			Units	Conditions
		Min	Typ	Max		
Supply current, I_{CC}	12		59	74	mA	V_{CC}=5V Prescaler enabled, DE=1
			52	65	mA	V_{CC}=5V Prescaler disabled, DE=0
RF input voltage	13, 14	40		300	mV_{rms}	300MHz to 2.7GHz Prescaler enabled, DE=1, See Fig. 5b
	13,14	100		300	mV_{rms}	100MHz Prescaler enabled, DE=1, See Fig. 5b.
	13, 14	40		300	mV_{rms}	100MHz to 2.0GHz Prescaler disabled, DE=0, See Fig. 5a
RF input impedance	13, 14		50		Ω	Refer to Fig. 4
RF input capacitance	13, 14	2			pF	Refer to Fig. 4
Data, Clock, Enable & Disable	3,4,5,6					
Input high voltage		3		V_{CC}	V	
Input low voltage		0		0.7	V	
Input high current				10	µA	Input voltage = V_{CC}
Input low current				–10	µA	Input voltage = V_{EE}
Clock Rate	6			500	kHz	
Clock data & enable input hysteresis	4,5,6		0.4		V	

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb}= –20°C to +80°C, V_{CC}=+4.5V to +5.5V. Reference frequency = 4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin (SP5658S)	Value			Units	Conditions
		Min	Typ	Max		
Bus Timing	4,5,6					
Data set up, t_{SU}		300			ns	See Fig. 3
Data hold, t_{HD}		600			ns	See Fig. 3
Enable set up, t_{ES}		300			ns	See Fig. 3
Enable hold, t_{EH}		600			ns	See Fig. 3
Clock to enable, t_{CE}		300			ns	See Fig. 3
Charge pump output current	1					See Table 3, V_{PIN1} = 2V
Charge pump output leakage	1		±3	±10	nA	V_{PIN1} = 2V
Charge pump drive output current	16	1			mA	V_{PIN16} = 0.7V
Oscillator temperature stability	2			2	ppm/°C	
Oscillator supply voltage stability	2			2	ppm/V	
External reference input frequency	2	2		20	MHz	AC coupled sinewave
External reference input amplitude	2	200		500	mV_{PP}	AC coupled sinewave
Crystal frequency	2	4		12	MHz	
Crystal oscillator drive level	2		45		mV_{PP}	
Recommended crystal series resistance		100		200	Ω	Applies to 4MHz crystal only. "Parallel resonant" crystal. Figure quoted is under all conditions including start up.
Crystal oscillator negative resistance	2	400			Ω	Includes temperature and process tolerances.
Comparison frequency				2	MHz	
Phase noise at phase detector			–142		dBC/Hz	6kHz loop BW, phase comparator freq 250kHz. Figure measured @ 1kHz offset, DSB (within loop band width).
RF division ratio		240		131071		Prescaler disabled, DE=0
		480		262142		Prescaler enabled, DE=1
Reference division ratio						See Table 1
Output ports P0–P3 #	7,8,9,10					
Sink current		10			mA	V_{PORT}=0.7V
Leakage current				10	µA	V_{PORT}=13.2V
Lock output	11					
Sink current		1			mA	V_{LOCK}=0.7V, 'out of lock'
Leakage current				10	µA	'in lock'

Ports P2 and P3 are not available on the SP5658F.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} at 0V

Characteristic	Pin (SP5658S)	Min	Max	Units	Conditions
Supply voltage, V_{CC}	12	–0.3	7	V	
RF input voltage	13, 14		2.5	V_{p-p}	AC coupled as per application
RF input DC offset	13, 14	–0.3	V_{CC}+0.3	V	
Port voltage	7 – 10	–0.3	14	V	Port in off state
	7 – 10	–0.3	6	V	Port in on state
Total port current	7 – 10		50	mA	
Lock output DC offset	11	–0.3	V_{CC}+0.3	V	
Charge pump DC offset	1	–0.3	V_{CC}+0.3	V	
Drive DC offset	16	–0.3	V_{CC}+0.3	V	
Crystal DC offset	2	–0.3	V_{CC}+0.3	V	
Data, Clock, Enable & Disable DC offset	3 – 6	–0.3	V_{CC}+0.3	V	
Storage temperature		–55	+125	°C	
Junction temperature			150	°C	
MP14 Thermal Resistance					
Chip to ambient			123	°C/W	
Chip to case			45	°C/W	
MP16 Thermal Resistance					
Chip to ambient			111	°C/W	
Chip to case			41	°C/W	
Power consumption at V_{CC}=5.5V			407	mW	All ports off, prescaler enabled
ESD protection	ALL	2		kV	MIL–STD 883 TM 3015

FUNCTIONAL DESCRIPTION

The SP5658 contains all the elements necessary, with the exception of a frequency reference, loop filter and external high voltage transistor, to control a varicap tuned local oscillator, so forming a complete PLL frequency synthesised source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with good phase noise performance. The RF preamplifier contains a selectable divide by two for operation above 2.0GHz. Up to 2GHz the RF input interfaces directly with the programmable divider, so eliminating degradation in phase noise due to the prescaler action. The block diagram is shown in Fig.2.

The SP5658 is controlled by a standard 3–wire bus comprising data, clock and enable inputs. The programming word for the 16 pin variant contains 28 bits, four of which are used for port selection, 18 to set the programmable divider ratio and enable/disable the prescaler, bit DE, three bits to select the reference division ratio, bits R0–R2, one bit to set charge pump current, bit C0, and the remaining two bits to access test modes, bit T0, and to disable the varactor drive, bit OS. The data word for 14 pin variant is identical to 16 pin except 26 bits only are required, two of which are used for port selection. The programming format is shown in Fig. 3.

The clock input is disabled by an enable low signal, data is therefore only clocked into the internal shift registers during an enable high and is loaded into the controlling buffers by an enable high to low transition. This load is also synchronised with the programmable divider so giving smooth fine tuning.

The RF signal is fed to an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier is fed to the ÷2/1 selectable prescaler and then to the 17 bit fully programmable divider, which is of MN+A architecture. The M counter is 13 bit and the A counter 4. If bit DE is set to a 0 the prescaler is disabled; Note that the control function DE cannot be used dynamically.

The output of the programmable divider is fed to the phase comparator where it is compared in both phase and frequency domain with the comparison frequency. This frequency is derived either from the on board crystal controlled oscillator or from an external source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider which is programmable into 1 of 8 ratios as described in Table 1.

The output of the phase comparator feeds the charge pump and loop amplifier section, which when used with an external high voltage transistor and loop filter integrates the current pulses into the varactor line voltage. The charge pump can be disabled to a high impedance state by the DISABLE input. The varactor drive output can also be disabled by the OS bit within the data word, so switching the external transistor 'OFF' and allowing an external voltage to be written to the varactor line for tuner alignment purposes.

The phase comparator also drives the lock detect circuit which generates a lock flag. 'In–lock' is indicated by a high impedance state on the lock output.

The programmable divider output divided by 2, $F_{pd}/2$ and the comparison frequency, F_{comp} can be switched to ports P0 and P1 respectively by switching the device into test mode. The test modes are described in Table 2.

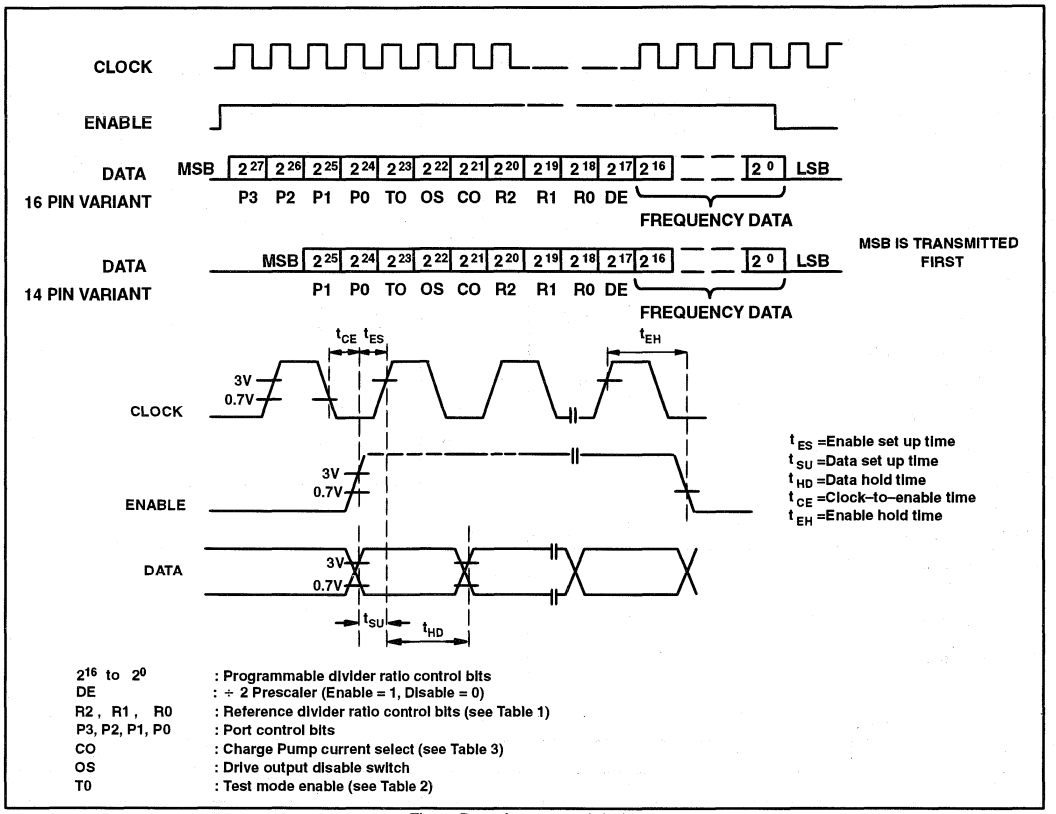


Fig. 3 Data format and timing

R2	R1	R0	RATIO	Comparison Frequency with a 4MHz external reference.
0	0	0	2	2MHz
0	0	1	4	1MHz
0	1	0	8	500kHz
0	1	1	16	250kHz
1	0	0	32	125kHz
1	0	1	64	62.5kHz
1	1	0	128	31.25kHz
1	1	1	256	15.625kHz

Table 1 Reference division ratios

TO	OS	DIS	P0/OP	P1/0C	FUNCTIONAL DESCRIPTION
0	0	0	#	#	NORMAL OPERATION
0	0	1	#	#	CHARGE PUMP DISABLE
1	0	0	$F_{pd/2}$	F_{comp}	NORMAL OPERATION
0	1	0	#	#	VARACTOR LINE DISABLE
0	1	1	#	#	CHARGE PUMP AND VARACTOR LINE DISABLE
1	X	1	–	–	NOT PERMITTED
#CONTROLLED BY BITS P0 AND P1 WITHIN DATA WORD					

Table 2 Test modes

C0	CURRENT IN mA		
	MIN	TYP	MAX
0	0.23	0.3	0.37
1	0.68	0.9	1.12

Table 3 Charge pump current

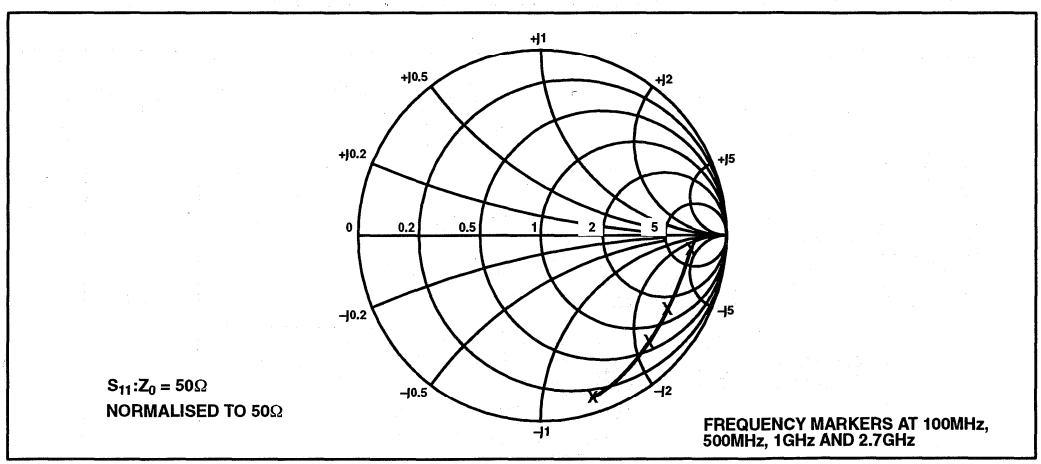


Fig. 4 Typical input impedance

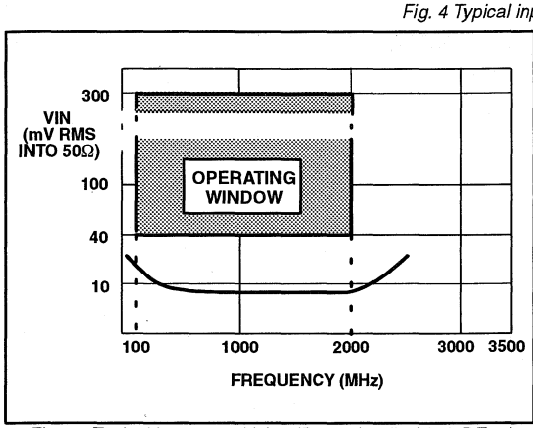


Fig. 5a Typical input sensitivity (Prescaler disabled, DE=0)

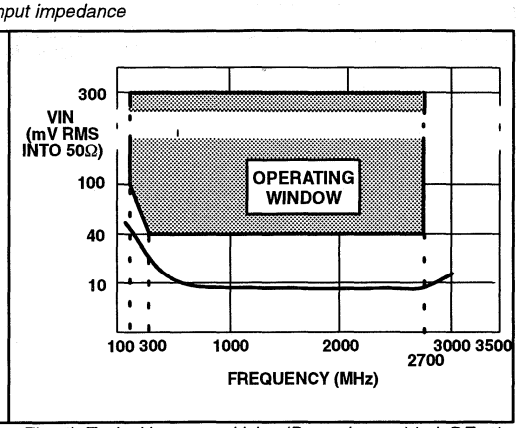


Fig. 5b Typical input sensitivity (Prescaler enabled, DE=1)

DOUBLE CONVERSION TUNER SYSTEMS

The high 2.7GHz maximum operating frequency and excellent noise characteristics of the SP5658 enables the construction of double conversion high IF tuners.

A typical system shown in Fig.7 will use the SP5658 as the first LO control for full band upconversion to an IF of greater than 1GHz. The wide range of reference division ratios allows the SP5658 to be used both for the up converter LO with a high phase comparator frequency (hence low phase noise) and the down converter which utilises the device in a lower comparison frequency mode (which offers a fine step size).

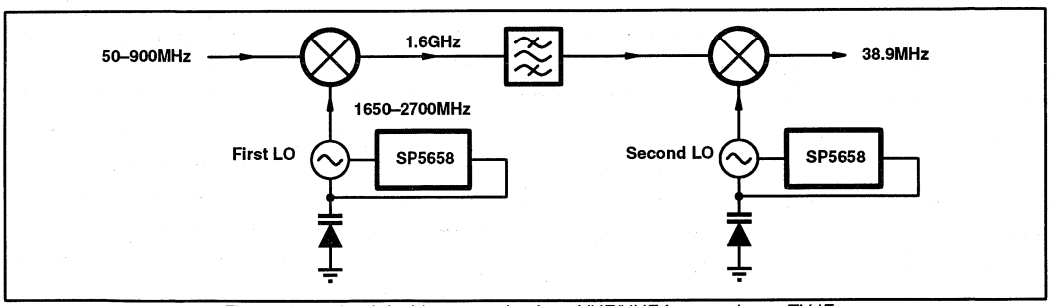


Fig. 6 Example of double conversion from VHF/UHF frequencies to TV IF

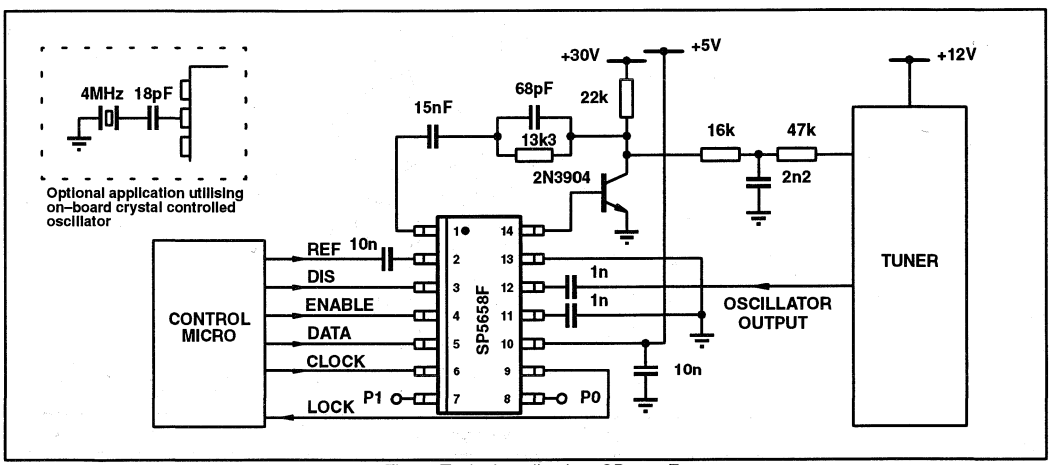


Fig. 7 Typical application, SP5658F

APPLICATION NOTES

A generic set of application notes AN168 for designing with synthesisers such as the SP5658 has been written. This covers aspects such as loop filter design and decoupling. This application note is also featured in the Media IC Handbook.

A generic test/demo board has been produced which can be used for the SP5658. A circuit diagram and layout for the board is shown in Figs. 8 and 9.

The board can be used for the following purposes:

(A) measuring RF sensitivity performance.
(B) Indicating port function.
(C) Synthesising a voltage controlled oscillator.
(D) Testing of external reference sources.

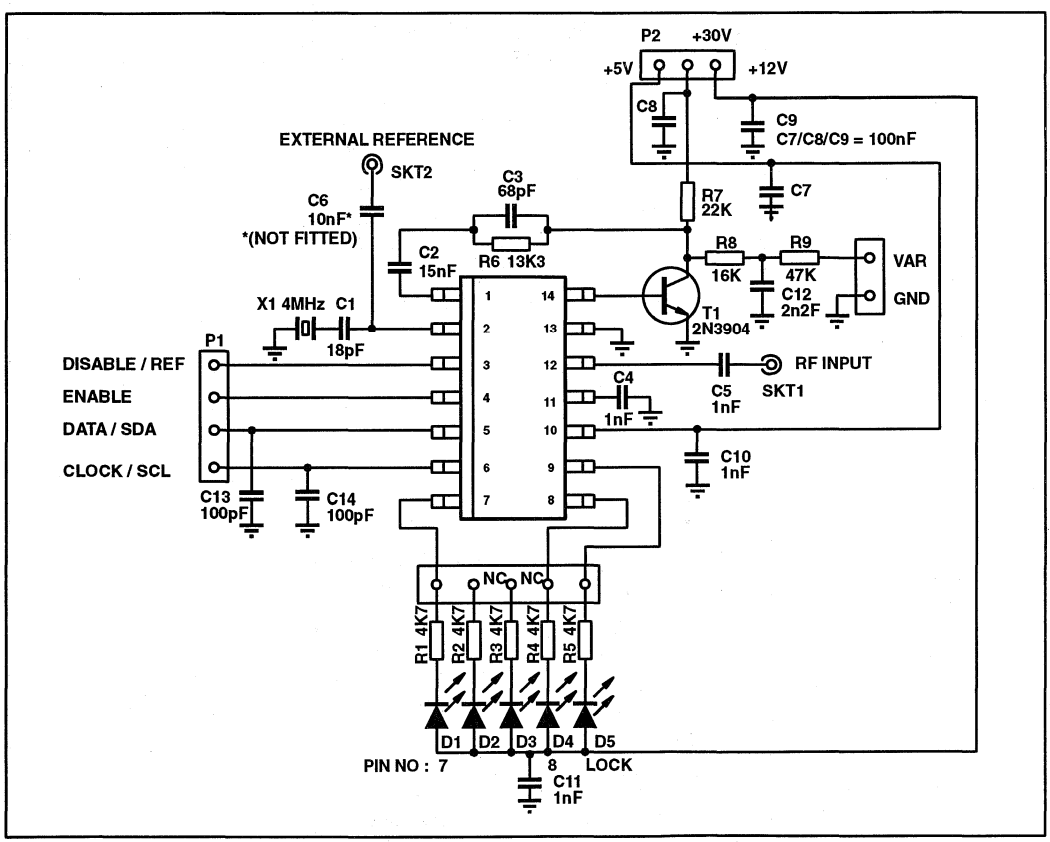
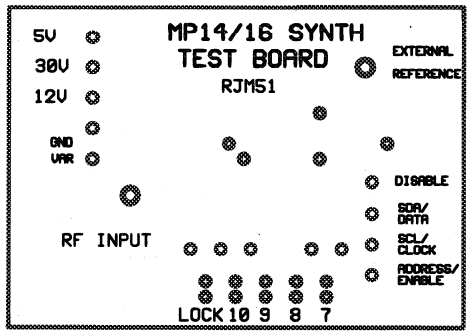
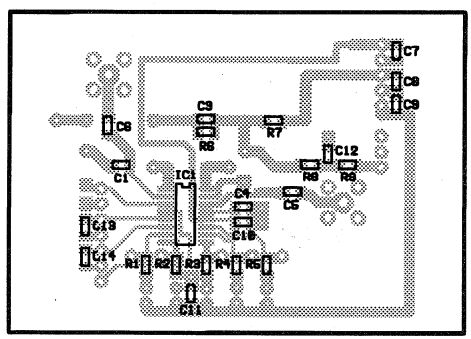


Fig. 8 Test board





RJM51 BOTTOM SILK SCREEN
COMPONENT LOCATION

Fig. 9 Test board (layout)

LOOP BANDWIDTH

The majority of applications for which the SP5658 is intended require a loop filter bandwidth of between 2kHz and 10kHz.

Typically the VCO phase noise will be specified at both 1kHz and10kHz offset. It is common practice to arrange the loop filter bandwidth such that the 1kHz figure lies within the loop bandwidth. Thus the phase noise depends on the synthesiser comparator noise floor, rather than the VCO.

The 10kHz offset figure should depend on the VCO providing the loop is designed correctly, and is not underdamped.

REFERENCE SOURCE

The SP5658 offers optimal LO phase noise performance when operated with a large step size. This is due to the fact that the LO phase noise within the loop bandwidth is:

$$\text{phase comparator noise floor} + 20 \log_{10} \left(\frac{\text{LO frequency}}{\text{phase comparator frequency}} \right)$$

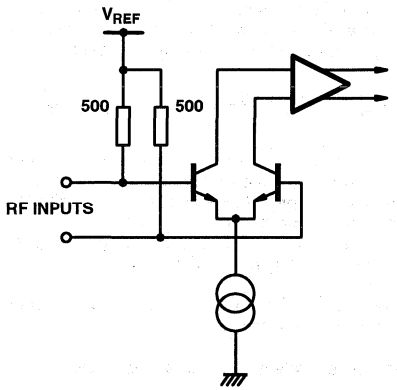
Assuming the phase comparator noise floor is flat irrespective of sampling frequency, this means that the best performance will be achieved when the overall LO to phase comparator division ratio is a minimum.

There are two ways of achieving a higher phase comparator sampling frequency:–

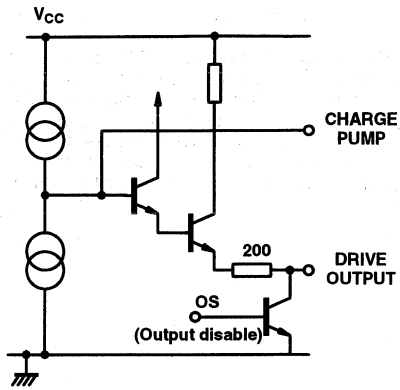
A) Reduce the division ratio between the reference source and the phase comparator

B) use a higher reference source frequency.

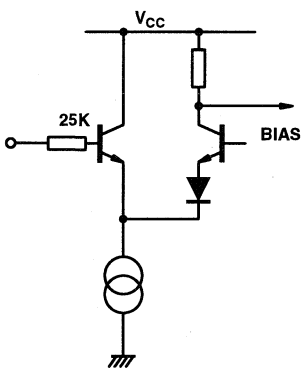
Approach B) may be preferred for best performance since it is possible that the noise floor of the reference oscillator may degrade the phase comparator performance if the reference division ratio is very small.



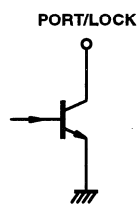
RF inputs



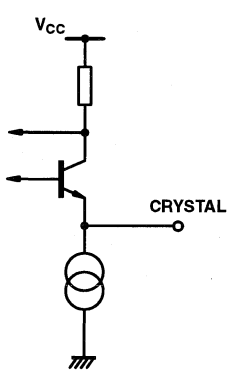
Loop amplifier



Disable, Enable, Data and Clock inputs



Output Ports and Lock Output



Reference oscillator

Fig.10 Input/Output interface circuits

SP5659

2.7GHz I²C BUS CONTROLLED LOW PHASE NOISE FREQUENCY SYNTHESISER

The SP5659 is a single chip frequency synthesiser designed for tuning systems up to 2.7GHz.

The RF preamplifier drives a divide by two prescaler which can be disabled for applications up to 2GHz, allowing direct interfacing with the programmable divider so enabling a step size equal to the comparison frequency. For applications up to 2.7GHz the divide by two is enabled, giving a step size of twice the comparison frequency.

The comparison frequency is obtained either from an on–chip crystal controlled oscillator, or from an external source. The oscillator frequency F_{ref} or the comparison frequency F_{comp} may be switched to the REF/COMP output. This feature is ideally suited to providing the reference frequency for a second synthersiser such as in a double conversion tuner (see Fig. 8).

The synthesiser is controlled via an I²C bus, and responds to one of four programmable addresses which are selected by applying a specific voltage to the 'address' input. This feature enables two or more synthesisers to be used in a system.

The device contains four switching ports P0–P3 and a 5–level ADC. The output of the ADC can be read via the I²C bus.

The device also contains a varactor line disable and charge pump disable facility.

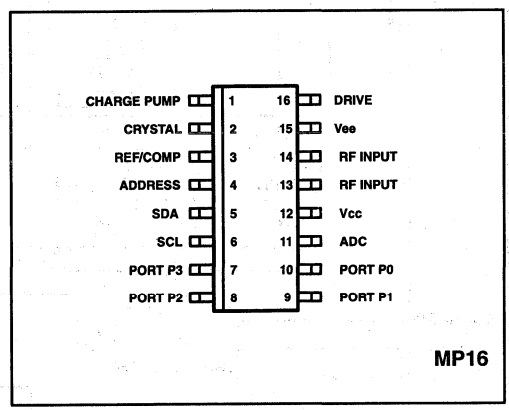


Fig. 1 Pin connections – top view

FEATURES

- Complete 2.7GHz single chip system
- Optimised for low phase noise
- Selectable divide by two prescaler
- Selectable reference division ratio
- Selectable reference/comparison frequency output
- Selectable charge pump current
- Four selectable I²C bus address
- 5–level ADC
- Pin compatible with the SP5658 3–wire bus controlled synthesiser
- ESD protection; (Normal ESD handling procedures should be observed)

APPLICATIONS

- SAT, TV, VCR and Cable tuning systems
- Communications systems

ORDERING INFORMATION

SP5659/KG/MP1S (Tubes)
SP5659/KG/MP1T (Tape and reel)

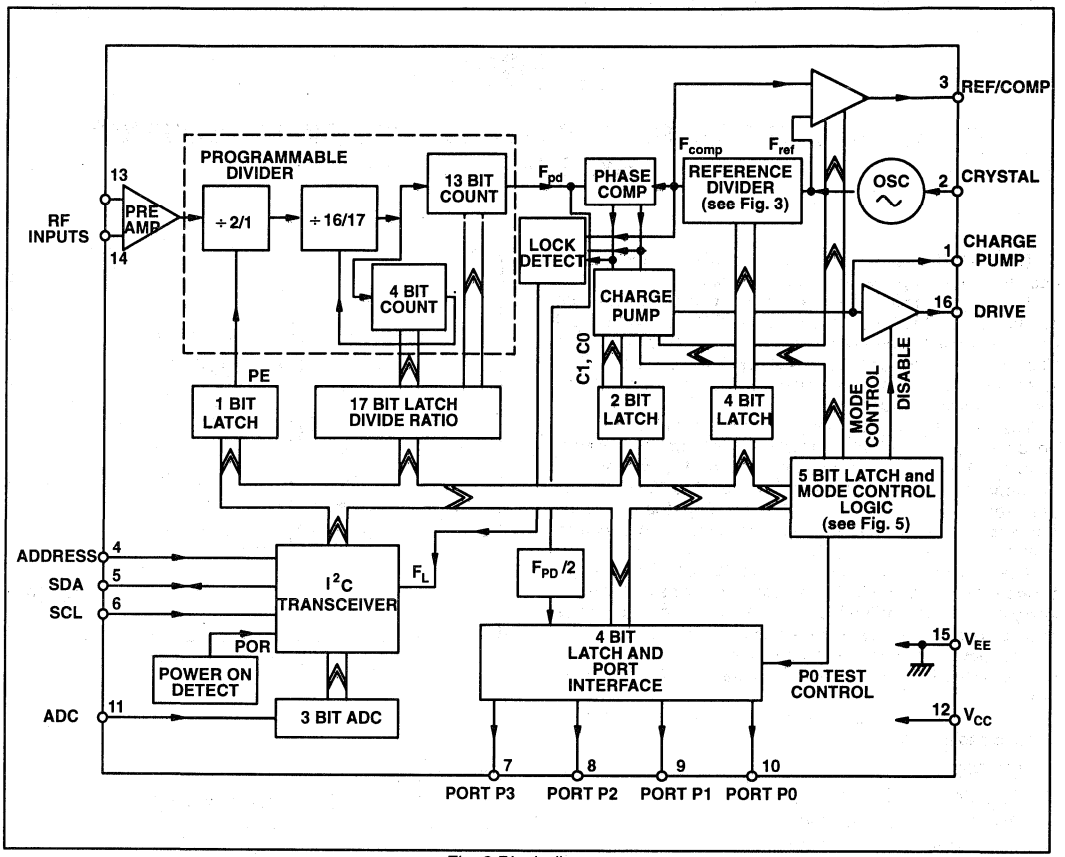


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +80°C, V_{CC}=+4.5V to +5.5V. Reference frequency = 4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current, I_{CC}	12		68	85	mA	V_{CC} = 5V prescaler enabled, PE = 1
			58	73	mA	V_{CC} = 5V prescaler disabled, PE = 0
RF input voltage	13, 14	40		300	mV_{rms}	300MHz to 2.7GHz Prescaler enabled, PE = 1, See Fig. 7b.
	13, 14	100		300	mVrms	100MHz prescaler enabled, PE=1, See Fig. 7b.
		40		300	mV_{rms}	100MHz to 2.0GHz Prescaler disabled PE = 0, See Fig. 7a
RF input impedance	13, 14		50		Ω	Refer to Fig. 13
RF input capacitance	13, 15		2		pF	Refer to Fig. 13

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb}= –20°C to +80°C, V_{CC}=+4.5V to +5.5V. Reference frequency = 4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
SDA, SCL	5, 6					
Input High voltage		3		5.5	V	
Input Low voltage		0		1.5	V	
Input High current				10	µA	Input voltage = V_{CC}
Input Low Current				–10	µA	Input voltage = V_{EE}
LeakageCurrent				10	µA	V_{CC} = V_{EE}
Input hysteresis			0.8		V	
SDA Output voltage	5			0.4	V	I_{sink} = 3mA
Charge pump output current	1					See Fig. 6, V_{pin} = 2V
Charge pump output leakage	1		±3	±10	nA	V_{pin1} = 2V
Charge pump drive output current	16	1			mA	V_{pin16} = 0.7V
Drive output saturation voltage when disabled	16			350	mV	
External reference input frequency	2	2		20	MHz	AC coupled sinewave
External reference input ampltude	2	200		500	mV_{p-p}	AC coupled sinewave
Crystal frequency	2	4		16	MHz	
Crystal oscillator drive level	2		35		mV_{p-p}	
Recommended crystal series resistance		10		200	Ω	Applies to 4MHz crystal only. 'Parallel resonant' crystal. Figure quoted is under all conditions including start up.
Crystal oscillator negative resistance	2	400			Ω	Includes temperature and process tolerances.
REF/COMP output	3					
Voltage			350		mV_{p-p}	AC coupled output. Output enabled, RE=1. See Note 1.
Comparison frequency				2	MHz	
Equivalent phase noise at phase detector			–142		dBC/Hz	6kHz loop BW, phase comparator freq 250kHz. Figure measured @ 1kHz offset, DSB (within loop band width).
RF division ratio		240		131071		Prescaler disabled, PE = 0
		480		262142		Prescaler enabled, PE = 1
Reference division ratio						See Fig. 3
Output ports P0, P1, P2, P3	7,8,9, 10					
Sink current		10			mA	V_{port} = 0.7V
Leakage current				10	µA	V_{port} = 13.2V
ADC input voltage	11					See Table 4, Fig 4
ADC input current	11			±10	µA	$V_{CC} \geq V_{input} \geq V_{EE}$
Address input current High	4			1	mA	Input voltage =V_{CC}
Address input current Low	4			–0.5	mA	Input voltage =V_{EE}

Note 1: If the REF/COMP output is not used, the output should be left open circuit or connected to V_{CC}, and disabled by setting RE=0.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} at 0V.

Characteristics	Pin	Value		Units	Conditions
		Min	Max		
Supply Voltage, V_{CC}	12	–0.3	7	V	
RF input voltage	13,14		2.5	V_{p-p}	AC coupled as per application
RF input DC offset	13,14	–0.3	V_{CC}+0.3	V	
Port voltage	7–10	–0.3	14	V	Port in off state
	7–10	–0.3	6	V	Port in on state
Total port current	7–10		50	mA	
ADC input DC offset	11	–0.3	V_{CC}+0.3	V	
REF/COMP output DC offset	3	–0.3	V_{CC}+0.3	V	
Charge pump DC offset	1	–0.3	V_{CC}+0.3	V	
Drive DC offset	16	–0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	–0.3	V_{CC}+0.3	V	
Address DC offset	4	–0.3	V_{CC}+0.3	V	
SDA and SCL DC offset	5, 6	–0.3	6V	V	
Storage temperature		–55	+150	°C	
Junction temperature			+150	°C	
MP16 thermal resistance					
chip to ambient			111	°C/W	
chip to case			41	°C/W	
Power consumption at V_{CC}=5.5V			468	mW	All ports off, prescaler enabled
ESD protection	All	4		kV	Mil Std 883 TM 3015

FUNCTIONAL DESCRIPTION

The SP5659 contains all the elements necessary, with the exception of a frequency reference, loop filter and external high voltage transistor, to control a varicap tuned local oscillator, so forming a complete PLL frequency synthesised source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with good phase noise performance. The block diagram is shown in Fig. 2.

The RF input signal is fed to an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier interfaces with the 17–bit fully programmable divider via a divide–by–two prescaler. For applications up to 2GHz RF input, the prescaler may be disabled so eliminating the degradation in phase noise due to prescaler action. The divider is of MN+A architecture, where the dual modulus prescaler is 16/17, the A counter is 4–bits, and the M counter is 13–bits.

The output of the programmable divider is fed to the phase comparator where it is compared in both phase and frequency domain with the comparison frequency. This frequency is derived either from the on–board crystal controlled oscillator or from an external reference source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider which is programmable into 1 of 15 ratios as detailed in Fig. 3.

The output of the phase detector feeds a charge pump and loop amplifier section, which when used with an external high voltage transistor and loop filter, integrates the current pulses into the varactor line voltage. By invoking the device test modes as described in Fig. 5, the varactor drive output can be disabled so switching the external transistor 'off' and allowing an external voltage to be written to the varactor line for tuner alignment purposes. Similarly, the charge pump may be also disabled to a high impedance state.

The programmable divider output Fpd/2 can be switched to port P0 by programming the device into test mode. The test modes are described in Fig. 5

PROGRAMMING

The SP5659 is controlled by an I^2C data bus. Data and Clock are fed in on the SDA and SCL lines respectively as defined by I^2C bus format. The synthesiser can either accept data (write mode) or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low, and read mode if it is high. Tables 1 and 2 in Fig. 4 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I^2C bus system. Table 3 in Fig.4 shows how the address is selected by applying a voltage to the 'address' input. When the device receives a valid address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are received. When the device is programmed into read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status

byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

WRITE MODE

With reference to Table 1, bytes 2 and 3 contain frequency information bits 2^{14}–2^{0} inclusive. Auxillary frequency bits 2^{16}–2^{15} are in byte 4. For most frequencies only bytes 2 and 3 will be required. The remainder of byte 4 and byte 5 control the prescaler enable, reference divider ratio (see Fig. 3), charge pump, REF/COMP output (see Fig. 5), output ports and test modes (see Fig. 5).

After reception and acknowledgement of a correct address (byte 1), the first bit of the following byte determines whether the byte is interpreted as a byte 2 or 4, a logic '0' indicating byte 2 and a logic '1' indicating byte 4. Having interpreted this byte as either byte 2 or 4 the following data byte will be interpreted as byte 3 or 5 respectively. Having received two complete data bytes, additional data bytes can be entered, where byte interpretation follows the same procedure, without readdressing the device. This procedure continues until a STOP condition is received. The STOP condition can be generated after any data byte, if however it occurs during a byte transmission, the previous data is retained.

To facilitate smooth fine tuning, the frequency data bytes are only accepted by the device after all 17 bits of frequency data have been received, or after the generation of a STOP condition. Repeatedly sending bytes 2 and 3 only will not change the frequency. A frequency change occurs when one of the following data sequences is sent to an addressed device;

Bytes 2, 3, 4, 5
Bytes 4, 5, 2, 3

or when a STOP condition follows valid data bytes as follows;

Bytes 2, 3, 4, STOP
Bytes 4, 5, 2 STOP
Bytes 2, 3, STOP
Bytes 2, STOP
Bytes 4, STOP

It should be noted that the device must be initially addressed with both frequency AND control byte data, since the control byte contains reference divider information which must be provided before a chosen frequency can be synthesised. This implies that after initial turn on, bytes 2, 3, 4 must be sent followed by a STOP condition as a minimum requirement. Alternatively bytes 2, 3, 4, 5 must be sent if port information is also required.

READ MODE

When the device is in read mode, the status byte read from the device takes the form shown in Table 2, Fig. 4.

Bit 1 (POR) is the power–on reset indicator, and this is set to a logic '1' if the VCC supply to the device has dropped below 3V (at 25°C), e.g. when the device is initially turned ON. The POR is reset to '0' when the read sequence is terminated by a STOP command. When POR is set high (at low VCC), the programmed information is lost and the output ports are all set to high impedance.

Bit 2 (FL) indicates whether the device is phase locked, a logic '1' is present if the device is locked, and a logic '0' if the device is unlocked.

Bits 6,7 and 8 (A2, A1, A0) combine to give the output of the ADC. The ADC can be used to feed AFC information to the microprocessor via the I^2C bus.

ADDITIONAL PROGRAMMABLE FEATURES

Prescaler enable

The divide by two prescaler is enabled by setting bit PE within byte 4 to a logic '1'. A logic '0' disables the prescaler, directly passing the RF input frequency to the 17–bit programmable counter. Bit PE is a static select only.

Charge pump current

The charge pump current can be programmed by bits C1 and C0 within data byte 5, as defined in Fig. 6.

Test mode

The test modes are invoked by setting bits RE=0 and RTS=1 within the programming data, and are selected by bits TS2, TS1 and TS0 as shown in Fig. 5. When TS2, TS1 and TS0 are received, the device retains previously received P2, P1 and P0 data.

Reference/Comparison frequency output

The reference frequency F_{ref} can be switched to the REF/COMP output, pin 3, by setting bit RE=1 and RTS=0 within byte 5. The comparison frequency F_{comp} can be switched to the REF/COMP output, pin 3, by setting bit RE=1 and RTS=1 within byte 5. For RE set to logic '0', the output is disabled and set to a high state. RE and RTS default to logic '1' during device power up, thus enabling the comparison frequency F_{comp} at the REF/COMP output.

R3	R2	R1	R0	Ratio	Comparison frequency with a 4MHz external reference
0	0	0	0	2	2MHz
0	0	0	1	4	1MHz
0	0	1	0	8	500kHz
0	0	1	1	16	250kHz
0	1	0	0	32	125kHz
0	1	0	1	64	62.5kHz
0	1	1	0	128	31.25kHz
0	1	1	1	256	15.625kHz
1	0	0	0	Not Allowed	–
1	0	0	1	5	800kHz
1	0	1	0	10	400kHz
1	0	1	1	20	200kHz
1	1	0	0	40	100kHz
1	1	0	1	80	50kHz
1	1	1	0	160	25kHz
1	1	1	1	320	12.5kHz

Fig. 3 Reference division ratios

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	Byte 1
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	Byte 2
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	Byte 3
CONTROL DATA	1	2^{16}	2^{15}	PE	R3	R2	R1	R0	A	Byte 4
CONTROL DATA	C1	C0	RE	RTS	P3	P2/TS2	P1/TS1	P0/TS0	A	Byte 5

Table 1 Write data format (MSB is transmitted first)

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	1	A	Byte 1
STATUS BYTE	POR	FL	X	X	X	A2	A1	A0	A	Byte 2

Table 2 Read data format (MSB is transmitted first)

A	:	Acknowledge bit
MA1, MA0	:	Variable address bits (see Table 3)
2^{16}–2^{0}	:	Programmable division ratio control bits
PE	:	Prescaler enable
R3,R2,R1,R0	:	Reference division ratio select (see Fig. 3)
C1, C0	:	Charge pump current select (see Fig.6)
RE	:	Reference oscillator output enable
RTS	:	REF/COMP output select when RE=1 (see Fig.5)
RTS	:	Test mode enable when RE=0 (see Fig.5)
TS2, TS1, TS0	:	Test mode control bits (valid when RE=0, RTS=1, see Fig. 5)
P0	:	P0 port output state (always valid except when RE=0, RTS=1)
P3, P2, P1	:	P3, P2 and P1 port output states
POR	:	Power On Reset indicator
FL	:	Phase Lock Flag
A2, A1, A0	:	ADC data (see Table 4)
X	:	Don't care

MA1	MA0	Address input voltage level
0	0	$0 - 0.1V_{CC}$
0	1	Open circuit
1	0	$0.4V_{CC} - 0.6V_{CC}$ #
1	1	$0.9V_{CC} - V_{CC}$

Programmed by connecting a 15kΩ resistor between pin 4 and V_{CC}

Table 3 Address selection

A2	A1	A0	Voltage on ADC input
1	0	0	$0.6V_{CC} - V_{CC}$
0	1	1	$0.45V_{CC}$ to $0.6V_{CC}$
0	1	0	$0.3V_{CC}$ to $0.45V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.3V_{CC}$
0	0	0	0 to $0.15V_{CC}$

Table 4 ADC levels

Fig. 4 Data formats

RE	RTS	TS2	TS1	TS0	REF/COMP OUTPUT MODE	Test mode description
0	0	X	X	X	Disabled to high state	Normal operation
0	1	X	0	0	Disabled to high state	Charge pump sink. Status byte FL = logic '1'
0	1	X	0	1	Disabled to high state	Charge pump source. Status byte FL = logic '0'
0	1	X	1	0	Disabled to high state	Charge pump disabled. Status byte FL=logic '0'
0	1	X	1	1	Disabled to high state	Port P0 = $F_{pd}/2$
0	1	1	X	X	Disabled to high state	Varactor Drive Output disabled
1	0	X	X	X	F_{ref} switched	Normal operation
1	1	X	X	X	F_{comp} switched	Normal operation

X=don't care

Fig. 5 REF/COMP output mode and Test modes

C1 byte 5, bit 1	C0 byte 5, bit 2	Current in µA		
		min	typ	max
0	0	±90	±120	±150
0	1	±195	±260	±325
1	0	±416	±555	±694
1	1	±900	±1200	±1500

Fig 6. Charge pump current

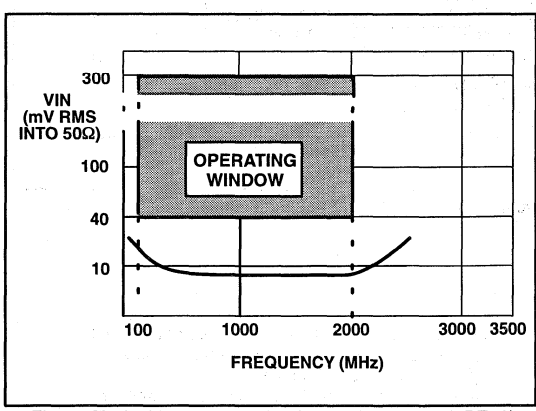


Fig. 7a Typical input sensitivity (Prescaler disabled, PE=0)

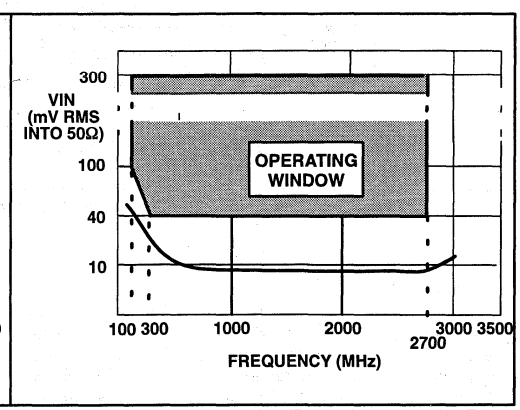


Fig. 7b Typical input sensitivity (Prescaler enabled, PE=1)

DOUBLE CONVERSION TUNER SYSTEMS

The high 2.7GHz maximum operating frequency and excellent noise characteristics of the SP5659 enables the construction of double conversion high IF tuners.

A typical system shown in Fig.8 will use the SP5659 as the first LO control for full band upconversion to an IF of greater than 1GHz. The wide range of reference division ratios allows the SP5659 to be used both for the up converter LO with a high phase comparator frequency (hence low phase noise) and the down converter which utilises the device in a lower comparison frequency mode (which offers a fine step size).

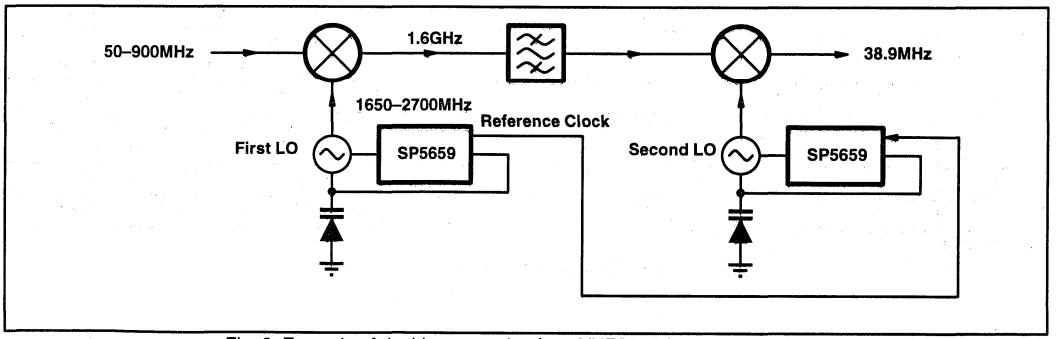


Fig. 8 Example of double conversion from VHF/UHF frequencies to TV IF

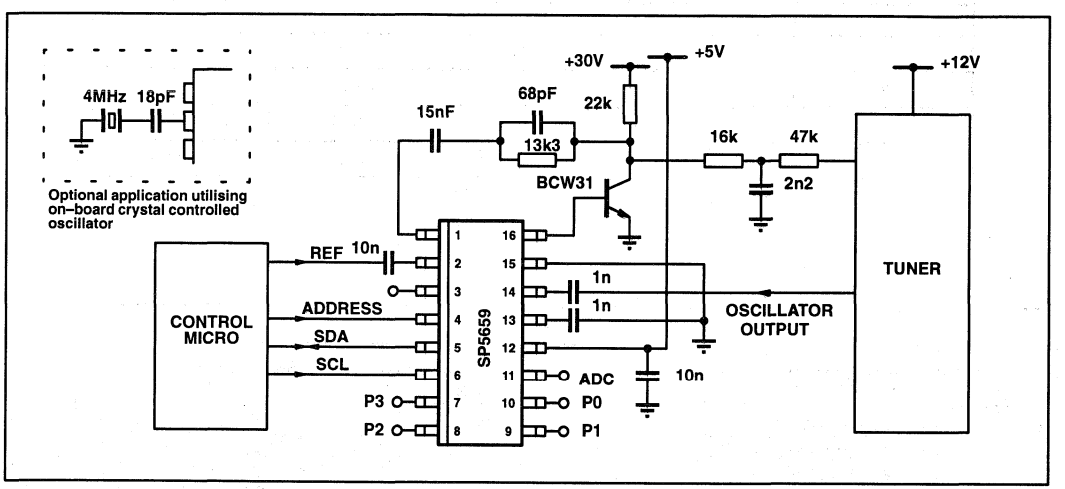


Fig. 9 Typical application

APPLICATION NOTES

A generic set of application notes AN168 for designing with synthesisers such as the SP5659 has been written. This covers aspects such as loop filter design and decoupling. This application note is also featured in the Consumer Data Book.

A generic test/demo board has been produced which can be used for the SP5659. A circuit diagram and layout for the board is shown in Figs. 10 and 11.

The board can be used for the following purposes:

(A) measuring RF sensitivity performance.
(B) Indicating port function.
(C) Synthesising a voltage controlled oscillator.
(D) Testing of external reference sources.

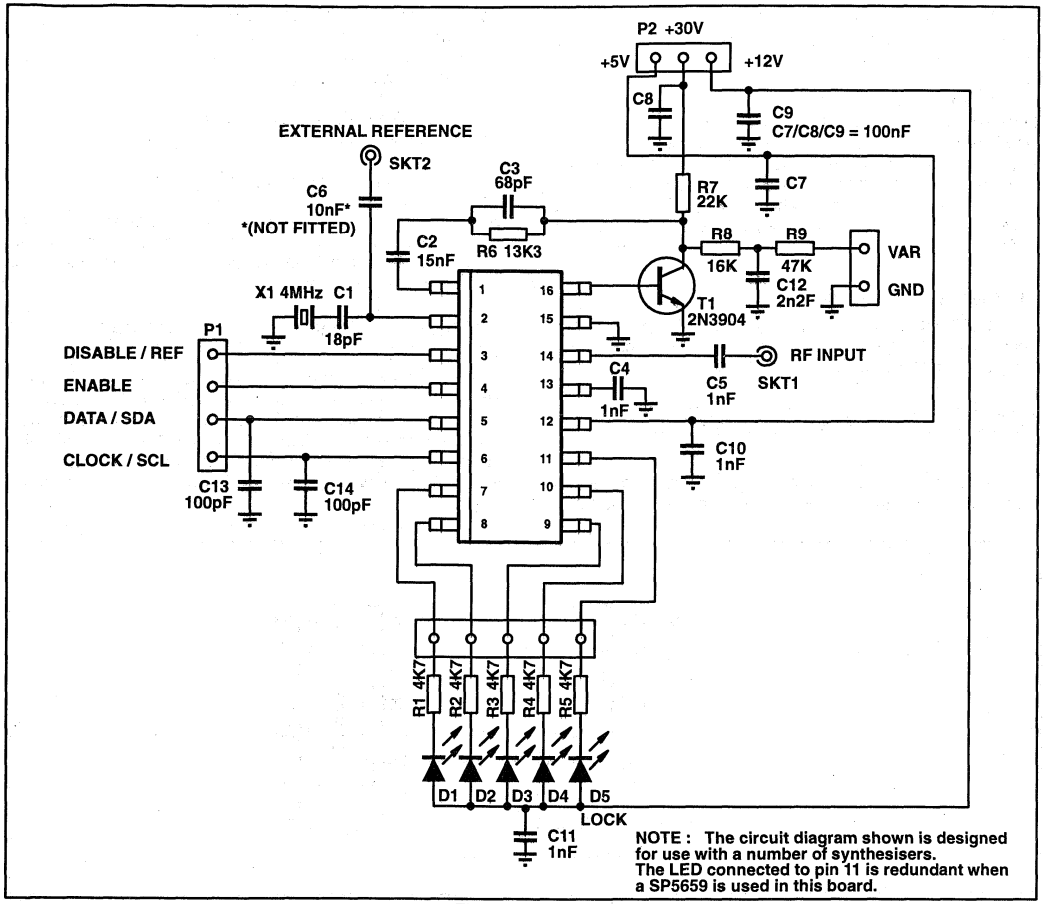


Fig. 10 Test board

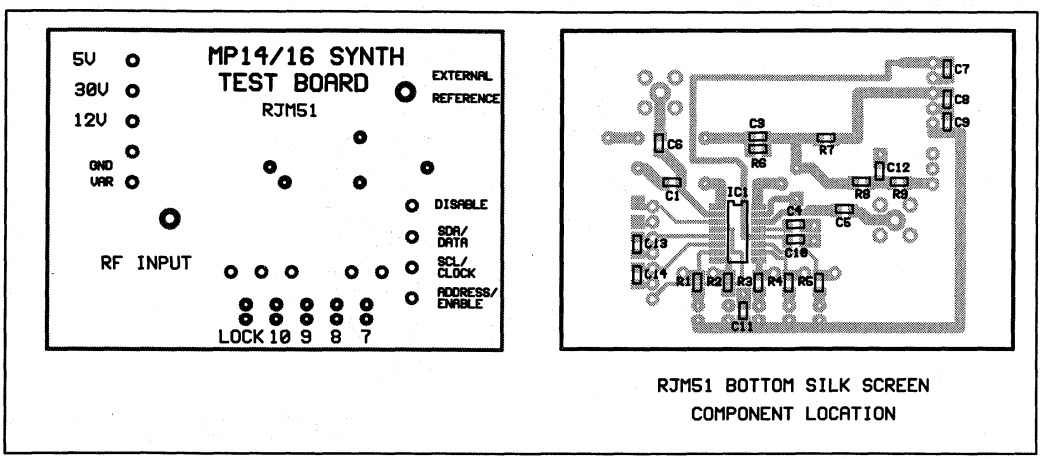


Fig. 11 Test board (layout)

LOOP BANDWIDTH

The majority of applications for which the SP5659 is intended require a loop filter bandwidth of between 2kHz and 10kHz.

Typically the VCO phase noise will be specified at both 1kHz and10kHz offset. It is common practice to arrange the loop filter bandwidth such that the 1kHz figure lies within the loop bandwidth. Thus the phase noise depends on the synthesiser comparator noise floor, rather than the VCO.

The 10kHz offset figure should depend on the VCO providing the loop is designed correctly, and is not underdamped.

REFERENCE SOURCE

The SP5659 offers optimal LO phase noise performance when operated with a large step size. This is due to the fact that the LO phase noise within the loop bandwidth is:

$$\text{phase comparator noise floor} + 20\log_{10}\left(\frac{\text{LO frequency}}{\text{phase comparator frequency}}\right)$$

Assuming the phase comparator noise floor is flat irrespective of sampling frequency, this means that the best performance will be achieved when the overall LO to phase comparator division ratio is a minimum.

There are two ways of achieving a higher phase comparator sampling frequency:–

A) Reduce the division ratio between the reference source and the phase comparator

B) use a higher reference source frequency.

Approach B) may be preferred for best performance since it is possible that the noise floor of the reference oscillator may degrade the phase comparator performance if the reference division ratio is very small.

DRIVING TWO DEVICES FROM A COMMON REFERENCE

As mentioned earlier in the Datasheet, the SP5659 has a REF/COMP output which allows two synthesisers to be driven from a common reference. To do this, the "Master" should be programmed by setting RE = 1 and RTS = 0. The driven device should be programmed for normal operation i.e. RE = 0, and RTS = 0. The two devices should be connected as shown below.

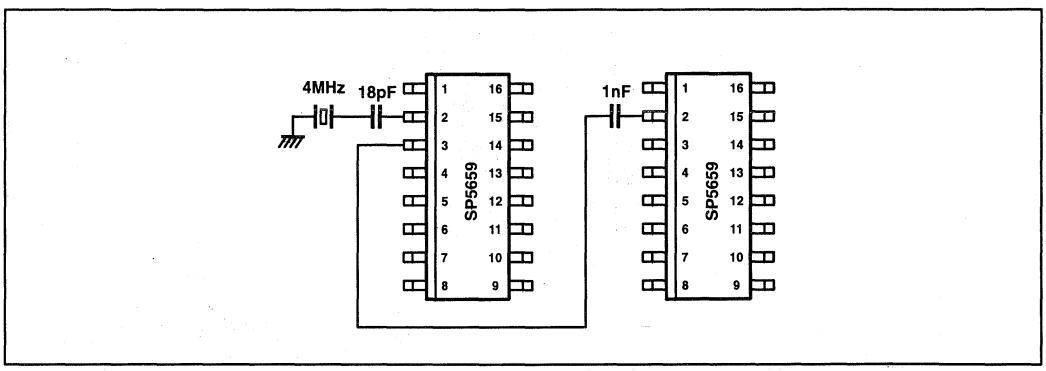


Fig. 12 Driving two devices from a common reference

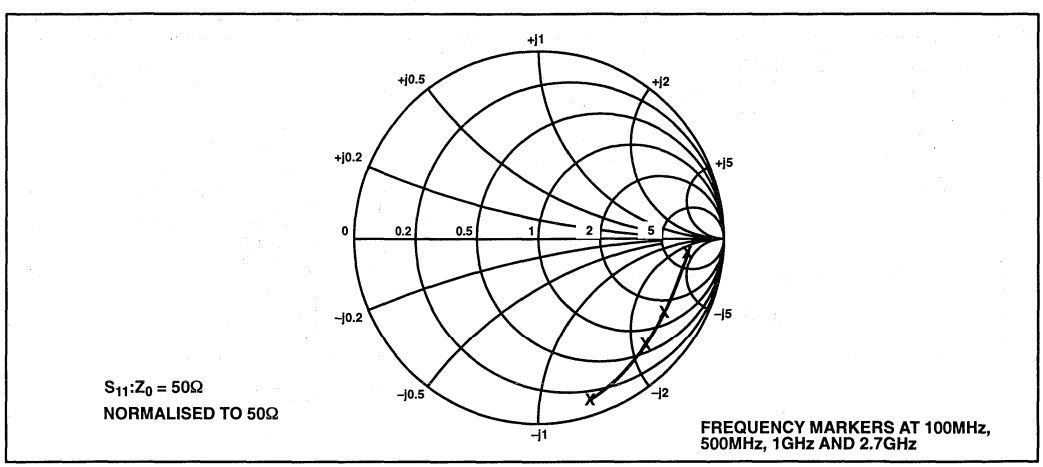
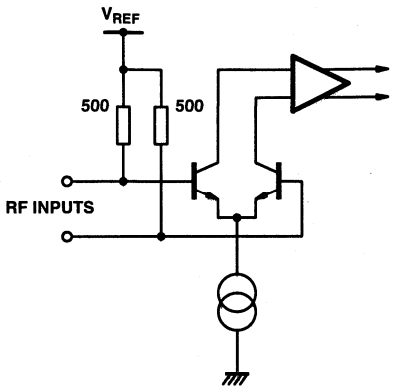
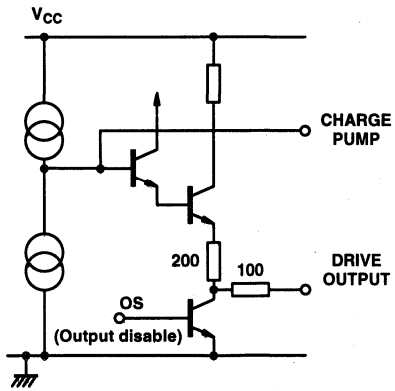


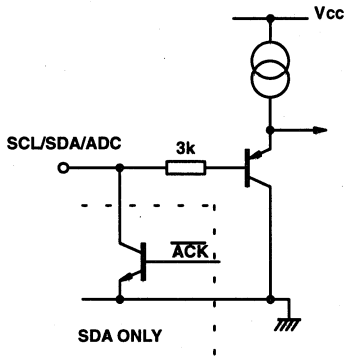
Fig. 13 Typical RF input impedance



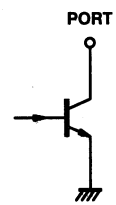
RF inputs



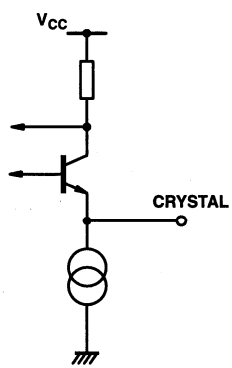
Loop amplifier



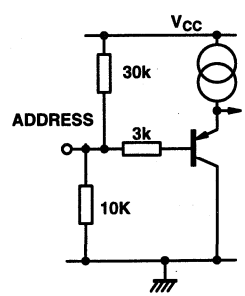
SDA and SCL and ADC



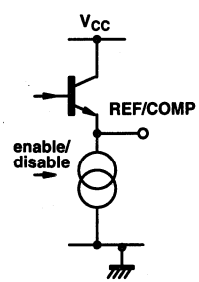
Output Ports



Reference oscillator



Address input



REF/COMP output

Fig.14 Input/Output interface circuits

Section 2

Satellite TV Receiver Circuits

GEC PLESSEY
SEMICONDUCTORS

VP211

DUAL 90MHz 6-BIT ANALOG TO DIGITAL CONVERTER

The VP211 is a dual 90MHz 6-bit Analog to Digital Converter designed for use in consumer satellite receivers and decoders, video systems, multimedia and communications applications.

Operating from a single +5V supply, the VP211 includes an on-chip high bandwidth ADC driver amplifier, a 6-bit ADC and digital I/O that can be interfaced to either +5V or +3V. The VP211 also has the necessary bias voltages for the reference resistor chain in the 'flash' architecture of the ADC.

FEATURES

- 90MHz Conversion Rate
- TTL Clock/Data Interface
- 2 Volt Analog Input Range
- Internal ADC Reference
- Digital I/O's compatible with +5V or +3V logic
- Single 5 Volt Supply
- Dual ADC System for good channel matching

APPLICATIONS

- Satellite Decoders
- Multimedia
- Communications

ORDERING INFORMATION

VP211A CG MP1S (Commercial - 28 pin plastic SO)

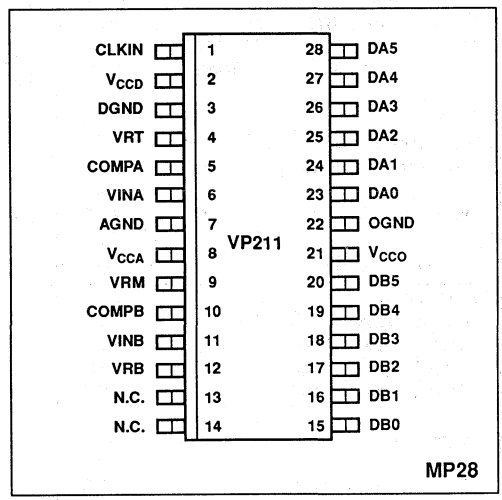


Fig.1 Pin connections - top view (wide body)

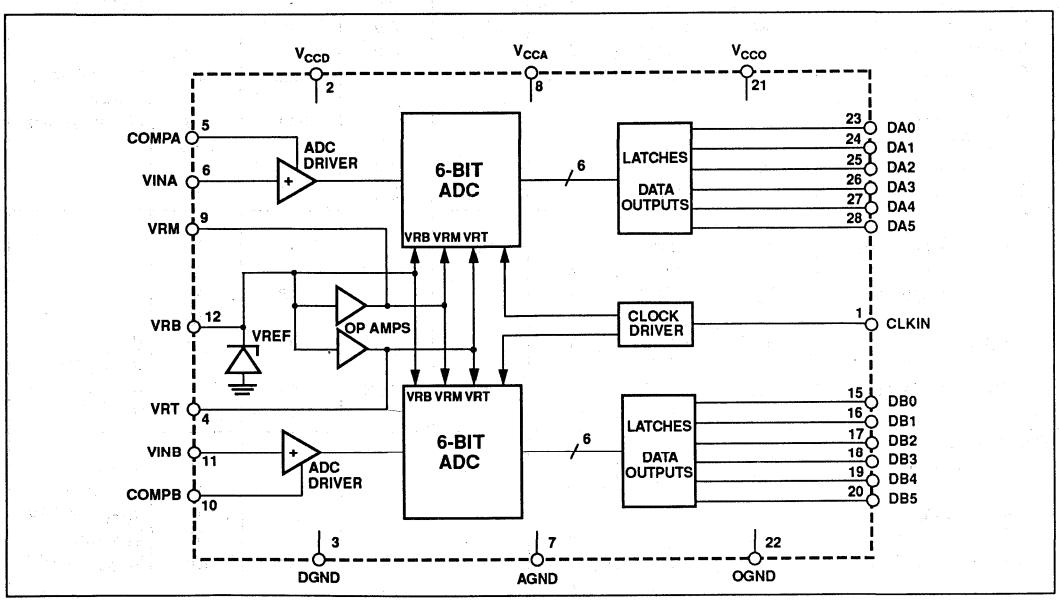


Fig.2 System block diagram

ABSOLUTE MAXIMUM RATINGS

DC supply voltage (V_{CCA}, V_{CCD}, V_{CCO})	-0.3 to+7V
Analog input voltage (VIN)	-0.3 to V_{CC}+0.3V
Digital inputs (CLKIN)	V_{CC}
Digital output current (Ioh, Iol, Isc)	-20 to +20mA
Ambient operating temperature (Tamb)	0°C to +70°C
Storage temperature (Tstorage)	-55°C to +125°C

THERMAL CHARACTERISTICS

THERMAL RESISTANCES

Junction to case(Θjc)	32°C/W
Junction to ambient(Θja)	84°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated) Tamb = 25°C, $V_{CCA/D/O}$ = +5V, full temperature range = 0°C to +70°C

DC CHARACTERISTICS All specifications apply to either of the two ADCs

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Resolution	-	-	-	6	-	-	Bits	
Static performance								
Differential non-linearity	DNL	+25°C	4	-	-	±0.5	LSB	
		Full	4	-	-	±0.5	LSB	
Integral non-linearity	INL	+25°C	4	-	-	±0.5	LSB	
		Full	4	-	-	±0.5	LSB	
No missing codes		Full	4	Guaranteed				
Power supply								
Analog supply voltage	V_{CCA}	Full	4	4.75	5.0	5.25	V	
Digital supply voltage	V_{CCD}	Full	4	4.75	5.0	5.25	V	
Output supply voltage	V_{CCO}	Full	4	4.75	5.0	5.25	V	
Analog supply current	AI_{CC}	+25°C	1	14	19	26	mA	
		Full	4	-	-	-	mA	
Digital supply current	DI_{CC}	+25°C	1	34	42	51	mA	
		Full	4	-	-	-	mA	
Output supply current	OI_{CC}	+25°C	1	3	11	15	mA	
		Full	4	-	-	-	mA	
Power dissipation	PD	+25°C	1	260	360	460	mW	
Analog input								
Input range	V_{in}	Full	5	-	2.0	-	V	Pk to Pk
Input resistance	R_{in}	+25°C	1	20k	25k	30k	Ω	
Input capacitance	C_{in}	+25°C	5	-	4.0	-	pF	
Gain variation	G_V	+25°C	4	-	-	0.25	dB	Fin=300Hz to 20MHz
Gain matching	G_m	+25°C	1	-	-	0.25	dB	Fin=15.68MHz
Input -3dB bandwidth	F3dB	+25°C	5	-	200	-	MHz	
Ain input voltage	Aindc	+25°C	1	3.6	3.9	4.1	V	
Comp output	Vcomp	+25°C	1	1.8	2.0	2.2	V	
CLKIN								
Input voltage high	V_{ih}	+25°C	1	2.0	-	-	V	
		Full	4	-	-	-	V	
Input voltage low	V_{il}	+25°C	1	-	-	0.8	V	
		Full	4	-	-	-	V	
Input current high	I_{ih}	+25°C	1	-	-	1	µA	V_{CCD} = 5.25V
		Full	4	-	-	-		V_{in} = 2.7V
Input current low	I_{il}	+25°C	1	–0.2	–0.35	–0.5	mA	V_{CCD} = 5.25V
		Full	4	-	-	-		V_{in} = 0.4V
TTL digital outputs								
Output voltage high	V_{oh}	+25°C	1	2.4	-	3.0	V	V_{CCO} = 4.75V
		Full	4	-	-	-	V	I_{oh} = 400µA
Output voltage low	V_{ol}	+25°C	1	-	-	0.4	V	V_{CCO} = 4.75V
		Full	4	-	-	-	V	I_{ol} = 1mA
Output current high	I_{oh}	+25°C	1	-	-	-400	µA	V_{CCO} = 4.75V
		Full	4	-	-	-	-	
Output current low	I_{ol}	+25°C	1	-	-	1	mA	V_{CCO} = 4.75V
		Full	4	-	-	-	-	

DC CHARACTERISTICS (cont.)

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Reference voltage								
V_{ref} ladder bottom	VRB	+25°C	1	2.367	2.5	2.671	V	
V_{ref} ladder middle	VRM	+25°C	1	2.848	3.0	3.212	V	
V_{ref} ladder top	VRT	+25°C	1	3.337	3.5	3.763	V	

AC CHARACTERISTICS

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Switching performance								
Clock high pulse width	$T_{pw}1$	+25°C	4	5.7	-	-	ns	
Clock low pulse width	$T_{pw}0$	+25°C	4	5.7	-	-	ns	
Max. conversion rate	F_{max}	+25°C	1	90	-	-	MHz	
Data output setup time	T_{setup}	+25°C	4	4	6	8	ns	Cload=10pF
Data output hold time	T_{hold}	+25°C	4	3	6	8	ns	Cload=10pF
Aperture delay	T_{ad}	+25°C	4	2	3	4	ns	
Aperture delay matching	$T_{ad\delta}$	+25°C	4	-	0.25	0.5	ns	
Aperture jitter	T_{aj}	+25°C	4	10	25	50	ps rms	
Dynamic performance								
Differential non-linearity	DNL	+25°C	4	–0.95	-	+1.2	LSB	F_{CLK} = 90.11MHz
Integral non-linearity	INL	+25°C	4	-	-	±1	LSB	
Signal to noise ratio	SNR	+25°C	1	31.8	-	-	dB	
Total harmonic distortion	THD	+25°C	4	40	-	-	dBc	
Effective No. of bits	ENOB	+25°C	1	5.0	5.6	-	bits	F_{IN} = 11.26MHz
Crosstalk rejection	CTR	+25°C	5	-	50	-	dBc	
Input offset	V_{os}	+25°C	1	-	±0.5	±1	LSB	
Error rate	BER	+25°C	5	-	$10e^{-8}$	-		

NOTES
1. An input voltage of 0.0 volts ±0.5 LSB should nominally correspond to the '011111' to '100000'B transition edge.

TEST LEVELS
Level 1 - 100% production tested.
Level 2 - 100% production tested at 25°C and sample tested at specified temperatures.
Level 3 - Sample tested only.
Level 4 - Parameter is guaranteed by design and characterisation testing.
Level 5 - Parameter is typical value only.

Code	Input Voltage	Digital Output
	2.0 Volt Full Scale	Binary
00	Least positive valid input	000000
01	-	000001
●	●	●
31	-	011111
32	0	100000
33	-	100001
●	●	●
62	-	111110
63	Most positive valid input	111111

Table 1: Output coding

PIN DESCRIPTIONS - 28 Pin Plastic SO Package

Pin	Name	Description
1	CLKIN	TTL clock input
2	V_{CCD}	Digital voltage supply for ADC's and input clock
3	DGND	Digital ground
4	VRT	Reference voltage- ladder top
5	COMPA	Capacitor compensation - A channel
6	VINA	Analog signal input - A channel
7	AGND	Analog ground
8	V_{CCA}	Analog voltage supply for drivers and references
9	VRM	Reference voltage- ladder middle
10	COMPB	Capacitor compensation - B channel
11	VINB	Analog signal input - B channel
12	VRB	Reference voltage- ladder bottom
13	N.C.	Not connected
14	N.C.	Not connected
15	DB0	TTL digital output - channel B - LSB
16	DB1	
17	DB2	
18	DB3	
19	DB4	
20	DB5	TTL digital output - channel B - MSB
21	V_{CCO}	Output voltage supply for TTL data outputs
22	OGND	Output ground
23	DA0	TTL digital output - channel A - LSB
24	DA1	
25	DA2	
26	DA3	
27	DA4	
28	DA5	TTL digital output - channel A - MSB

Table 2: Pin descriptions

ELECTRICAL CHARACTERISTICS DEFINITIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency, as determined by FFT analysis is reduced by 3dB.

Aperture Delay

The delay between the rising edge of the 90MHz clock signal and the instant the analog input signal is sampled.

Aperture Jitter

The sample to sample variation in aperture delay.

Bit Error Rate (BER)

The number of spurious code errors produced for any given input sinewave frequency at a given clock frequency. In this case it is the number of codes occurring outside the histogram cusp for a 1/2 FS sinewave.

Data Outputs, Set-up and Hold Time

Data output timings are measured from the 50% threshold to the 50% threshold on the rising edge of the output clock.

Differential Non-linearity

The deviation in any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)

This is a measure of a device's dynamic performance and may be obtained from the SNR or from a sine wave curve test fit according to the following expressions:

ENOB = SNR-1.76/6.02 or

ENOB = N-log2[rms error (actual)/rms error (ideal)]

where N is the conversion resolution and the actual rms error is the deviation from an ideal sine wave, calculated from the converter outputs with a sine wave input.

Integral Non-linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

Signal-to-Noise Ratio (SNR)

The ratio of the rms signal amplitude to the rms value of 'noise' which is defined as the sum of all other spectral components, including the harmonics, but excluding D.C. with a full-scale analog input signal.

Device Description

The VP211 is a dual 90MHz 6-bit ADC system, (see Fig.2). Included on chip is a high bandwidth ADC driver amplifier, a 6-bit analog to digital converter, latches and TTL compatible data outputs. The VP211 also has the necessary bias voltages for the reference resistor chain in the 'flash' architecture of the ADC.

Analog Input

The analog inputs, (VIN_A,B) are A.C. coupled into the non-inverting input of the ADC driver amplifiers, which provide the necessary bandwidth, gain, offset and low impedance required to drive the ADC. The amplifier has been designed so that an input of 0 volts will produce an output level equal to the voltage present at the middle of the ADC resistor chain, VRM (3.00V typ.). This is achieved by an internal feedback loop within each amplifier which compares the amplifier output with VRM, (see Fig.3). This voltage will produce a transition binary code of 011111 to 100000 at the output of the ADC.

Reference Voltage

An on chip band gap voltage reference circuit combined with two op-amps provides all the necessary bias voltages for the ADC reference resistor chain, bottom (VRB), middle (VRM) and top(VRT). VRB, VRM and VRT have been brought out to pins 12, 9 and 4 respectively and should be decoupled with 100nF capacitors close to the package pins.

ADC Circuit

The VP211 employs a 'flash' architecture consisting of a reference resistor chain, an array of 64 comparators, encoding logic and a 6-bit latch. The 63 reference levels generated by the resistor chain are compared with the analog output signal from the ADC driver amplifier using the comparator array. This produces a thermometer code which the encoding logic converts into a 6-bit word.

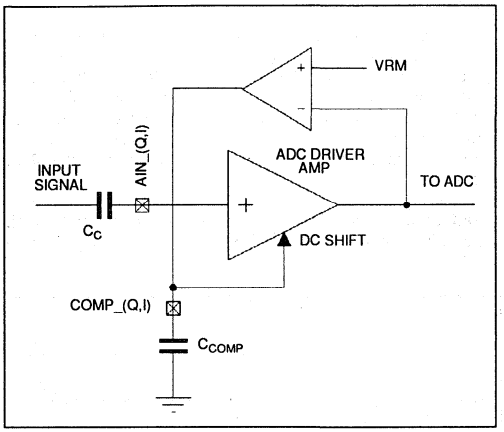


Fig.3 DC offset internal feedback loop

Digital Interface

The TTL data output pins, (DA0-DA5) and (DB0-DB5), have been optimized to interface with devices in close proximity to the VP211 and are designed to provide satisfactory logic levels at speeds up to 90MHz into a fanout of one and a total load capacitance of 10pF. All data outputs should have approximately equivalent loading to ensure proper setup and hold times. For capacitive loads in excess of 10pF, output buffers are recommended.

Clock Interface

The clock signal to the ADC synchronizes the sampling, conversion and output stages of the device as shown in the timing diagram (see Fig.4). The output of the ADC driver amp is sampled when the comparator array is latched on the rising edge of the input clock. Data is then presented to the TTL data outputs and latched on the falling edge of the input clock.

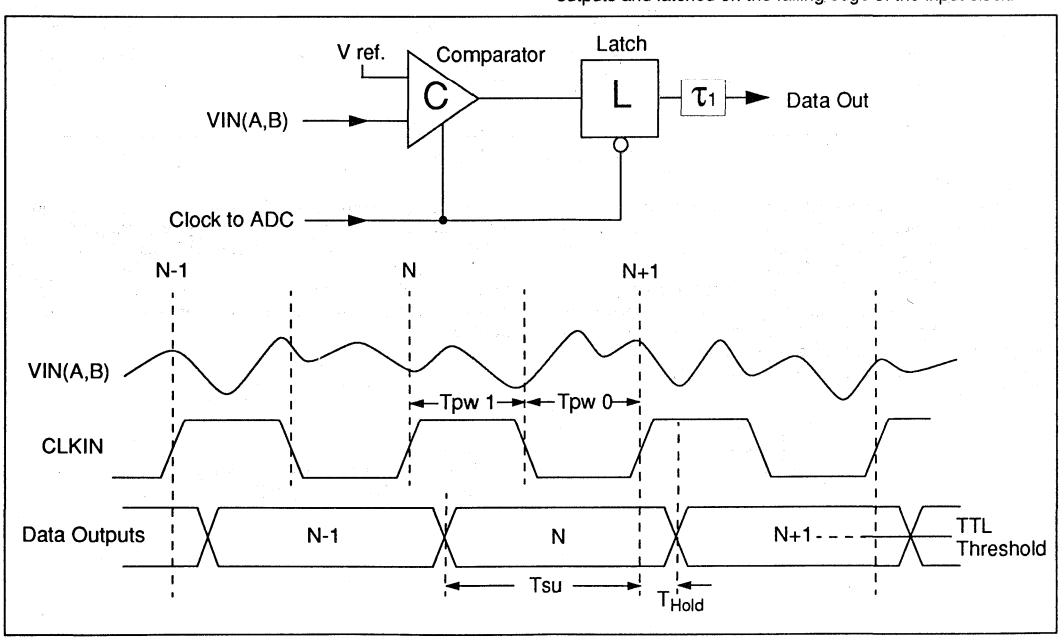


Fig.4 System timing diagram

Layout And Grounding

As with all high speed A to D converters, careful consideration must be given to the PCB layout. High performance can be obtained from the VP211 by tying all grounds to a solid low impedance ground plane. Separate analog and digital ground planes with a single common link under the device can also be used to help reduce the amount of digital noise fed back into the analog section of the converter.

The VP211 should be decoupled with low impedance 100nF ceramic capacitors close to the package pins to avoid lead inductance effects and the decoupling on supply lines should further be improved by using a 47µF tantalum capacitor in parallel with a 100nF ceramic capacitor. If VCCA is derived from VCCD, a small inductor should be used to reduce digital noise on the analog power supply. Jitter and noise on clock input pins must be minimised. Long clock lines should therefore be avoided and all clock lines correctly terminated. Cross talk of digital signals to the analog inputs must also be prevented as sampling cross talk produces DC offsets on the sampled data, for this reason analog inputs should not be run next to clock or data lines. Device connections to the ground plane should be as short as possible.

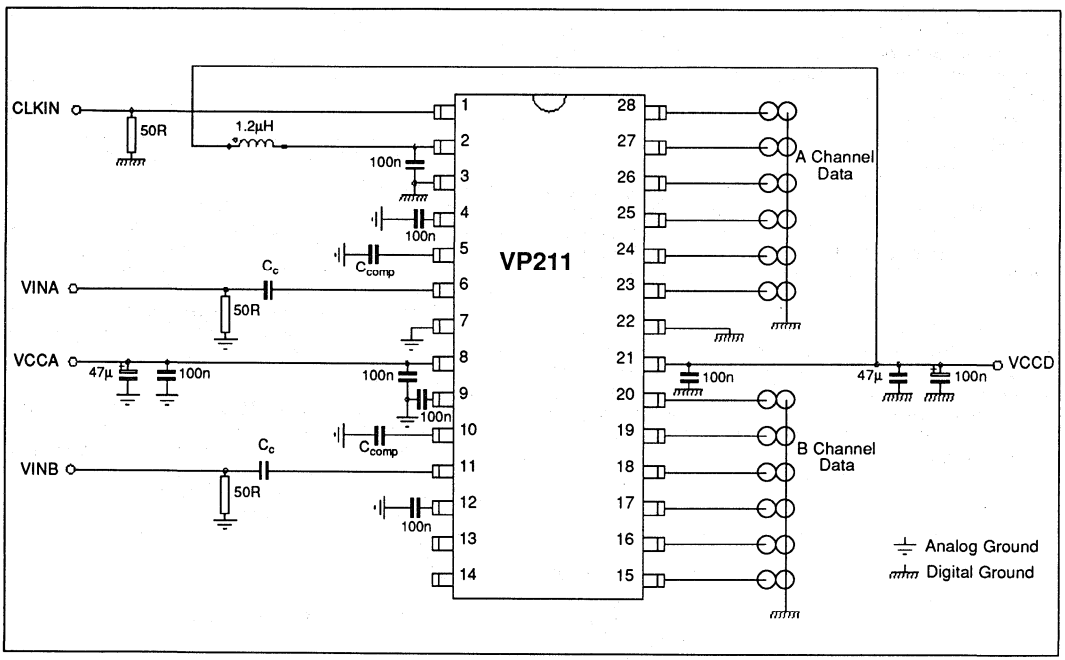


Fig.5 Applications diagram

Application Circuit

Fig.5 shows a typical applications circuit for the VP211. The supply connections are made using separate low noise digital and analog power supplies and VCCD is further isolated from VCCO using a 1.2µH inductor.

The COMPA and COMPB pins must be decoupled to reduce any ripple at low frequencies which may distort the ADC driver amplifier output, (see Fig.2.) The decoupling capacitor value is determined by the required low frequency performance of the system and can be obtained from the following equation.

$$C_{Comp} = \frac{75 \times 10^{-6}}{F_{in} \times V_{Ripple}}$$

A ripple voltage ≤ 10mV is recommended for good system performance, e.g. If the analog input frequency F_{in}= 10KHz a value of 0.75µF is required for C_{Comp}.

To ensure effective A.C. coupling at low input frequencies, the coupling capacitors on pins 6 and 11 can be calculated from the high pass filter corner frequency equation,

$$F_c = \frac{1}{2 \times \pi \times RC}$$

where
F_c = Lower -3dB corner frequency
(R = Input Resistance, 25K typ. - 20K min)

VP213

DUAL 90MHz 6-BIT ANALOG TO DIGITAL CONVERTER

The VP213 is a dual 90MHz 6-bit Analog to Digital Converter designed for use in consumer satellite receivers and decoders, video systems, multimedia and communications applications.

Operating from a single +5V supply, the VP213 includes an on-chip high bandwidth ADC driver amplifier, a 6-bit ADC and digital I/O that can be interfaced to either +5V or +3V. The VP213 also has the necessary bias voltages for the reference resistor chain in the 'flash' architecture of the ADC.

FEATURES

- 90MHz Conversion Rate
- TTL Clock/Data Interface
- 1 Volt Analog Input Range
- Internal ADC Reference
- Digital I/O's compatible with +5V or +3V logic
- Single 5 Volt Supply
- Dual ADC System for good channel matching

APPLICATIONS

- Satellite Decoders
- Multimedia
- Communications

ORDERING INFORMATION

VP213A CG MP1S (Commercial - 28 pin plastic SO)

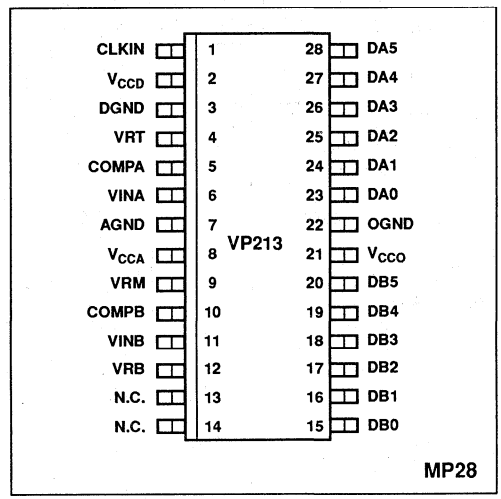


Fig.1 Pin connections - top view (wide body)

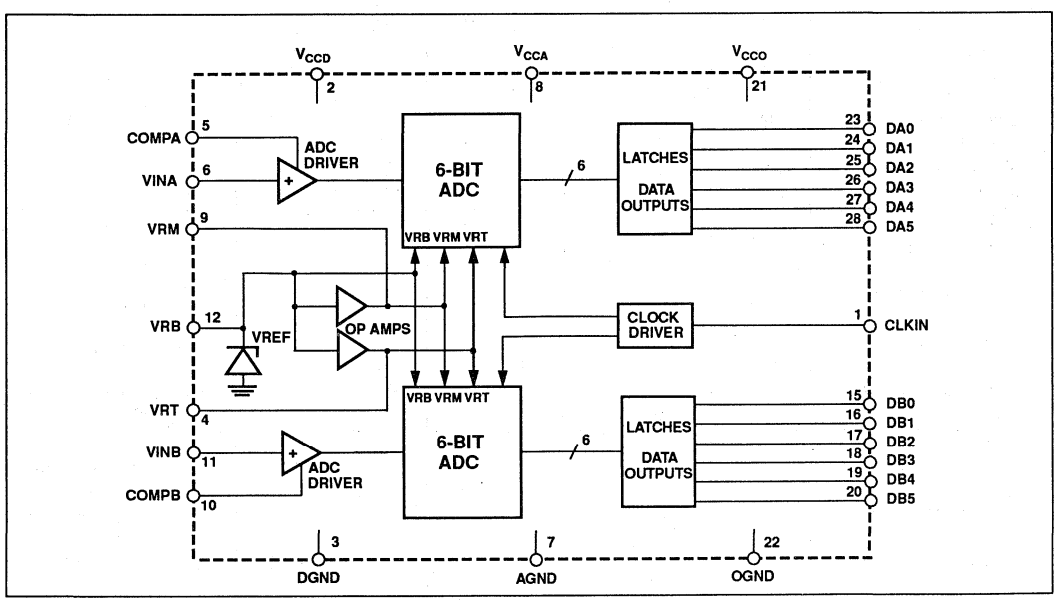


Fig.2 System block diagram

ABSOLUTE MAXIMUM RATINGS

DC supply voltage (V_{CCA}, V_{CCD}, V_{CCO})	-0.3 to+7V
Analog input voltage (VIN)	-0.3 to V_{CC}+0.3V
Digital inputs (CLKIN)	V_{CC}
Digital output current (Ioh, Iol, Isc)	-20 to +20mA
Ambient operating temperature (Tamb)	0°C to +70°C
Storage temperature (Tstorage)	-55°C to +125°C

THERMAL CHARACTERISTICS

THERMAL RESISTANCES

Junction to case(Θjc)	32°C/W
Junction to ambient(Θja)	84°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated) Tamb = 25°C, $V_{CCA/D/O}$ = +5V, full temperature range = 0°C to +70°C

DC CHARACTERISTICS All specifications apply to either of the two ADCs

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Resolution	-	-	-	6	-	-	Bits	
Static performance								
Differential non-linearity	DNL	+25°C	4	-	-	±0.5	LSB	
		Full	4	-	-	±0.5	LSB	
Integral non-linearity	INL	+25°C	4	-	-	±0.5	LSB	
		Full	4	-	-	±0.5	LSB	
No missing codes		Full	4	Guaranteed				
Power supply								
Analog supply voltage	V_{CCA}	Full	4	4.75	5.0	5.25	V	
Digital supply voltage	V_{CCD}	Full	4	4.75	5.0	5.25	V	
Output supply voltage	V_{CCO}	Full	4	4.75	5.0	5.25	V	
Analog supply current	AI_{CC}	+25°C	1	14	19	26	mA	
		Full	4	-	-	-	mA	
Digital supply current	DI_{CC}	+25°C	1	34	42	51	mA	
		Full	4	-	-	-	mA	
Output supply current	OI_{CC}	+25°C	1	3	11	15	mA	
		Full	4	-	-	-	mA	
Power dissipation	PD	+25°C	1	260	360	460	mW	
Analog input								
Input range	V_{in}	Full	5	-	1.0	-	V	Pk to Pk
Input resistance	R_{in}	+25°C	1	20k	25k	30k	Ω	
Input capacitance	C_{in}	+25°C	5	-	4.0	-	pF	
Gain variation	G_V	+25°C	4	-	-	0.25	dB	Fin=300Hz to 20MHz
Gain matching	G_m	+25°C	1	-	-	0.25	dB	Fin=15.36MHz
Input -3dB bandwidth	F3dB	+25°C	4	-	200	-	MHz	
Ain input voltage	Aindc	+25°C	1	3.35	3.6	3.85	V	
Comp output	Vcomp	+25°C	1	1.8	2.0	2.2	V	
CLKIN								
Input voltage high	V_{ih}	+25°C	1	2.0	-	-	V	
		Full	4	-	-	-	V	
Input voltage low	V_{il}	+25°C	1	-	-	0.8	V	
		Full	4	-	-	-	V	
Input current high	I_{ih}	+25°C	1	-	-	1	µA	V_{CCD} = 5.25V
		Full	4	-	-	-		V_{in} = 2.7V
Input current low	I_{il}	+25°C	1	-0.2	-0.35	-0.5	mA	V_{CCD} = 5.25V
		Full	4	-	-	-		V_{in} = 0.4V
TTL digital outputs								
Output voltage high	V_{oh}	+25°C	1	2.4	-	3.0	V	V_{CCO} = 4.75V
		Full	4	-	-	-	V	I_{oh} = 400µA
Output voltage low	V_{ol}	+25°C	1	-	-	0.4	V	V_{CCO} = 4.75V
		Full	4	-	-	-	V	I_{ol} = 1mA
Output current high	I_{oh}	+25°C	1	-	-	-400	µA	V_{CCO} = 4.75V
		Full	4	-	-	-	-	
Output current low	I_{ol}	+25°C	1	-	-	1	mA	V_{CCO} = 4.75V
		Full	4	-	-	-	-	

DC CHARACTERISTICS (cont.)

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Reference voltage								
V_{ref} ladder bottom	VRB	+25°C	1	2.367	2.525	2.671	V	
V_{ref} ladder middle	VRM	+25°C	1	2.848	3.04	3.212	V	
V_{ref} ladder top	VRT	+25°C	1	3.337	3.55	3.763	V	

AC CHARACTERISTICS

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Switching performance								
Clock high pulse width	$T_{pw}1$	+25°C	4	5.7	-	-	ns	
Clock low pulse width	$T_{pw}0$	+25°C	4	5.7	-	-	ns	
Max. conversion rate	F_{max}	+25°C	1	90	-	-	MHz	
Data output setup time	T_{setup}	+25°C	4	4	6	8	ns	Cload=10pF
Data output hold time	T_{hold}	+25°C	4	3	6	8	ns	Cload=10pF
Aperture delay	T_{ad}	+25°C	4	2	3	4	ns	
Aperture delay matching	$T_{ad\delta}$	+25°C	4	-	0.25	0.5	ns	
Aperture jitter	T_{aj}	+25°C	4	10	25	50	ps rms	
Dynamic performance								
Differential non-linearity	DNL	+25°C	4	–0.95	-	+1.2	LSB	F_{CLK} = 90.11MHz
Integral non-linearity	INL	+25°C	4	-	-	±1	LSB	
Signal to noise ratio	SNR	+25°C	1	31.8	-	-	dB	
Total harmonic distortion	THD	+25°C	4	40	-	-	dBc	
Effective No. of bits	ENOB	+25°C	1	5.0	5.6	-	bits	F_{IN} = 11.26MHz
Crosstalk rejection	CTR	+25°C	5	-	50	-	dBc	
Input offset	V_{os}	+25°C	1	-	±0.5	±1	LSB	
Error rate	BER	+25°C	5	-	$10e^{-8}$	-		

NOTES
1. An input voltage of 0.0 volts ±0.5 LSB should nominally correspond to the '011111' to '100000'B transition edge.

TEST LEVELS
Level 1 - 100% production tested.
Level 2 - 100% production tested at 25°C and sample tested at specified temperatures.
Level 3 - Sample tested only.
Level 4 - Parameter is guaranteed by design and characterisation testing.
Level 5 - Parameter is typical value only.

Code	Input Voltage	Digital Output
	1.0 Volt Full Scale	Binary
00	Least positive valid input	000000
01	-	000001
●	●	●
31	-	011111
32	0	100000
33	-	100001
●	●	●
62	-	111110
63	Most positive valid input	111111

Table 1: Output coding

PIN DESCRIPTIONS - 28 Pin Plastic SO Package

Pin	Name	Description
1	CLKIN	TTL clock input
2	V_{CCD}	Digital voltage supply for ADC's and input clock
3	DGND	Digital ground
4	VRT	Reference voltage- ladder top
5	COMPA	Capacitor compensation - A channel
6	VINA	Analog signal input - A channel
7	AGND	Analog ground
8	V_{CCA}	Analog voltage supply for drivers and references
9	VRM	Reference voltage- ladder middle
10	COMPB	Capacitor compensation - B channel
11	VINB	Analog signal input - B channel
12	VRB	Reference voltage- ladder bottom
13	N.C.	Not connected
14	N.C.	Not connected
15	DB0	TTL digital output - channel B - LSB
16	DB1	
17	DB2	
18	DB3	
19	DB4	
20	DB5	TTL digital output - channel B - MSB
21	V_{CCO}	Output voltage supply for TTL data outputs
22	OGND	Output ground
23	DA0	TTL digital output - channel A - LSB
24	DA1	
25	DA2	
26	DA3	
27	DA4	
28	DA5	TTL digital output - channel A - MSB

Table 2: Pin descriptions

ELECTRICAL CHARACTERISTICS DEFINITIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency, as determined by FFT analysis is reduced by 3dB.

Aperture Delay

The delay between the rising edge of the 90MHz clock signal and the instant the analog input signal is sampled.

Aperture Jitter

The sample to sample variation in aperture delay.

Bit Error Rate (BER)

The number of spurious code errors produced for any given input sinewave frequency at a given clock frequency. In this case it is the number of codes occurring outside the histogram cusp for a 1/2 FS sinewave.

Data Outputs, Set-up and Hold Time

Data output timings are measured from the 50% threshold to the 50% threshold on the rising edge of the output clock.

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The deviation in any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)

This is a measure of a device's dynamic performance and may be obtained from the SNR or from a sine wave curve test fit according to the following expressions:

ENOB = SNR-1.76/6.02 or

ENOB = N-log2[rms error (actual)/rms error (ideal)]

where N is the conversion resolution and the actual rms error is the deviation from an ideal sine wave, calculated from the converter outputs with a sine wave input.

Integral Non-linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

Signal-to-Noise Ratio (SNR)

The ratio of the rms signal amplitude to the rms value of 'noise' which is defined as the sum of all other spectral components, including the harmonics, but excluding D.C. with a full-scale analog input signal.

Device Description

The VP213 is a dual 90MHz 6-bit ADC system, (see Fig.2). Included on chip is a high bandwidth ADC driver amplifier, a 6-bit analog to digital converter, latches and TTL compatible data outputs. The VP213 also has the necessary bias voltages for the reference resistor chain in the 'flash' architecture of the ADC.

Analog Input

The analog inputs, (VIN_A,B) are A.C. coupled into the non-inverting input of the ADC driver amplifiers, which provide the necessary bandwidth, gain, offset and low impedance required to drive the ADC. The amplifier has been designed so that an input of 0 volts will produce an output level equal to the voltage present at the middle of the ADC resistor chain, VRM (3.00V typ.). This is achieved by an internal feedback loop within each amplifier which compares the amplifier output with VRM, (see Fig.3). This voltage will produce a transition binary code of 011111 to 100000 at the output of the ADC.

Reference Voltage

An on chip band gap voltage reference circuit combined with two op-amps provides all the necessary bias voltages for the ADC reference resistor chain, bottom (VRB), middle (VRM) and top(VRT). VRB, VRM and VRT have been brought out to pins 12, 9 and 4 respectively and should be decoupled with 100nF capacitors close to the package pins.

ADC Circuit

The VP213 employs a 'flash' architecture consisting of a reference resistor chain, an array of 64 comparators, encoding logic and a 6-bit latch. The 63 reference levels generated by the resistor chain are compared with the analog output signal from the ADC driver amplifier using the comparator array. This produces a thermometer code which the encoding logic converts into a 6-bit word.

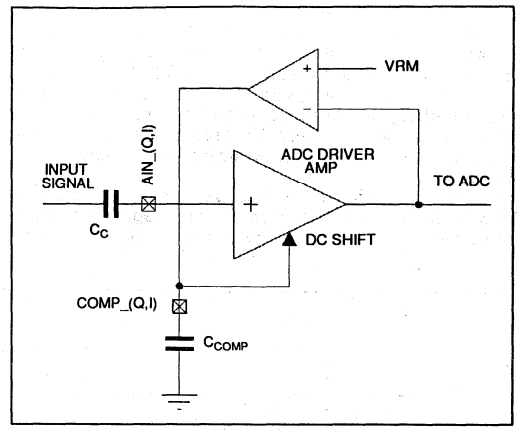


Fig.3 DC offset internal feedback loop

Digital Interface

The TTL data output pins, (DA0-DA5) and (DB0-DB5), have been optimized to interface with devices in close proximity to the VP213 and are designed to provide satisfactory logic levels at speeds up to 90MHz into a fanout of one and a total load capacitance of 10pF. All data outputs should have approximately equivalent loading to ensure proper setup and hold times. For capacitive loads in excess of 10pF, output buffers are recommended.

Clock Interface

The clock signal to the ADC synchronizes the sampling, conversion and output stages of the device as shown in the timing diagram (see Fig.4). The output of the ADC driver amp is sampled when the comparator array is latched on the rising edge of the input clock. Data is then presented to the TTL data outputs and latched on the falling edge of the input clock.

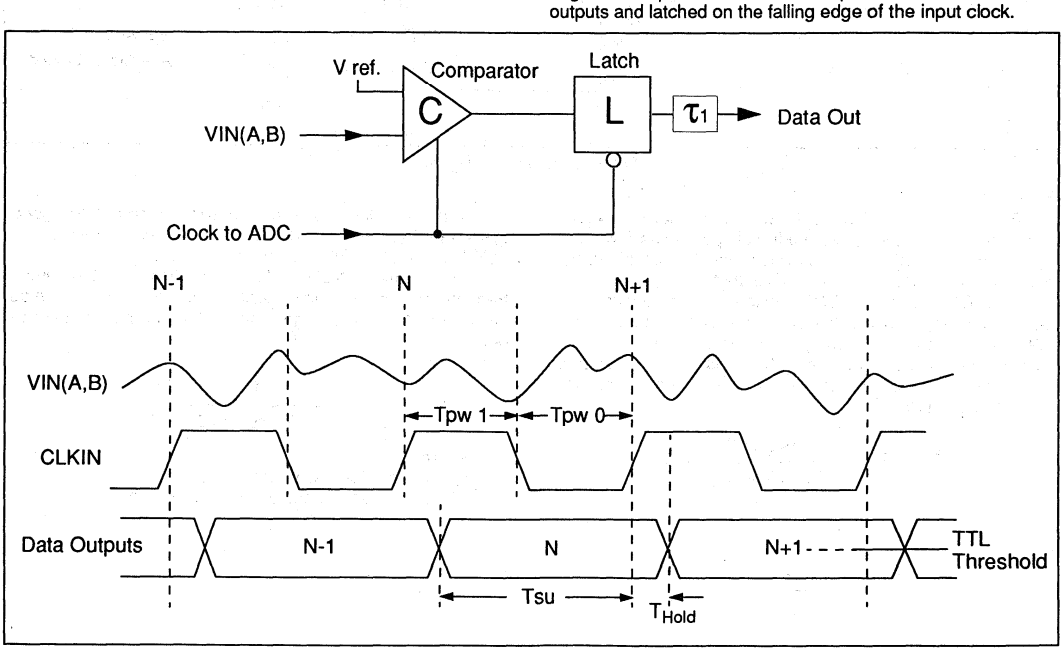


Fig.4 System timing diagram

Layout And Grounding

As with all high speed A to D converters, careful consideration must be given to the PCB layout. High performance can be obtained from the VP213 by tying all grounds to a solid low impedance ground plane. Separate analog and digital ground planes with a single common link under the device can also be used to help reduce the amount of digital noise fed back into the analog section of the converter.

The VP213 should be decoupled with low impedance 100nF ceramic capacitors close to the package pins to avoid lead inductance effects and the decoupling on supply lines should further be improved by using a 47µF tantalum capacitor in parallel with a 100nF ceramic capacitor. If VCCA is derived from VCCD, a small inductor should be used to reduce digital noise on the analog power supply. Jitter and noise on clock input pins must be minimised. Long clock lines should therefore be avoided and all clock lines correctly terminated. Cross talk of digital signals to the analog inputs must also be prevented as sampling cross talk produces DC offsets on the sampled data, for this reason analog inputs should not be run next to clock or data lines. Device connections to the ground plane should be as short as possible.

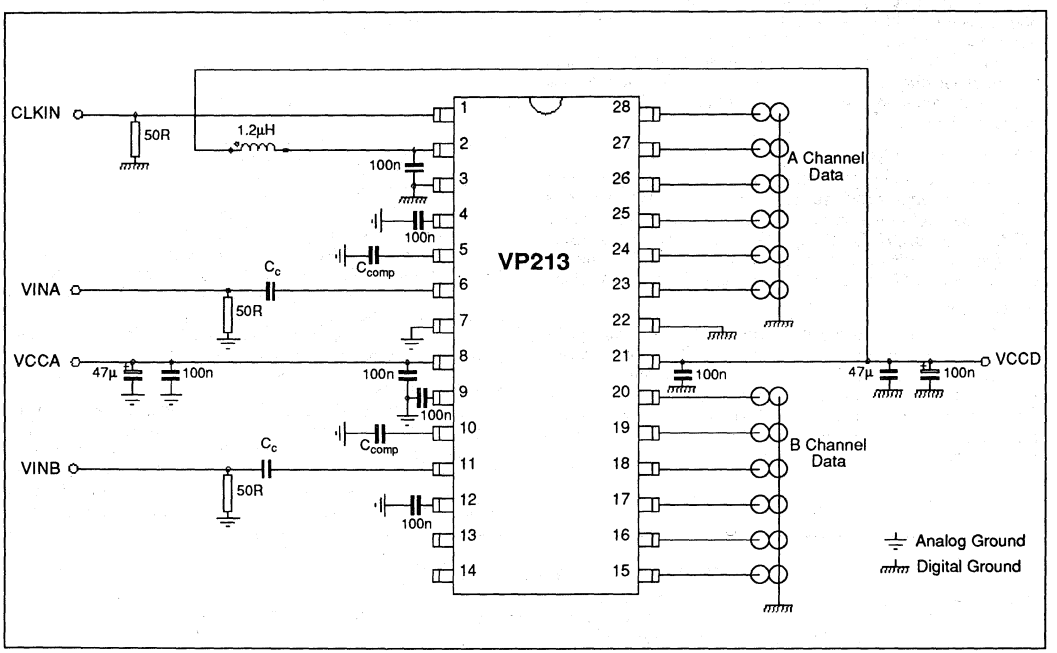


Fig.5 Applications diagram

Application Circuit

Fig.5 shows a typical applications circuit for the VP213. The supply connections are made using separate low noise digital and analog power supplies and VCCD is further isolated from VCCO using a 1.2µH inductor.

The COMPA and COMPB pins must be decoupled to reduce any ripple at low frequencies which may distort the ADC driver amplifier output, (see Fig.2.) The decoupling capacitor value is determined by the required low frequency performance of the system and can be obtained from the following equation.

$$C_{Comp} = \frac{75 \times 10^{-6}}{F_{in} \times V_{Ripple}}$$

A ripple voltage ≤ 10mV is recommended for good system performance, e.g. If the analog input frequency F_{in}= 10KHz a value of 0.75µF is required for C_{Comp}.

To ensure effective A.C. coupling at low input frequencies, the coupling capacitors on pins 6 and 11 can be calculated from the high pass filter corner frequency equation,

$$F_c = \frac{1}{2 \times \pi \times RC}$$

where
F_c = Lower -3dB corner frequency
(R = Input Resistance, 25K typ. - 20K min)

VP215

DUAL 90MHz 6-BIT ANALOG TO DIGITAL CONVERTER

The VP215 is a dual 90MHz 6-bit Analog to Digital Converter designed for use in consumer satellite receivers and decoders, video systems, multimedia and communications applications.

Operating from a single +5V supply, the VP215 includes an on-chip high bandwidth ADC driver amplifier, a 6-bit ADC and digital I/O that can be interfaced to either +5V or +3V. The VP215 also has the necessary bias voltages for the reference resistor chain in the 'flash' architecture of the ADC.

FEATURES

- 90MHz Conversion Rate
- TTL Clock/Data Interface
- 0.5 Volt Analog Input Range
- Internal ADC Reference
- Digital I/O's compatible with +5V or +3V logic
- Single 5 Volt Supply
- Dual ADC System for good channel matching

APPLICATIONS

- Satellite Decoders
- Multimedia
- Communications

ORDERING INFORMATION

VP215A CG MP1S (Commercial - 28 pin plastic SO)

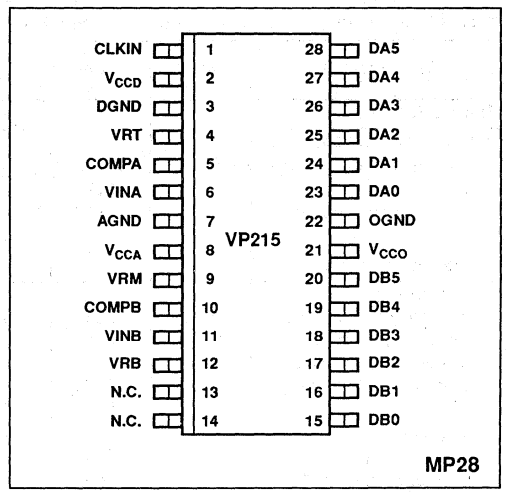


Fig.1 Pin connections - top view (wide body)

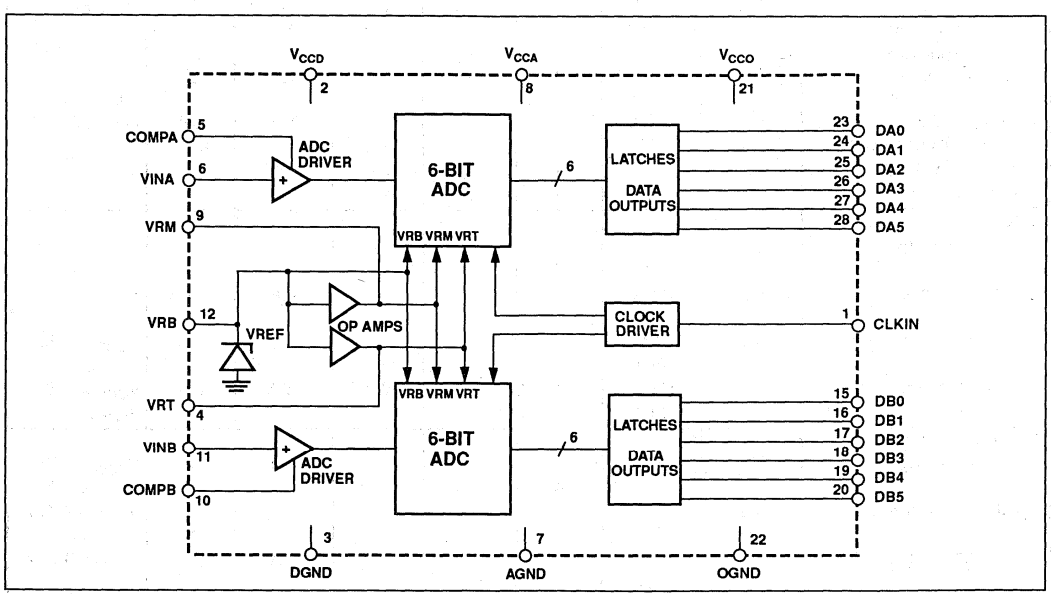


Fig.2 System block diagram

ABSOLUTE MAXIMUM RATINGS

DC supply voltage (V_{CCA}, V_{CCD}, V_{CCO})	-0.3 to+7V
Analog input voltage (VIN)	-0.3 to V_{CC}+0.3V
Digital inputs (CLKIN)	V_{CC}
Digital output current (Ioh, Iol, Isc)	-20 to +20mA
Ambient operating temperature (Tamb)	0°C to +70°C
Storage temperature (Tstorage)	-55°C to +125°C

THERMAL CHARACTERISTICS

THERMAL RESISTANCES

Junction to case(Θjc)	32°C/W
Junction to ambient(Θja)	84°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated) Tamb = 25°C, $V_{CCA/D/O}$ = +5V, full temperature range = 0°C to +70°C

DC CHARACTERISTICS All specifications apply to either of the two ADCs

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Resolution	-	-	-	6	-	-	Bits	
Static performance								
Differential non-linearity	DNL	+25°C	4	-	-	±0.5	LSB	
		Full	4	-	-	±0.5	LSB	
Integral non-linearity	INL	+25°C	4	-	-	±0.5	LSB	
		Full	4	-	-	±0.5	LSB	
No missing codes		Full	4	Guaranteed				
Power supply								
Analog supply voltage	V_{CCA}	Full	4	4.75	5.0	5.25	V	
Digital supply voltage	V_{CCD}	Full	4	4.75	5.0	5.25	V	
Output supply voltage	V_{CCO}	Full	4	4.75	5.0	5.25	V	
Analog supply current	AI_{CC}	+25°C	1	14	19	26	mA	
		Full	4	-	-	-	mA	
Digital supply current	DI_{CC}	+25°C	1	34	42	51	mA	
		Full	4	-	-	-	mA	
Output supply current	OI_{CC}	+25°C	1	3	11	15	mA	
		Full	4	-	-	-	mA	
Power dissipation	PD	+25°C	1	260	360	460	mW	
Analog input								
Input range	V_{in}	Full	5	-	0.5	-	V	Pk to Pk
Input resistance	R_{in}	+25°C	1	20k	25k	30k	Ω	
Input capacitance	C_{in}	+25°C	5	-	4.0	-	pF	
Gain variation	G_V	+25°C	4	-	-	0.25	dB	Fin=300Hz to 20MHz
Gain matching	G_m	+25°C	1	-	-	0.25	dB	Fin=15.36MHz
Input -3dB bandwidth	F3dB	+25°C	4	-	200	-	MHz	
Ain input voltage	Aindc	+25°C	1	3.35	3.6	3.85	V	
Comp output	Vcomp	+25°C	1	1.8	2.0	2.2	V	
CLKIN								
Input voltage high	V_{ih}	+25°C	1	2.0	-	-	V	
		Full	4	-	-	-	V	
Input voltage low	V_{il}	+25°C	1	-	-	0.8	V	
		Full	4	-	-	-	V	
Input current high	I_{ih}	+25°C	1	-	-	1	µA	V_{CCD} = 5.25V
		Full	4	-	-	-		V_{in} = 2.7V
Input current low	I_{il}	+25°C	1	–0.2	–0.35	–0.5	mA	V_{CCD} = 5.25V
		Full	4	-	-	-		V_{in} = 0.4V
TTL digital outputs								
Output voltage high	V_{oh}	+25°C	1	2.4	-	3.0	V	V_{CCO} = 4.75V
		Full	4	-	-	-	V	I_{oh} = 400µA
Output voltage low	V_{ol}	+25°C	1	-	-	0.4	V	V_{CCO} = 4.75V
		Full	4	-	-	-	V	I_{ol} = 1mA
Output current high	I_{oh}	+25°C	1	-	-	-400	µA	V_{CCO} = 4.75V
		Full	4	-	-	-		
Output current low	I_{ol}	+25°C	1	-	-	1	mA	V_{CCO} = 4.75V
		Full	4	-	-	-	-	

DC CHARACTERISTICS (cont.)

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Reference voltage								
V_{ref} ladder bottom	VRB	+25°C	1	2.367	2.525	2.671	V	
V_{ref} ladder middle	VRM	+25°C	1	2.848	3.04	3.212	V	
V_{ref} ladder top	VRT	+25°C	1	3.337	3.55	3.763	V	

AC CHARACTERISTICS

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Switching performance								
Clock high pulse width	$T_{pw}1$	+25°C	4	5.7	-	-	ns	
Clock low pulse width	$T_{pw}0$	+25°C	4	5.7	-	-	ns	
Max. conversion rate	F_{max}	+25°C	1	90	-	-	MHz	
Data output setup time	T_{setup}	+25°C	4	4	6	8	ns	Cload=10pF
Data output hold time	T_{hold}	+25°C	4	3	6	8	ns	Cload=10pF
Aperture delay	T_{ad}	+25°C	4	2	3	4	ns	
Aperture delay matching	$T_{ad\delta}$	+25°C	4	-	0.25	0.5	ns	
Aperture jitter	T_{aj}	+25°C	4	10	25	50	ps rms	
Dynamic performance								
Differential non-linearity	DNL	+25°C	4	–0.95	-	+1.2	LSB	F_{CLK} = 90.11MHz
Integral non-linearity	INL	+25°C	4	-	-	±1	LSB	
Signal to noise ratio	SNR	+25°C	1	31.8	-	-	dB	
Total harmonic distortion	THD	+25°C	4	40	-	-	dBc	F_{IN} = 11.26MHz
Effective No. of bits	ENOB	+25°C	1	5.0	5.6	-	bits	
Crosstalk rejection	CTR	+25°C	5	-	50	-	dBc	
Input offset	V_{os}	+25°C	1	-	±0.5	±1	LSB	
Error rate	BER	+25°C	5	-	$10e^{-8}$	-		

NOTES
1. An input voltage of 0.0 volts ±0.5 LSB should nominally correspond to the '011111' to '100000'B transition edge.

TEST LEVELS
Level 1 - 100% production tested.
Level 2 - 100% production tested at 25°C and sample tested at specified temperatures.
Level 3 - Sample tested only.
Level 4 - Parameter is guaranteed by design and characterisation testing.
Level 5 - Parameter is typical value only.

Code	Input Voltage	Digital Output
	0.5 Volt Full Scale	Binary
00	Least positive valid input	000000
01	-	000001
●	●	●
31	-	011111
32	0	100000
33	-	100001
●	●	●
62	-	111110
63	Most positive valid input	111111

Table 1: Output coding

PIN DESCRIPTIONS - 28 Pin Plastic SO Package

Pin	Name	Description
1	CLKIN	TTL clock input
2	V_{CCD}	Digital voltage supply for ADC's and input clock
3	DGND	Digital ground
4	VRT	Reference voltage- ladder top
5	COMPA	Capacitor compensation - A channel
6	VINA	Analog signal input - A channel
7	AGND	Analog ground
8	V_{CCA}	Analog voltage supply for drivers and references
9	VRM	Reference voltage- ladder middle
10	COMPB	Capacitor compensation - B channel
11	VINB	Analog signal input - B channel
12	VRB	Reference voltage- ladder bottom
13	N.C.	Not connected
14	N.C.	Not connected
15	DB0	TTL digital output - channel B - LSB
16	DB1	
17	DB2	
18	DB3	
19	DB4	
20	DB5	TTL digital output - channel B - MSB
21	V_{CCO}	Output voltage supply for TTL data outputs
22	OGND	Output ground
23	DA0	TTL digital output - channel A - LSB
24	DA1	
25	DA2	
26	DA3	
27	DA4	
28	DA5	TTL digital output - channel A - MSB

Table 2: Pin descriptions

ELECTRICAL CHARACTERISTICS DEFINITIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency, as determined by FFT analysis is reduced by 3dB.

Aperture Delay
The delay between the rising edge of the 90MHz clock signal and the instant the analog input signal is sampled.

Aperture Jitter
The sample to sample variation in aperture delay.

Bit Error Rate (BER)
The number of spurious code errors produced for any given input sinewave frequency at a given clock frequency. In this case it is the number of codes occurring outside the histogram cusp for a 1/2 FS sinewave.

Data Outputs, Set-up and Hold Time
Data output timings are measured from the 50% threshold to the 50% threshold on the rising edge of the output clock.

Differential Non-linearity
The deviation in any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)
This is a measure of a device's dynamic performance and may be obtained from the SNR or from a sine wave curve test fit according to the following expressions:

ENOB = SNR-1.76/6.02 or

ENOB = N-log2[rms error (actual)/rms error (ideal)]

where N is the conversion resolution and the actual rms error is the deviation from an ideal sine wave, calculated from the converter outputs with a sine wave input.

Integral Non-linearity (INL)
The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of 'noise' which is defined as the sum of all other spectral components, including the harmonics, but excluding D.C. with a full-scale analog input signal.

Device Description

The VP215 is a dual 90MHz 6-bit ADC system, (see Fig.2). Included on chip is a high bandwidth ADC driver amplifier, a 6-bit analog to digital converter, latches and TTL compatible data outputs. The VP215 also has the necessary bias voltages for the reference resistor chain in the 'flash' architecture of the ADC.

Analog Input

The analog inputs, (VIN_A,B) are A.C. coupled into the non-inverting input of the ADC driver amplifiers, which provide the necessary bandwidth, gain, offset and low impedance required to drive the ADC. The amplifier has been designed so that an input of 0 volts will produce an output level equal to the voltage present at the middle of the ADC resistor chain, VRM (3.00V typ.). This is achieved by an internal feedback loop within each amplifier which compares the amplifier output with VRM, (see Fig.3). This voltage will produce a transition binary code of 011111 to 100000 at the output of the ADC.

Reference Voltage

An on chip band gap voltage reference circuit combined with two op-amps provides all the necessary bias voltages for the ADC reference resistor chain, bottom (VRB), middle (VRM) and top(VRT). VRB, VRM and VRT have been brought out to pins 12, 9 and 4 respectively and should be decoupled with 100nF capacitors close to the package pins.

ADC Circuit

The VP215 employs a 'flash' architecture consisting of a reference resistor chain, an array of 64 comparators, encoding logic and a 6-bit latch. The 63 reference levels generated by the resistor chain are compared with the analog output signal from the ADC driver amplifier using the comparator array. This produces a thermometer code which the encoding logic converts into a 6-bit word.

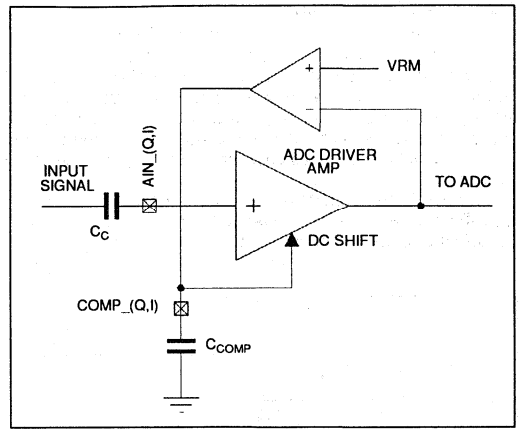


Fig.3 DC offset internal feedback loop

Digital Interface

The TTL data output pins, (DA0-DA5) and (DB0-DB5), have been optimized to interface with devices in close proximity to the VP215 and are designed to provide satisfactory logic levels at speeds up to 90MHz into a fanout of one and a total load capacitance of 10pF. All data outputs should have approximately equivalent loading to ensure proper setup and hold times. For capacitive loads in excess of 10pF, output buffers are recommended.

Clock Interface

The clock signal to the ADC synchronizes the sampling, conversion and output stages of the device as shown in the timing diagram (see Fig.4). The output of the ADC driver amp is sampled when the comparator array is latched on the rising edge of the input clock. Data is then presented to the TTL data outputs and latched on the falling edge of the input clock.

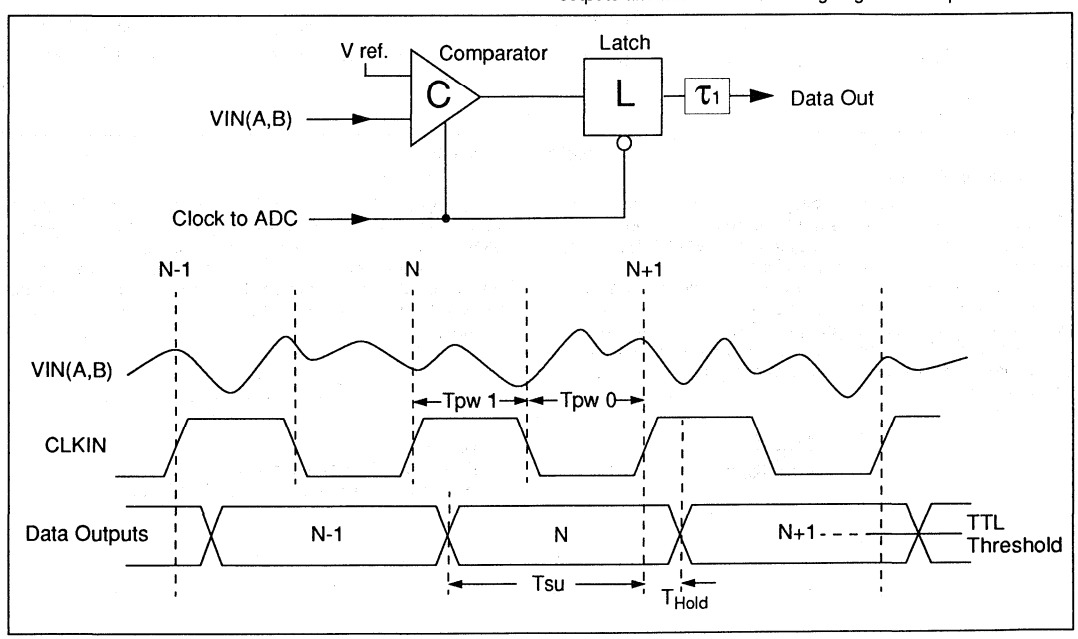


Fig.4 System timing diagram

Layout And Grounding

As with all high speed A to D converters, careful consideration must be given to the PCB layout. High performance can be obtained from the VP215 by tying all grounds to a solid low impedance ground plane. Separate analog and digital ground planes with a single common link under the device can also be used to help reduce the amount of digital noise fed back into the analog section of the converter.

The VP215 should be decoupled with low impedance 100nF ceramic capacitors close to the package pins to avoid lead inductance effects and the decoupling on supply lines should further be improved by using a 47µF tantalum capacitor in parallel with a 100nF ceramic capacitor. If VCCA is derived from VCCD, a small inductor should be used to reduce digital noise on the analog power supply. Jitter and noise on clock input pins must be minimised. Long clock lines should therefore be avoided and all clock lines correctly terminated. Cross talk of digital signals to the analog inputs must also be prevented as sampling cross talk produces DC offsets on the sampled data, for this reason analog inputs should not be run next to clock or data lines. Device connections to the ground plane should be as short as possible.

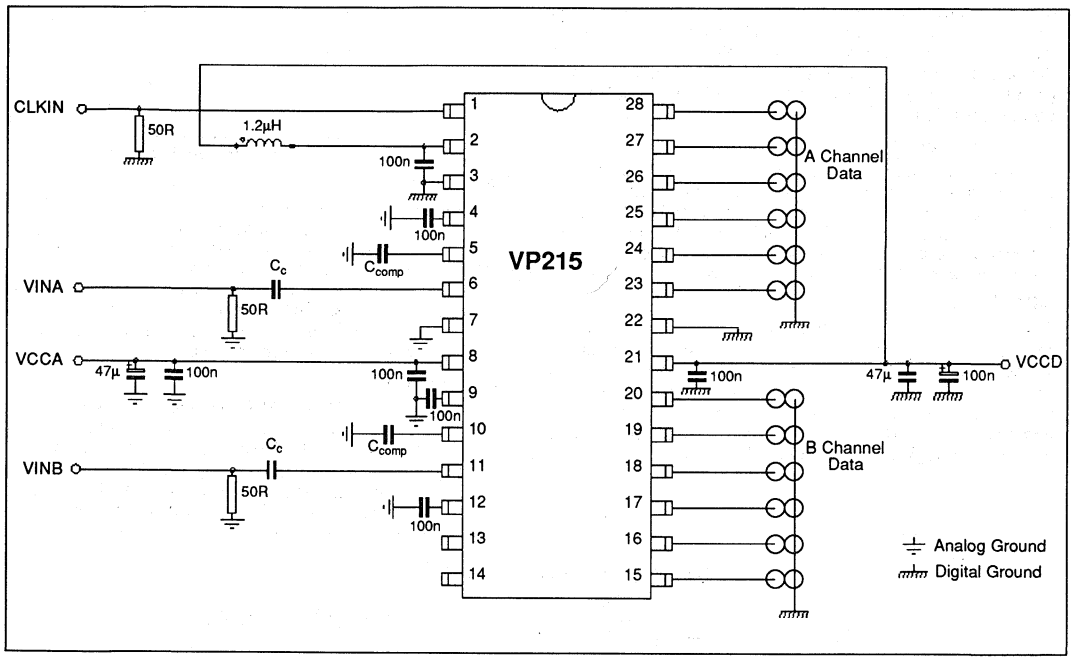


Fig.5 Applications diagram

Application Circuit

Fig.5 shows a typical applications circuit for the VP215. The supply connections are made using separate low noise digital and analog power supplies and VCCD is further isolated from VCCO using a 1.2µH inductor.

The COMPA and COMPB pins must be decoupled to reduce any ripple at low frequencies which may distort the ADC driver amplifier output, (see Fig.2.) The decoupling capacitor value is determined by the required low frequency performance of the system and can be obtained from the following equation.

$$C_{Comp} = \frac{75 \times 10^{-6}}{F_{in} \times V_{Ripple}}$$

A ripple voltage ≤ 10mV is recommended for good system performance, e.g. If the analog input frequency F_{in}= 10KHz a value of 0.75µF is required for C_{Comp}.

To ensure effective A.C. coupling at low input frequencies, the coupling capacitors on pins 6 and 11 can be calculated from the high pass filter corner frequency equation,

$$F_c = \frac{1}{2 \times \pi \times RC}$$

where
F_c = Lower -3dB corner frequency
(R = Input Resistance, 25K typ. - 20K min)

VP216

DUAL 90MHz 6-BIT ANALOG TO DIGITAL CONVERTER WITH VCO

The VP216 is a dual 90MHz 6-bit Analog to Digital Converter designed for use in consumer satellite receivers and decoders, video systems, multimedia and communications applications.

Operating from a single +5V supply, the VP216 includes an on-chip high bandwidth ADC driver amplifier, a 6-bit ADC, VCO or Ext. clock interface. The VP216 also has the necessary bias voltages for the reference resistor chain in the 'flash' architecture of the ADC.

FEATURES

- 90MHz Conversion Rate
- VCO or Ext. Clock Interface
- High Bandwidth ADC Driver Amplifier
- Internal ADC Reference
- TTL Data Outputs
- Single 5 Volt Supply
- Dual ADC System for good channel matching

APPLICATIONS

- Satellite Decoders
- Multimedia
- Communications

ORDERING INFORMATION

VP216A CG HP1S (Commercial - 44 pin PLCC)

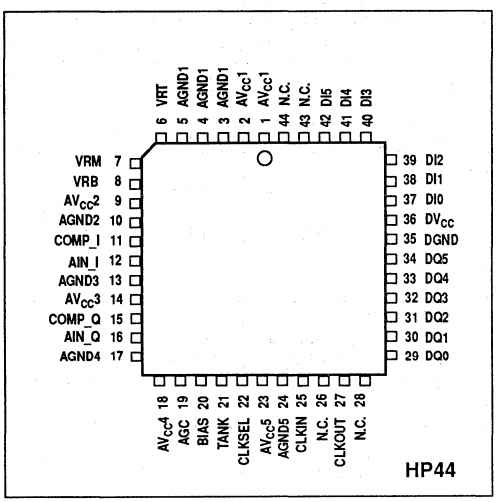


Fig.1 Pin connections - top view

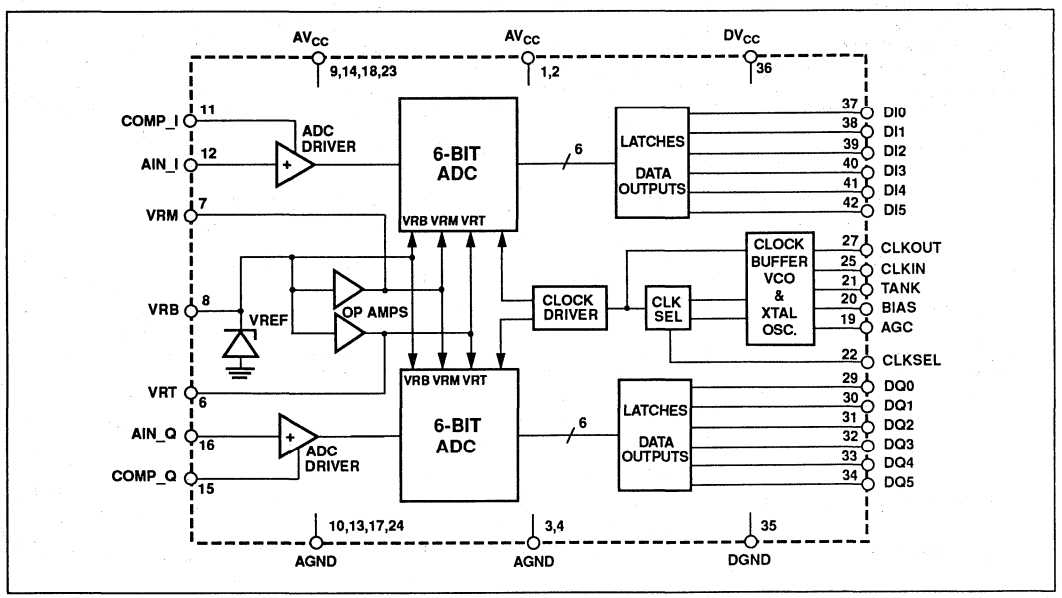


Fig.2 System block diagram

ABSOLUTE MAXIMUM RATINGS

DC supply voltage (V_{CC})	-0.3 to +7V
Analog input voltage (AIN)	-0.3 to V_{CC}+0.3V
Digital inputs (CLKSEL, MSBSEL)	V_{CC}
Digital output current (Ioh, Iol, Isc)	-20 to +20mA
Ambient operating temperature (Tamb)	0°C to +70°C
Storage temperature (Tstorage)	-55°C to +125°C

THERMAL CHARACTERISTICS

THERMAL RESISTANCES

Junction to case(Θjc)	19°C/W
Junction to ambient(ΘjA)	55°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated) Tamb = 25°C, AV_{CC} = DV_{CC} = +5V, full temperature range = 0°C to +70°C

DC CHARACTERISTICS All specifications apply to either of the two ADCs

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Resolution	-	-	-	6	-	-	Bits	
Static performance								
Differential non-linearity	DNL	+25°C	4	-	-	±0.5	LSB	
		Full	4	-	-	±0.5	LSB	
Integral non-linearity	INL	+25°C	4	-	-	±0.5	LSB	
		Full	4	-	-	±0.5	LSB	
Missing codes		Full	4	Guaranteed				
Power supply								
Analog supply voltage	AV_{CC}	Full	4	4.75	5.0	5.25	V	
Digital supply voltage	DV_{CC}	Full	4	4.75	5.0	5.25	V	
Analog supply current	AI_{CC}	+25°C	1	60	72	85	mA	
		Full	4	-	-	-	mA	
Digital supply current	DI_{CC}	+25°C	1	15	23	30	mA	
		Full	4	-	-	-	mA	
Power dissipation	P	+25°C	1	375	475	575	mW	
		Full	4	-	-	-	mW	
Analog input								
Input range	V_{in}	Full	5	-	1.0	-	V	Pk to Pk
Input resistance	R_{in}	+25°C	1	4.5k	5.75k	7.5k	Ω	
Input capacitance	C_{in}	+25°C	5	-	3.0	-	pF	
Gain matching	A_{VH}	+25°C	1	-	-	0.25	dB	
Input -3dB bandwidth	F3dB	+25°C	4	-	200	-	MHz	
Ain input voltage	Aindc	+25°C	1	3.6	3.85	4.1	V	
Comp output	Vcomp	+25°C	1	1.6	1.8	2.0	V	
CLKIN								
Input voltage high	V_{ih}	+25°C	1	2.0	-	-	V	
		Full	4	-	-	-	V	
Input voltage low	V_{il}	+25°C	1	-	-	0.8	V	
		Full	4	-	-	-	V	
Input current high	I_{ih}	+25°C	1	-	-	1	µA	DV_{CC}= 5.25V
		Full	4	-	-	-		V_{in} = 2.7V
Input current low	I_{il}	+25°C	1	–0.2	-	–0.5	mA	DV_{CC}= 5.25V
		Full	4	-	-	-		V_{in} = 0.4V
TTL digital outputs								
Output voltage high	V_{oh}	+25°C	1	2.4	-	3.0	V	DV_{CC} = 4.75V
		Full	4	-	-	-	V	I_{oh} = -400µA
Output voltage low	V_{ol}	+25°C	1	-	-	0.4	V	DV_{CC} = 4.75V
		Full	4	-	-	-	V	I_{ol} = 1mA
Output current high	I_{oh}	+25°C	1	-	-	–400	µA	DV_{CC} = 4.75V
		Full	4	-	-	-	-	
Output current low	I_{ol}	+25°C	1	-	-	1	mA	DV_{CC} = 4.75V
		Full	4	-	-	-	-	

DC CHARACTERISTICS (cont.)

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
CLKSEL								
Input voltage high	V_{ih}	+25°C	1	2.0	-	-	V	
		Full	4	-	-	-	V	
Input voltage low	V_{il}	+25°C	1	-	-	0.8	V	
		Full	4	-	-	-	V	
Input current high	I_{ih}	+25°C	1	-	-	1.0	µA	DV_{CC} = 5.25V
		Full	4	-	-	-		V_{ih} = 2.7V
Input current low	I_{il}	+25°C	1	–50	–100	–150	µA	DV_{CC} = 5.25V
		Full	4	-	-	-		V_{il} = 0.4V
VCO								
Input capacitance	C_{tank}	+25°C	5	-	2.0	-	pF	
Bias voltage	V_{bias}	+25°C	1	1.4	1.6	1.8	V	
AGC voltage	V_{agc}	+25°C	1	1.3	1.65	1.7	V	
Reference voltage								
REF 2.5	VRB	+25°C	1	2.374	2.525	2.677	V	} no load
REF 3.0	VRM	+25°C	1	2.848	3.03	3.212	V	
REF 3.5	VRT	+25°C	1	3.323	3.55	3.747	V	

AC CHARACTERISTICS

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Switching performance								
Clock high pulse width	$T_{pw}1$	+25°C	4	30	50	70	%	Cload=10pF
Clock low pulse width	$T_{pw}0$	+25°C	4	30	50	70	%	Cload=10pF
Max. conversion rate	F_{max}	+25°C	1	90	-	-	MHz	
Data setup time	T_{su}	Full	4	8	10	-	ns	
Data hold time	T_h	Full	4	2	4	-	ns	
Aperture delay	T_{ad}	+25°C	4	2	3	4	ns	
Aperture delay matching	$T_{ad\delta}$	+25°C	4	-	0.2	0.5	ns	
Aperture jitter	T_{aj}	+25°C	4	10	25	50	ps rms	
Dynamic performance								
Differential non-linearity	DNL	+25°C	1	–0.95	-	+1.2	LSB	A_{IN}=15MHz
Integral non-linearity	INL	+25°C	1	-	-	±1	LSB	A_{IN}=15MHz
Signal to noise ratio	SNR	+25°C	1	31.8	-	-	dB	
Total harmonic distortion	THD	+25°C	4	40	-	-	dBc	
Effective No. of bits	ENOB	+25°C	1	5.0	5.5	-	bits	A_{IN}=15MHz
Crosstalk rejection	CTR	+25°C	5	-	50	-	dBc	
Input offset	V_{os}	+25°C	1	-	±0.5	±1	LSB	A_{IN}=15MHz
Error rate	BER	+25°C	5	-	$10e^{-8}$	-		

NOTES
1. An input voltage of 0.0 volts ±0.5 LSB should nominally correspond to the '011111' to '100000'B transition edge.

TEST LEVELS

Level 1 - 100% production tested.

Level 2 - 100% production tested at 25°C and sample tested at specified temperatures.

Level 3 - Sample tested only.

Level 4 - Parameter is guaranteed by design and characterisation testing.

Level 5 - Parameter is typical value only.

PIN DESCRIPTIONS - 44 Pin J-lead PLCC package

Pin	Name	Description
1	AV_{CC} 1	Analog voltage supply for the 6-bit ADCs
2	AV_{CC} 1	Analog voltage supply for the 6-bit ADCs
3	AGND1	Analog ground
4	AGND1	Analog ground
5	AGND1	Analog ground
6	VRT	3.5V reference voltage - ladder top
7	VRM	Reference voltage - ladder middle
8	VRB	2.5V reference voltage - ladder bottom
9	$AV_{CC}2$	Analog voltage supply for the reference bias circuits
10	AGND2	Analog ground
11	COMP-I	Capacitor compensation - I channel
12	AIN-I	Analog signal input - I channel
13	AGND3	Analog ground for the I channel buffer amplifier
14	$AV_{CC}3$	Analog voltage supply for the I channel buffer amplifier
15	COMP-Q	Capacitor compensation - Q channel
16	AIN-Q	Analog signal input - Q channel
17	AGND4	Analog ground
18	$AV_{CC}4$	Analog voltage supply for the Q channel buffer amplifier
19	AGC	AGC control voltage
20	BIAS	Input bias voltage
21	TANK	Tank circuit connection
22	CLKSEL	Clock select - VCO or external clock
23	$AV_{CC}5$	Analog voltage supply for the VCO
24	AGND5	Analog ground
25	CLKIN	Clock input positive
26	N.C.	Not connected
27	CLKOUT	Clock output positive
28	N.C.	Not connected
29	DQ0	Digital TTL output - LSB -Q channel
30	DQ1	
31	DQ2	
32	DQ3	
33	DQ4	
34	DQ5	Digital TTL output - MSB - Q channel
35	DGND	Digital ground
36	DV_{CC}	Digital voltage supply
37	DI0	Digital TTL output - LSB - I channel
38	DI1	
39	DI2	
40	DI3	
41	DI4	
42	DI5	Digital TTL output - MSB - I channel
43	N.C.	Not connected
44	N.C.	Not connected

Table 1: Pin descriptions

Device Description

The VP216 is a dual 90MHz 6-bit ADC system, (see Fig.2). Included on chip is a high bandwidth ADC driver amplifier, a 6-bit analog to digital converter, latches and TTL data outputs. The VP216 also has the necessary bias voltages for the reference resistor chain in the 'flash' architecture of the ADC and has an optional VCO or external oscillator interface.

Analog Input

The analog inputs, (AIN_I,Q) are A.C. coupled into the non-inverting ADC driver amplifiers, which provide the necessary bandwidth, gain, offset and low impedance required to drive the ADC. The amplifier has been designed so that an input of 0 volts will produce an output level equal to the voltage present at the middle of the ADC resistor chain, (VRM = 3V typ.). This is achieved by an internal feedback loop within each amplifier which compares the amplifier output with VRM, (see Fig.3). This voltage will produce a transition binary code of 011111 to 100000 at the output of the ADC.

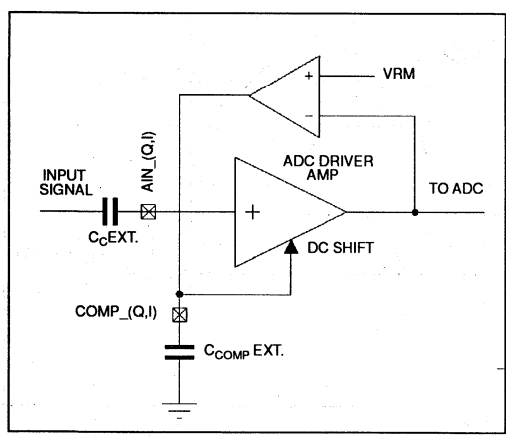


Fig.3 DC offset internal feedback loop.

Reference Voltage

An on chip band gap voltage reference circuit combined with two op-amps provides all the necessary bias voltages for the ADC reference resistor chain, (VRB), (VRM) and (VRT). VRB, VRM and VRT have been brought out to pins 8, 7 and 6 respectively and should be decoupled with 100nF capacitors close to the package pins.

Digital Interface

The TTL data output pins, (DI0-DI5) and (DQ0-DQ5) have been optimized to interface with devices in close proximity to the VP216 and are designed to provide satisfactory logic levels at speeds up to 90MHz into a fanout of one and a total load capacitance of 10pF. All data outputs should have approximately equivalent loading to ensure proper setup and hold timing. For capacitive loads in excess of 10pF, output buffers are recommended.

Clock Interface

The VP216 clock interface allows the ADC to be clocked in a number of ways. With the CLKSEL pin tied low the on chip VCO is selected. With the CLKSEL pin tied high the external TTL clock input is selected.

CLKSEL	Clock Source
1	External Clock
0	VCO

Table 2

The clock signal to the ADC synchronizes the sampling, conversion and output stages of the device as shown in the timing diagram (see Fig.4). The output of the ADC driver amp is sampled when the comparator array is latched after a rising edge of the input clock. Latched data is then presented to the TTL data outputs and latched on the falling edge of the input clock. The clock interface also provides a TTL clock output on pin 27. This output is limited to driving capacitive loads of 10pF. Output buffers are recommended for loads in excess of 10pF.

Code	Input Voltage 1 Volt Full Scale 16mV = 1LSB	Binary
00	Least +Ve Valid Input	000000
01	●	000001
●	●	●
31	●	011111
32	●	100000
33	●	100001
●	●	●
62	●	111110
63	Most +Ve Valid Input	111111

Table 3: Output coding

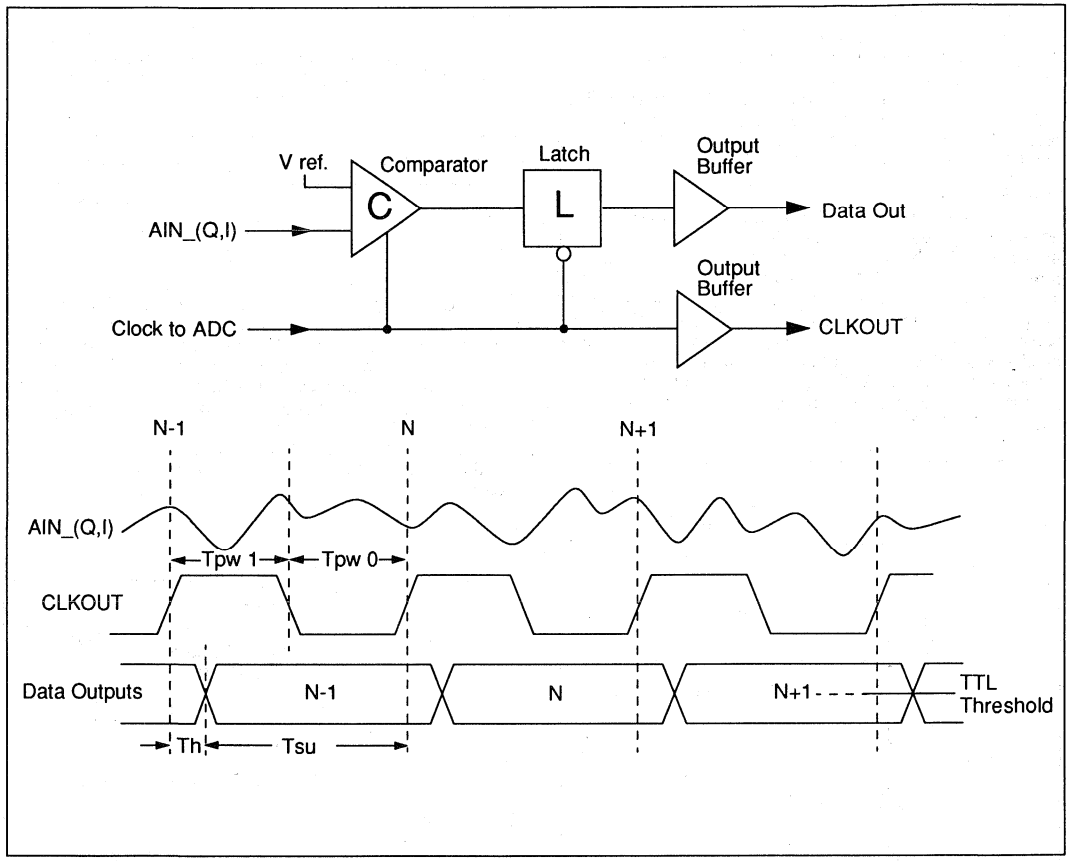


Fig.4 System timing diagram

ELECTRICAL CHARACTERISTICS DEFINITIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency, as determined by FFT analysis is reduced by 3dB.

Aperture Delay

The delay between the rising edge of the 90MHz clock signal and the instant the analog input signal is sampled.

Aperture Jitter

The sample to sample variation in aperture delay.

Bit Error Rate (BER)

The number of spurious code errors produced for any given input sinewave frequency at a given clock frequency. In this case it is the number of codes occurring outside the histogram cusp for a 1/2 FS sinewave.

Data Outputs, Set-up and Hold Time

Data output timings are measured from 2.4V and 0.4V to the 1.4V threshold on the rising edge of the output clock.

Differential Non-linearity

The deviation in any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)

This is a measure of a device's dynamic performance and may be obtained from the SNR or from a sine wave curve test fit according to the following expressions:

$$ENOB = SNR-1.76/6.02 \quad \text{or}$$

$$ENOB = N-\log2[\text{rms error (actual)}/\text{rms error (ideal)}]$$

where N is the conversion resolution and the actual rms error is the deviation from an ideal sine wave, calculated from the converter outputs with a sine wave input.

Integral Non-linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

Signal-to-Noise Ratio (SNR)

The ratio of the rms signal amplitude to the rms value of 'noise' which is defined as the sum of all other spectral components, including the harmonics, but excluding D.C. with a full-scale analog input signal.

SL1461SA

WIDEBAND PLL FM DEMODULATOR

The SL1461SA is a wideband PLL FM demodulator, intended primarily for application in satellite tuners.

The device contains all elements necessary, with the exception of external oscillator sustaining network and loop feedback components, to form a complete PLL system operating at frequencies up to 800MHz.

An AFC with window adjust is provided, whose output signal can be used to correct for any frequency drift at the head end local oscillator.

FEATURES

- Single chip PLL system for wideband FM demodulation
- Simple low component count application
- Allows for application of threshold extension
- Fully balanced low radiation design
- High operating input sensitivity
- Improved VCO stability with variations in supply or temperature
- AGC detect and bias adjust
- 75Ω video output drive with low distortion levels
- Dynamic self biasing analog AFC
- Full ESD protection *

* Normal ESD handling procedures should be observed

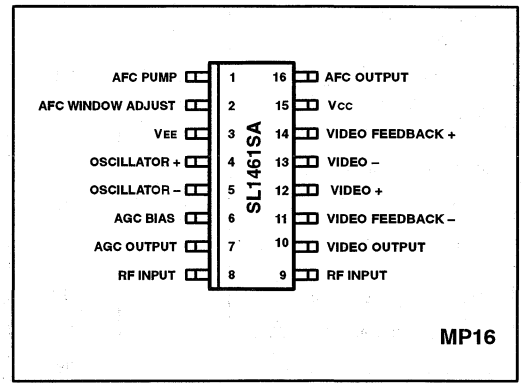


Fig. 1 Pin connections top view

APPLICATIONS

- Satellite receiver systems
- Data communications systems

ORDERING INFORMATION

SL1461SA/KG/MPAS

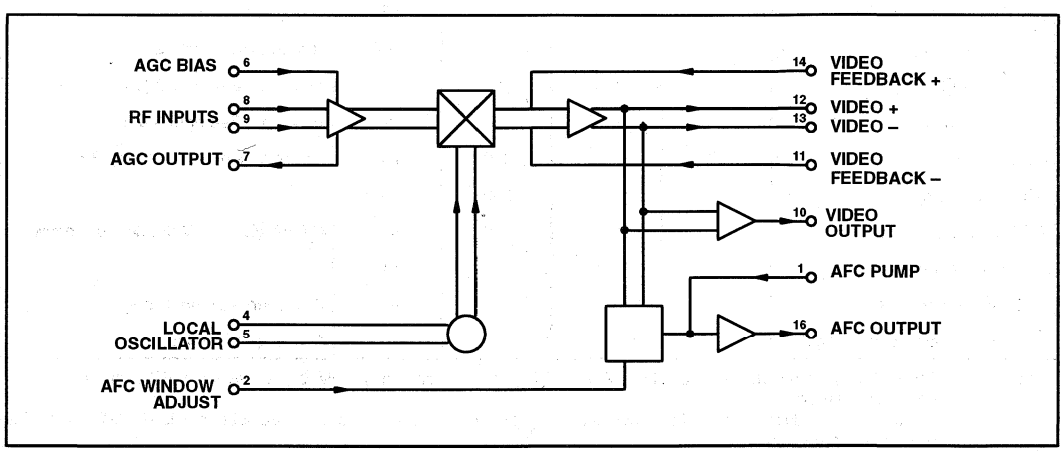


Fig. 2 SL1461SA block diagram

ELECTRICAL CHARACTERISTICS

T_{amb}=–20°C to +80°C, V_{CC}=+4.5V to +5.5V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristics	Value			Units	Conditions
	Min	Typ	Max		
Supply current		36	40	mA	
Operating frequency	300		800	MHz	
Input sensitivity		–40		dBm	Preamp limiting
Input overload	0			dBm	
VCO sensitivity (dF/dV)	25	32	39	MHz/V	Refer to application in Fig. 3
VCO linearity		25		%	Refer to application in Fig. 3; with 13.5MHz p–p deviation
VCO supply stability		2.0		MHz/V	See Note 5
VCO temperature stability		20		KHz/°C	See Note 5
Phase detector gain		0.5 0.25		V/rad V/rad	Differential loop filter Single ended loop filter
Loop amplifier input impedance	450	570	700	Ω	Single ended
Loop amplifier output impedance		25		Ω	Single ended
Loop amplifier open loop gain		38		dB	Single ended
Loop amplifier gain bandwidth product		240		MHz	Single ended
Loop amplifier output swing			1.2	Vp–p	Single ended
Video drive output impedance	55	75	95	Ω	
Video drive;					
Luminance nonlinearity		1.9	5	%	1KΩ load, See note 3 & 4
– differential gain		0.5	2.5	%	75Ω load, See note 3 & 4
– differential phase		1.0	3	Degree	75Ω load, See note 3 & 4
– intermodulation			–40	dB	See notes 1+3 & 4
– Signal/noise	66	72		dB	1KΩ load, See note 2 & 4
–Tilt		0.3	3	%	1KΩ load, See note 3 & 4
– baseline distortion		0.4	2	%	1KΩ load, See note 3 & 4
AGC output current	10		400	μA	Maximum load voltage drop 2V
AGC bias current	0		250	μA	
AFC window current	0		400	μA	400 μA gives 1.5V deadband window
AFC charge pump current		50		μA	
AFC leakage current			10	μA	With charge pump disabled
AFC output saturation voltage			0.4	V	AFC output enabled

Note 1. Product of input modulation f_1 at 4.43MHz, 13.5MHz p–p deviation and f_2 at 6MHz p–p deviation, (PAL chroma and sound subcarriers).

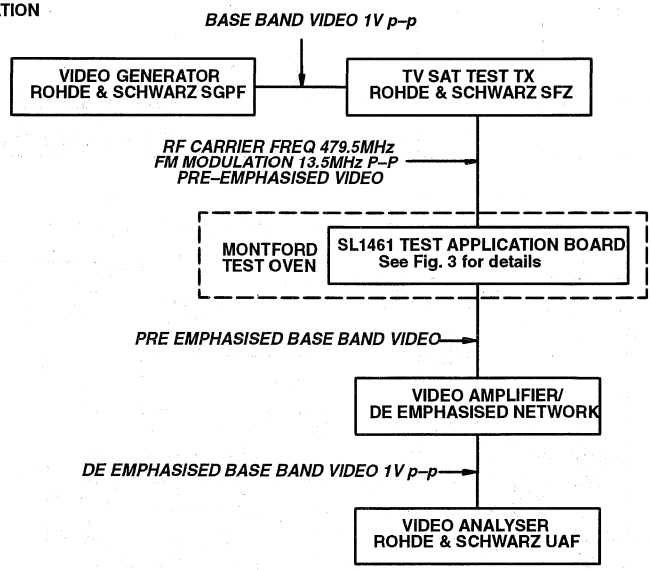
Note 2. Ratio of output video signal with input modulation at 1MHz, 13.5MHz p–p deviation, to output rms noise in 6MHz bandwidth with no input modulation.

Note 3 Input test signal pre–emphasised video 13.5MHz p–p deviation. Output voltage 600mV pk–pk.

Note 4 See page 3

Note 5 Assuming operating frequency of 479.5MHz set with V_{CC} @ 5.0V and ambient temperature of +20°C. Only applies to Application shown in Fig. 3. also refer to Fig. 8.

TEST CONFIGURATION



The video drive characteristics measurements were made using the above test configuration. The maximum figures recorded in the Electrical Characteristics Table coincide with high temperatures and extremes of supply voltage. No adjustment to the recorded figures has been made to compensate for the effects of temperature on the external components of the application test board, in particular the varactor diodes. If operation of the device at high ambient temperatures is envisaged then attention to temperature compensation of the external circuitry will result in performance figures closer to the stated typical figures.

Note 4.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} at 0V.

Characteristic	Min	Max	Units	Conditions
Supply voltage	–0.3	7	V	
RF input voltage		2.5	V p–p	
RF input DC offset	–0.3	V_{CC}+0.3	V	
Oscillator +&–DC offset	–0.3	V_{CC}+0.3	V	
Video +&–DC offset	–0.3	V_{CC}+0.3	V	
Video feedback +&–DC offset	–0.3	V_{CC}+0.3	V	
Video output DC offset	–0.3	V_{CC}+0.3	V	
AFC pump DC offset	–0.3	V_{CC}+0.3	V	
AFC disable DC offset	–0.3	V_{CC}+0.3	V	
AFC deadband DC offset	–0.3	V_{CC}+0.3	V	
AGC bias DC offset	–0.3	V_{CC}+0.3	V	
AGC output DC offset	–0.3	V_{CC}+0.3	V	
Storage temperature	–55	125	°C	
Junction temperature		150	°C	
MP16 package thermal resistance, chip to ambient		111	°C/W	

ABSOLUTE MAXIMUM RATINGS cont.

All voltages are referred to V_{EE} at 0V.

MP16 package thermal resistance chip to case		41	°C/W	
Power consumption at 5.5V		250	mW	
ESD protection – pins 1 to 15	2		kV	Mil–std –883 method 3015 class1
ESD protection – pin 16	1.7		kV	Mil–std –883 method 3015 class1

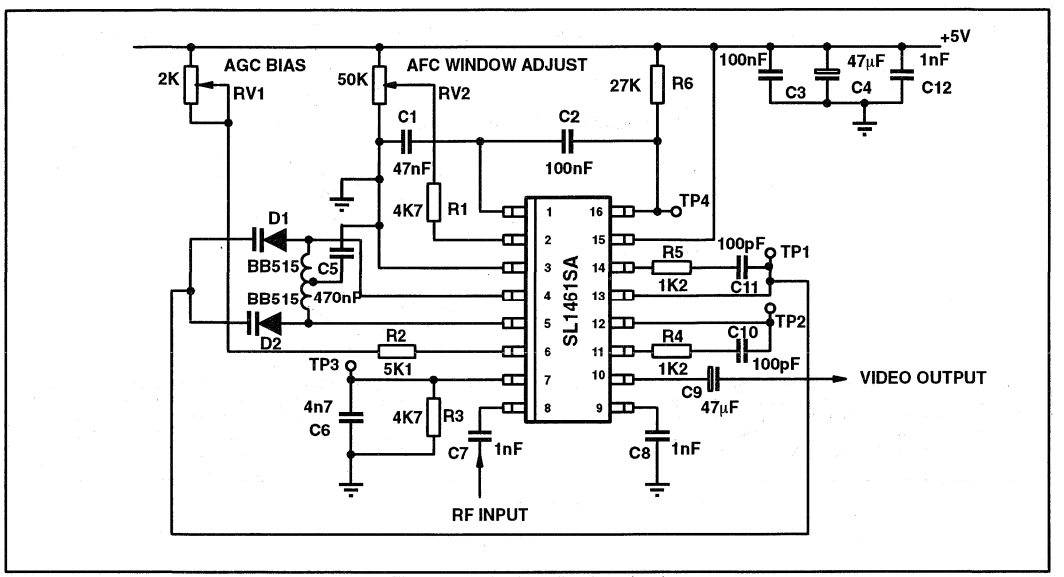


Fig.3. Standard application circuit

FUNCTIONAL DESCRIPTION

The SL1461SA is a wideband PLL FM demodulator, optimised for application in satellite receiver systems and requiring a minimum external component count. It contains all the elements required for construction of a phase locked loop circuit, with the exception of tuning components for the local oscillator, and an AFC detector circuit for generation of error signal to correct for any frequency drift in the outdoor unit local oscillator. A block diagram is contained in Fig. 2 and the typical application in Fig. 3.

The internal pin connections are contained in Fig.6/6a.

In normal applications the second satellite IF frequency of typically 402 or 479.5MHz is fed to the RF preamplifier, which has a working sensitivity of typically –40 dBm, depending on application and layout. The preamplifier contains an RF level detect circuit, which generates an AGC signal that can be used for controlling the gain of the IF amplifier stages, so maintaining a fixed level to the RF input of the SL1461SA, for optimum threshold performance. The bias point of the AGC circuit can be adjusted to cater for variation in AGC line voltage requirement and device input power. The typical AGC curves are shown in Fig. 9. It is recommended that the device is operated with an input signal between –30 and –35dBm. This ensures optimum linearity and threshold performance, and gives a good safety margin over the typical sensitivity of –40dBm.

The output of the preamplifier is fed to the mixer section which is of balanced design for low radiation. In this stage the RF signal is mixed with the local oscillator frequency, which is generated by an on–board oscillator. The oscillator block uses an external varactor tuned sustaining network and is optimised for high linearity over the normal deviation range. A typical frequency versus voltage characteristic for the oscillator is contained in Fig. 7. The loop output is designed to compensate for first order temperature variation effects; the typical stability is shown in Fig. 8

The output of the mixer is then fed to the loop amplifier around which feedback is applied to determine loop transfer characteristic . Feedback can be applied either in differential or single ended mode; if the appropriate phase detector gains are assumed in calculating loop filters, both modes should give the same loop response.

The loop amplifier drives a 75Ω output impedance buffer amplifier, which can either be connected to a 75Ω load or used to drive a high input impedance stage giving greater linearity and approximately 6dB higher demodulated signal output level.

DESIGN OF PLL LOOP PARAMETERS

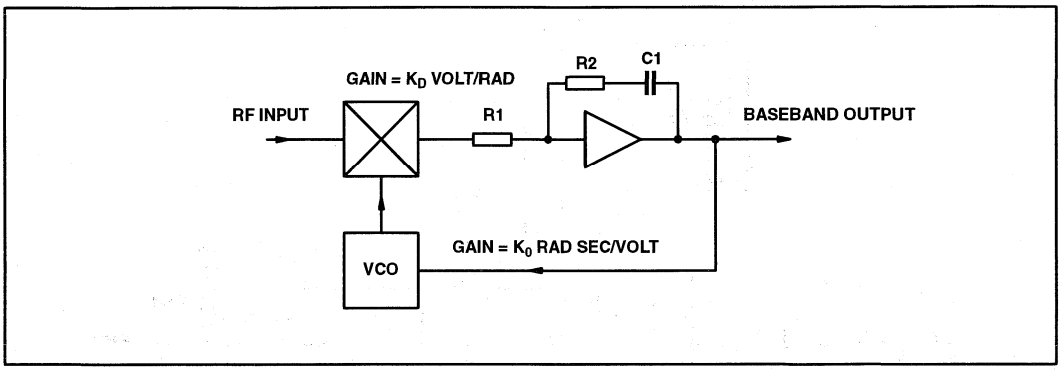


Fig. 4

The SL1461SA is normally used as a type 1 second order loop and can be represented by the above diagram. For such a system the following parameters apply;

$\tau_1 = C1.R1$

$\tau_2 = C1.R2$

and

$$\tau_1 = \frac{K_0 K_D}{\omega_n^2}$$

$$\tau_2 = \frac{2\zeta}{\omega_n}$$

where:
K_0 is the VCO gain in radian seconds per volt
K_D is the phase detector gain in volts per radian
ω_n is the natural loop bandwidth
ζ is the loop damping factor
R1 is loop amplifier input impedance

Note: K_0 is dependant on sensitivity of VCO used.
K_D = 0.25V/rad single ended, 0.5V/rad differential

From these factors the loop 3dB bandwidth can be determined from the following expression;

$$\omega_{3dB}^2 = \omega_n^2(2\zeta^2 + 1) \pm \omega_n^2\sqrt{(2\zeta^2 + 1)^2 + 1}$$

Which approximates to $\omega_{3dB} = 2\omega_n$ when $\zeta = \frac{1}{\sqrt{2}}$

AFC FACILITY

The SL1461SA contains an analog frequency error detect circuit, which generates DC voltage proportional to the integral of frequency error. If the incident RF is high then the AFC voltage increases, if low then the voltage decreases. The AFC voltage can then be converted by an ADC to be read by the micro controller for frequency fine tuning; if used in an I^2C system it is recommended the device is used with either the SP5055 or SP5056 frequency synthesiser which contains an internal ADC readable via the I^2C bus.

The voltage corresponding to frequency alignment is arbitrary and user defined; if used with the SP5055 it is suggested the aligned voltage is 0.375 V_{CC}, corresponding to the centre code of the ADC on port 6.

The AFC detect circuit contains a deadband centred around the aligned frequency. The deadband can be adjusted from zero window to approximately 25MHz width assuming an oscillator dF/dV of 15MHz/V. If the incident RF is within this window the AFC voltage does not integrate, except by component leakage.

With reference to Fig.5; in normal operation the demodulated video is fed to a dual comparator where it is compared with two reference voltages, corresponding to the extremes of the deadband, or window. These voltages are variable and set by the window adjust input.

The comparators produce two digital outputs corresponding to voltages above or below the voltage window, or frequency above or below deadband. These digital control signals are used to control a complimentary current source pump. The current signals are then fed to the input of an amplifier which is arranged as an integrator, so integrating the pulses into a DC voltage.

If the frequency is correctly aligned both the current source and sink are disabled, therefore the DC output voltage remains constant. There will be a small drift due to component leakage; the maximum drift can be calculated from;

$$\frac{dV}{dt} = \frac{I}{2500.C} \quad \text{where } I = \frac{V_{CC}}{R_{EXT}}, \quad C = C_{EXT}$$

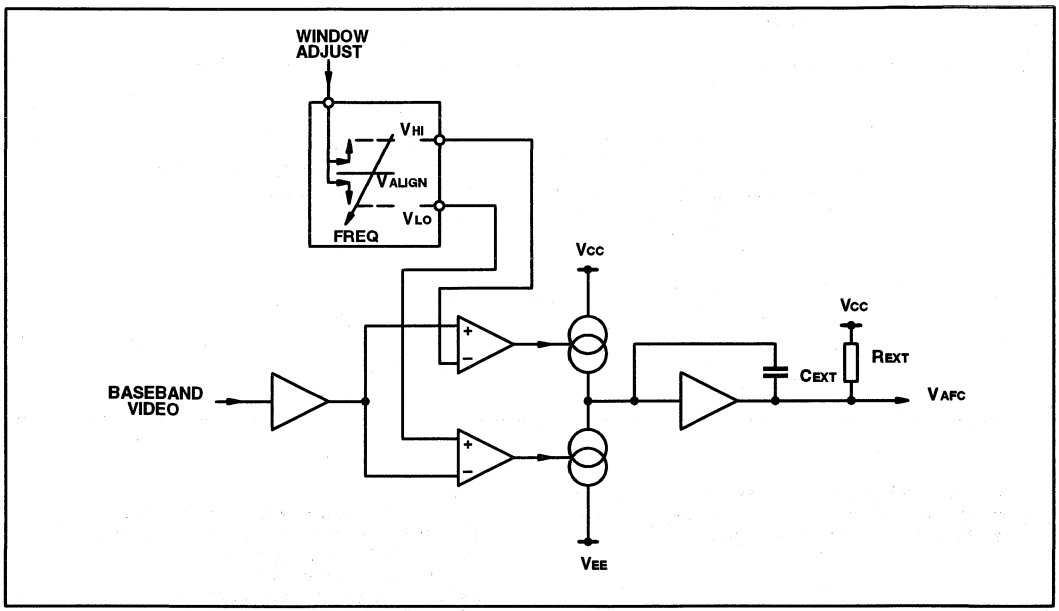
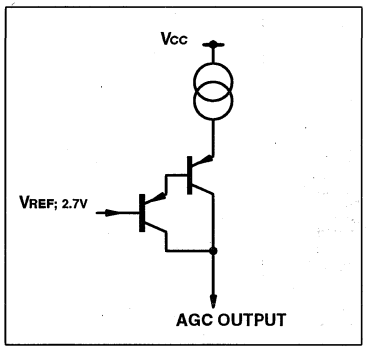
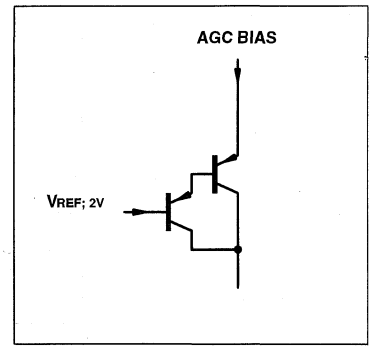


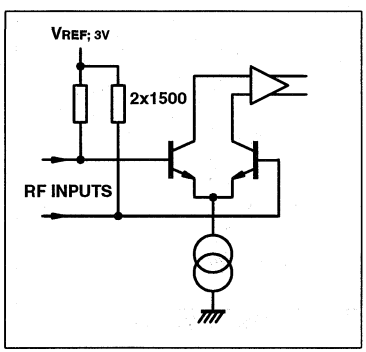
Fig. 5 AFC system block diagram



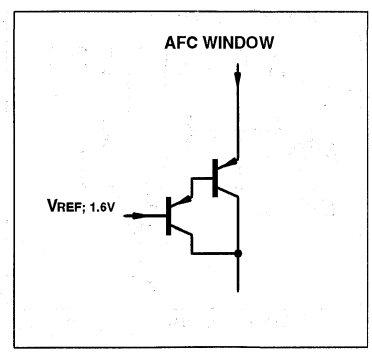
AGC output



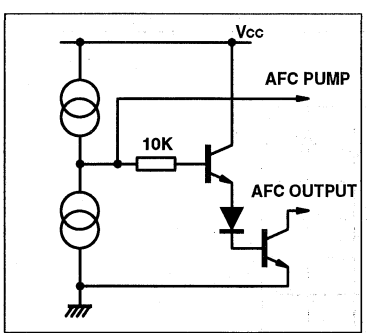
AGC bias adjust



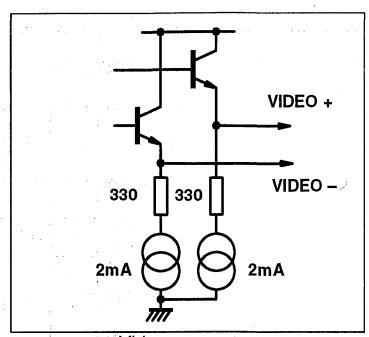
RF inputs



AFC window adjust

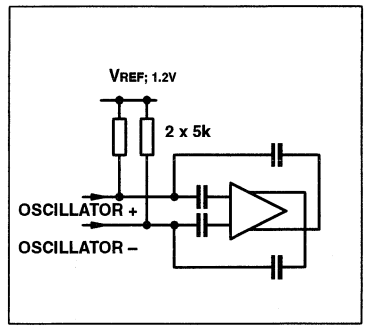


AFC output stage

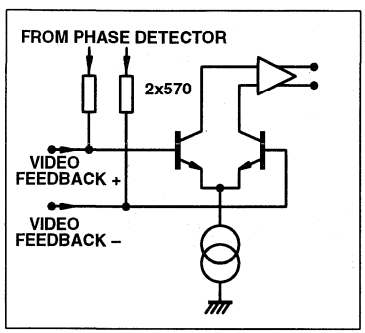


Video amp outputs

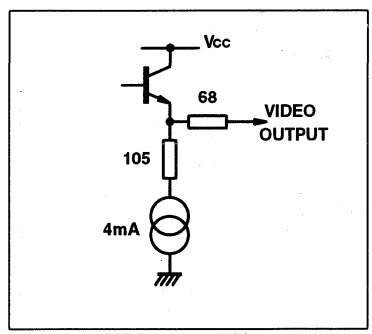
Fig.6 SL1461SA I/O port internal circuitry



Local oscillator



Video amp feedback inputs



Video output drive

Fig. 6a SL1461SA I/O port internal circuitry

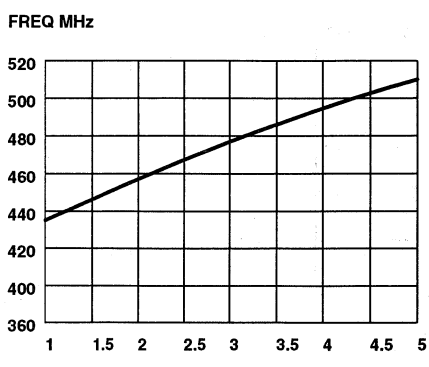


Fig. 7 Typical VCO frequency vs DC control voltage

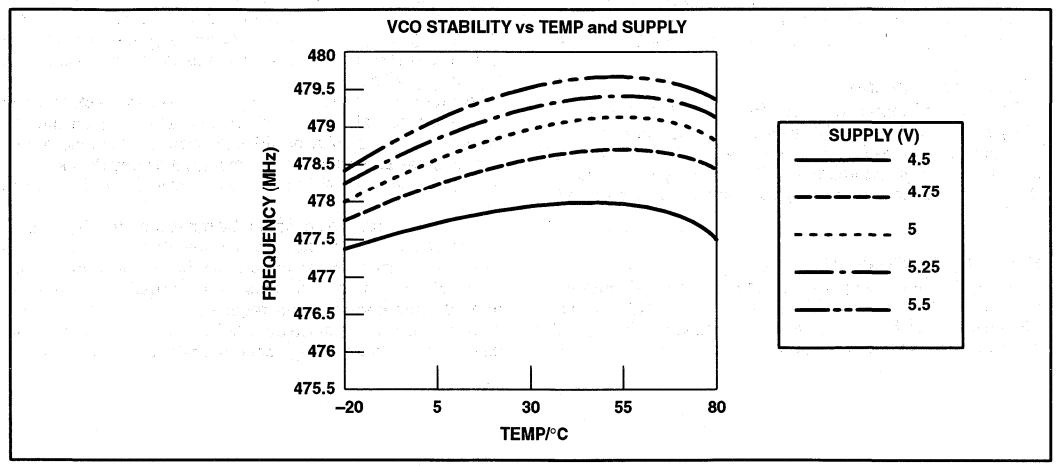


Fig. 8 SL1461SA VCO centre frequency uncompensated temperature stability.

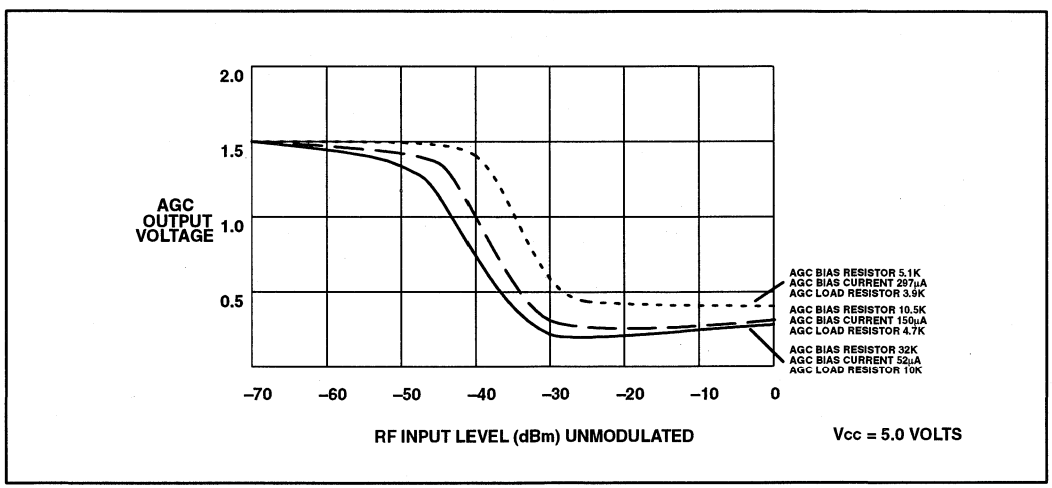


Fig.9 SL1461SA AGC output voltage for differing values of AGC bias resistor

APPLICATION NOTES

Capture range

Under conditions when there is no RF input signal present, the SL1461SA may react to spurious radiation from the free running oscillator coupling into the RF inputs. Because of the constant phase error between the VCO input to the phase detector and the spuriously coupled signal via the RF input, the phase comparator will drive the control voltage to either the bottom or the top of the range.

In such a case, the capture range will be asymmetrical about the VCO free running frequency, since any control voltage will only be able to tune the VCO in one direction if the tuning voltage is already at the max or min.

This effect can be avoided by driving the RF input differentially or achieving good common mode rejection to the VCO signal.

The lock range is independant of the above effects and will be symmetric about the centre of the phase detector S–curve provided the VCO is correctly aligned.

EXAMPLE

Loop out of lock

Tuning voltage =4.3V (maximum)

frequency =520MHz (maximum

It is only possible to capture signals below this frequency since the VCO is already at its maximum frequency.

Testing of capture range should be done with the device operating under normal conditions. An input signal of between –35dBm to –10dBm is suitable for such a measurement.

Lock range

Lock range should be symmetric about the centre of the S–curve. When the oscillator is sitting in the centre of the S–curve, the two video outputs will be at the same DC voltage.

RF oscillator design

The standard application circuit for the SL1461SA is shown in Fig.3 The layout of the VCO tank should follow normal good RF techniques – ie as compact as possible. This will minimise parasitics, thus giving improved VCO linearity and stability. The PCB layout used for testing purpose is shown in Fig. 11.

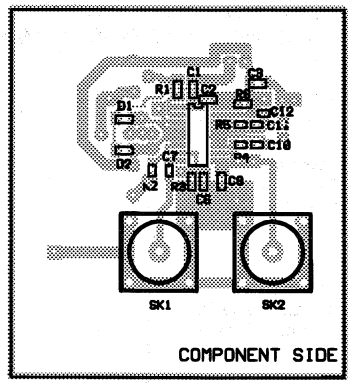
Setting up of oscillator

The VCO should be set up so that the desired input RF frequency is at the centre of the lock range. This will coincide with the centre of the S–curve and the point at which the AFC toggles when set to zero deadband.

The easiest way to centralise the VCO is to input an RF carrier which is being modulated by a low frequency squarewave. The tuning coil(s) should be adjusted until the AFC voltage toggles between 0.2V and $V_{CC-0.7V}$. The smaller the FM deviation of the squarewave used, the more accurate the setting will be.

A pre–emphasised video input containing black to white transitions can also be used for this setting, since the DC content in a pre–emphased video is much less than that in non pre–emphasised video. This is important as any dc content in the input waveform will introduce an offset in the AFC transition point.

The setting can be confirmed by measuring the DC voltage on the two video outputs, the voltages should be the same when the oscillator is centred around the incoming frequency. This DC measurement must be carried out with an unmodulated carrier of the required frequency. Modulation must not be present, since by definition, the dc voltages would be changing, thus making accurate measurement difficult.



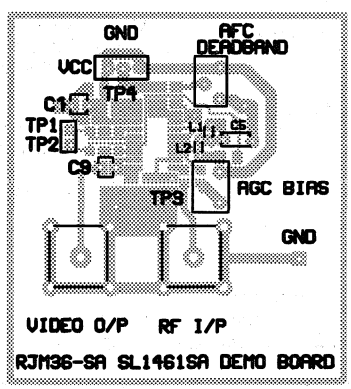


Fig. 11 Layout of demo board with component locations

SL1710

QUADRATURE DOWNCONVERTER

(Supersedes version in October 1995 Media IC Handbook, HB3120–3)

The SL1710 is a quadrature downconverter intended for use with both Professional and Consumer Digital Satellite Applications.

The device contains high linearity, low noise amplifiers, quadrature mixers, plus an on–chip oscillator, operating between 350MHz and 500MHz, which may be synthesised via the differential prescaler outputs.

An AGC with 18dB gain control is provided to cope with a wide range of input signal levels.

I and Q outputs are via low impedance single ended amplifiers. These may be connected to a dual channel analog to digital converter such as the PCA869, 913 and 916 via a suitable anti–alias filter.

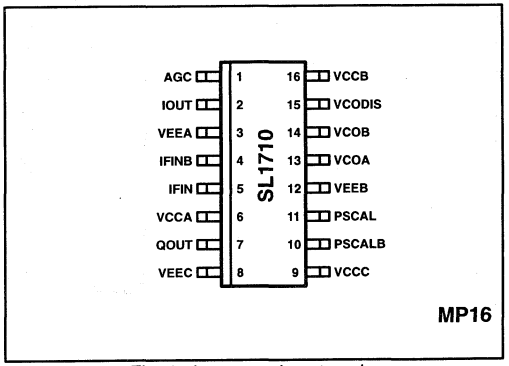


Fig. 1 pin connections top view

FEATURES

- Wide input frequency range (350–500MHz)
- On–chip VCO with quadrature generation, Phase match better than ±2°, gain match better than 1dB
- Nominal 40dB conversion gain from IF input to I and Q outputs
- AGC amplifier with 18dB gain control range
- Low impedance I and Q single ended outputs, with 15MHz ±1dB BW
- Divide by 32 prescaler outputs
- Suitable for QPSK and up to 64QAM systems

APPLICATIONS

- Consumer digital satellite decoders
- Professional digtal satellite decoders
- Communication systems

ORDERING INFORMATION

SL1710/KG/MPAS
SL1710/KG/MPAD (Tape & Reel)

ABSOLUTE MAXIMUM RATINGS

Storage temperature	–55°C to +150°C
Junction temperature	–20°C to +150°C
Supply voltage	–0.3 to +7.0V
Voltage at any other pin	–0.3 to +7.0V

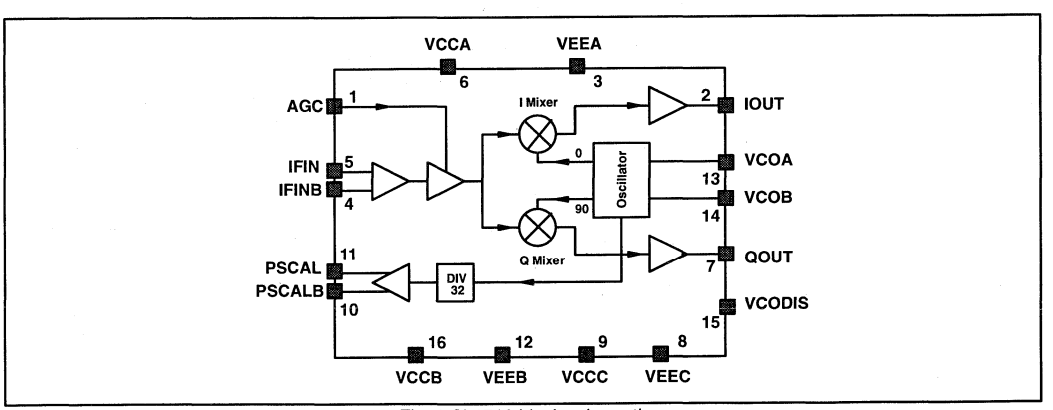


Fig. 2 SL1710 block schematic

ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C, V_{CC} = +4.75 to 5.25 volt. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	6,9,16	4.75		5.25	V	
Supply current	6,9,16		94	110	mA	
RF Input						
RF freq range	4, 5	350		500	MHz	
Impedance	4, 5		75		ohm	@ 480 MHz. Fig. 4.
VSWR	4, 5			1.7		@ 480 MHz. Fig. 4.
Noise Figure	4, 5			19	dB	AGC at maximum gain
Noise Figure variation with gain	4, 5		0.5	1	dB/dB	
VCO						
V_{CO} freq (fo) control range	13, 14	350		500	MHz	External tank circuit with varicap
Phase noise	13, 14			–85	dBc/Hz	@10kHz from fo. but measured in I or Q output. Note (1, 2)
Fo sensitivity to V_{CC}	13, 14			2	MHz/Volt	Fixed external components and no control loop.
Fo sensitivity to temperature	13, 14			40	KHz/°C	Uncompensated.
Prescaler output, VOH	10, 11	V_{CC}–0.96			Volt	At 25°C
VOL	10, 11			V_{CC}–1.65	Volt	
Prescaler output duty cycle	10, 11	40		60	%	Under maximum load conditions Fig. 5
AGC						
Gain, Vagc= +2.5V			40		dB	
Temp stability of gain	1			±2	dB	For any gain setting 0V TO 5V
Gain, Vagc= +0.5V	1	44			dB	See Fig. 6
Gain, Vagc= +V_{CC}–0.5V	1			32	dB	See Fig. 6
AGC range			18		dB	
I Q outputs						480MHz local oscillator, 481 to 495MHz RF input @–51dBV. Gain set to give –11dBV, 1–15MHz baseband output into maximum load. Fig. 7
Output impedance	2, 7			8	ohm	Fig.8
Output clipping level	2, 7	1.5			V p–p	
I phase lag with respect to Q	2, 7	88	90	92	degs	1 –15MHz
IQ crosstalk				20	dB	
Output amplitude match	2, 7			1	dB	I relative to Q, 1–15MHz
Baseband flatness	2, 7			±1	dB	1–15MHz, 1kΩ 15pF load
Two tone 3rd order intercept point	2, 7	+3			dBV	Referred to output. @ 1MHz Output load 1kohm, 15pF, all AGC settings, 0.7V pk–pk output.
Im3	2, 7	28			dBc	
LO, and Spurii in IQ outputs	2, 7			–30	dBV	1–100MHz

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb} = 0°C to +70°C, V_{CC} = +4.75 to 5.25 volt. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Prescaler sidebands	2, 7		–50	–47	dBV	Measured in IQ outputs
Power supply rejection	2, 7	25	30		dB	Attenuation V_{CC} to IQ outputs, over 0–500kHz

Notes:
1. The choice of L will have an effect on phase noise of the VCO
2: Target value at fo=500MHz, L (tank)=10nH, Q (tank, unloaded)=50, SSB

DESCRIPTION

The SL1710 is a quadrature downconverter, intended for high linearity, low noise digital satellite applications. It contains all the elements necessary, with the exception of the VCO tuning components, to extract baseband I and Q signal from a QPSK or QAM IF input signal.

A block diagram for the SL1710 is shown in Fig. 2.

In normal consumer digital satellite applications, the device is fed via a SAW filter, centred at the standard IF of 479.5MHz. A filtered single channel is therefore presented to the device, at a typical level of –51dBV. An AGC is included with 18dB of gain control, which is guaranteed to provide an overall conversion gain between 30 and 45dB from the RF input to the I and Q outputs.

The quadrature mixers are fed from an on–chip oscillator which is centred on the incoming IF. The oscillator external tuning network should be fully symmetric, to ensure optimum gain and phase match.

Single ended I and Q amplifiers are provided, which output a 760mV (p/p) signal, assuming a nominal –51dBV input signal and 40dB gain, suitable for driving a dual channel ADC such as the PCA 869, PCA 913 & PCA 916 via an anti–alias filter (see application notes). The ADC is normally AC coupled via two capacitors (typically 4.7µF).

The SL1710 also includes divide by 32 prescaler output. These may be fed to an external PLL circuit which can be used to drive the on–chip oscillator, thus forming a complete control loop.

The VCO can be disabled by applying 0V to pin 15.

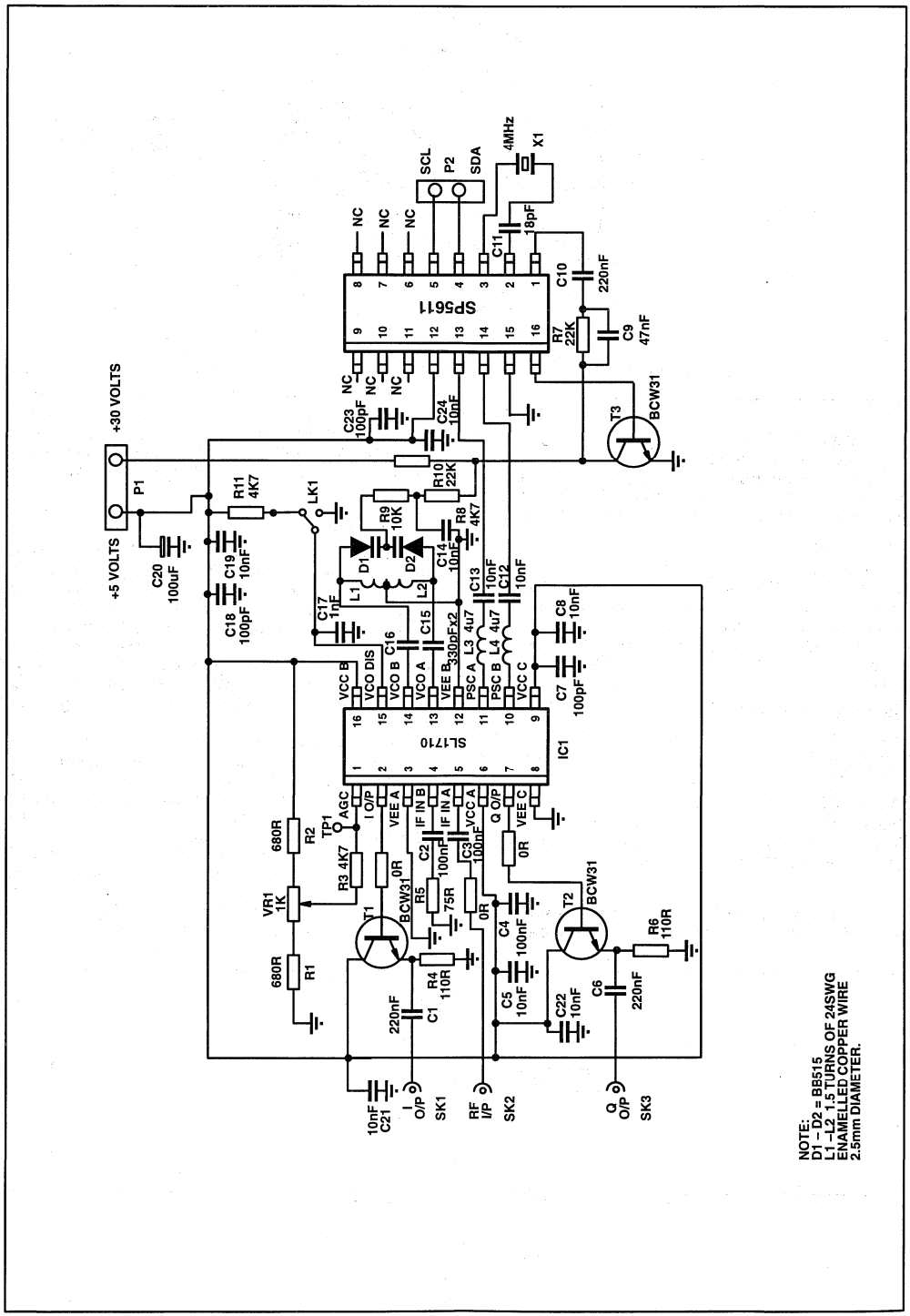


Fig. 3 Demonstration board circuit diagram

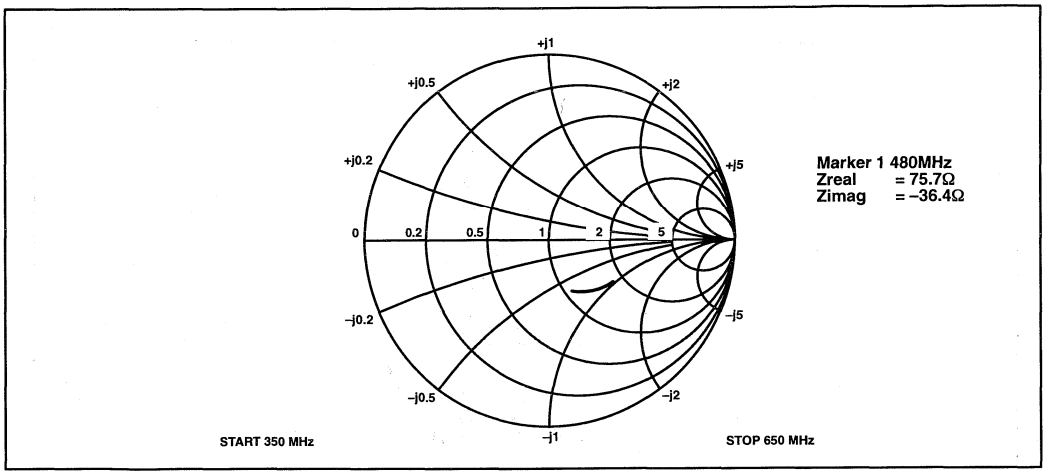


Fig. 4 Input impedance

APPLICATION NOTES

These application notes should be read in conjunction with the circuit diagram Fig 3. and the PCB layout illustrated in Figs 9 & 10. This board has been designed to permit the initial evaluation of the SL1710 performance.

OSCILLATOR

This application uses a synthesised VCO with a tuning range of 350MHz to 500MHz. The inductors L1 and L2 consist of 1.5 turns of 24SWG enamelled copper wire, of 2.5mm diameter. The VCO frequency is controlled by the SP5611 synthesiser which is programmed via an I^2C bus. The RF input to the synthesiser is from the SL1710 prescaler outputs via RF inductors L3 and L4.

PRESCALER OUTPUTS

The VCO frequency/32 is available at the differential prescaler outputs. pins 10 and 11. This enables the on board VCO to be synthesised via a PLL.

VCO DISABLE

The on–chip oscillator can be disabled by connecting the VCO Disable (pin 15) to ground and enabled by connecting the pin to V_{CC} via a 4K7 pull up resistor.

AGC

The DC voltage measured at TP1 should be adjusted using VR1 to read 2.5 volts with respect to V_{EE}. This voltage equates to the nominal centre of the AGC control curve. The control voltage applied to Pin 1 can be varied between 0.5 Volts (maximum gain) and V_{CC}–0.5Volts (minimum gain).

I & Q OUTPUTS

The I and Q output stages of the SL1710 are sensitive to the loads connected to them. To avoid degrading the output signals resistive loads connected to these Pins should always be 1KΩ or greater with a parallel capacitance of 15pF or less.

For evaluation purpose this makes the output unsuitable for connection to test equipment via normal coaxial cables. To alleviate this problem the application board is fitted with emitter follower buffer amplifiers which allow the connection of loads as low as 50Ω via coaxial cables without loading the output stages of the SL1710.

This technique may also be used in a real application where the SL1710 is used to drive an ADC via an anti–alias filter. Great care must be taken to ensure that the loading conditions stated above are not exceeded when designing the anti–alias filter section. Use of an emitter follower buffer is the easiest way to alleviate this constraint.

With the AGC voltage adjusted to 2.5 Volts apply an input signal to the IF IN (Pin 5) and monitor the Base Band output level at the I and Q outputs. Adjust the RF input level until an output level of 760mV pk–pk is achieved. For best performance this level should not be exceeded.

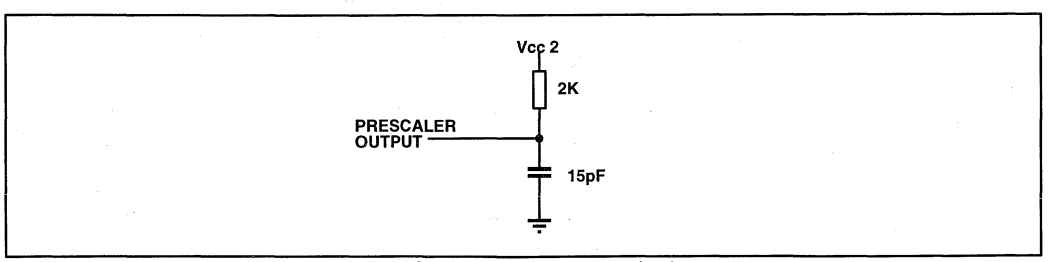


Fig. 5 Maximum prescaler output load.

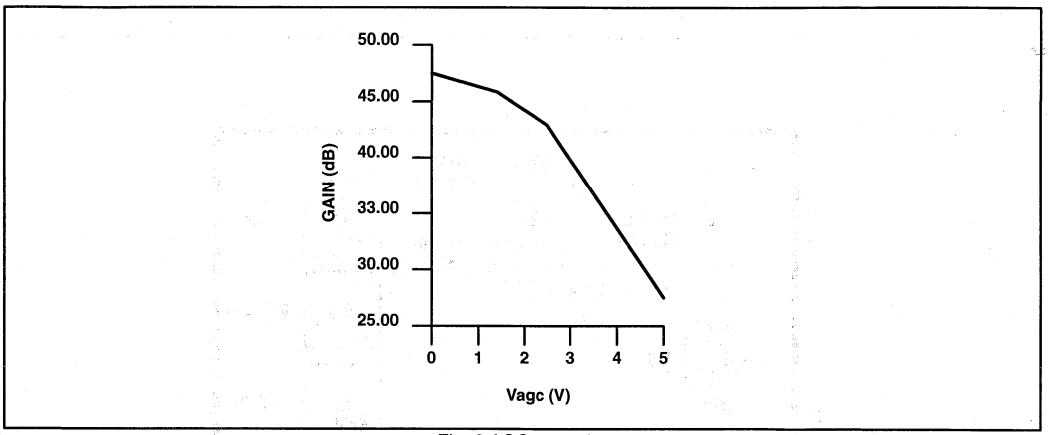


Fig. 6 AGC operation

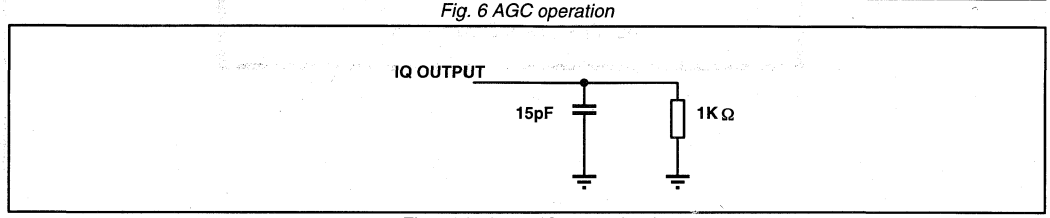


Fig. 7 Maximum IQ output load

Marker	Freq	Zreal	Zimag
1	500KHz	3.5Ω	0.5Ω
2	15MHz	4.5Ω	32Ω
3	30MHz	56Ω	92Ω

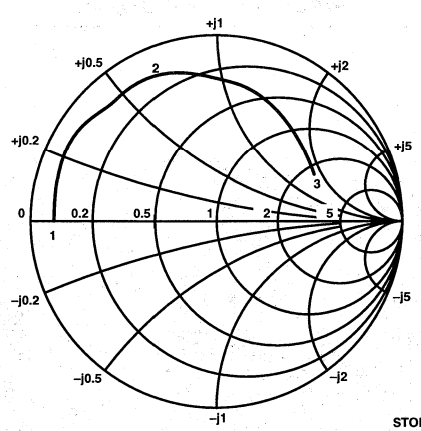


Fig. 8 Output impedance

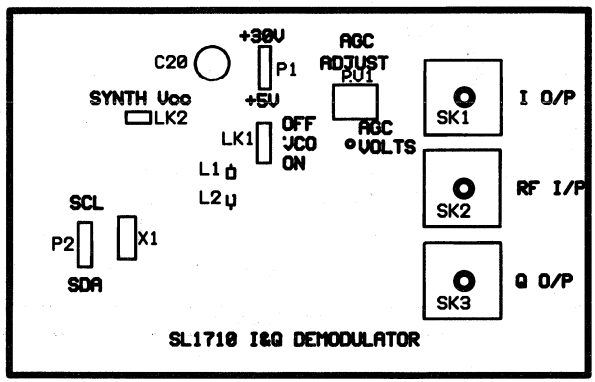


Fig.9 Demonstration PCB top view

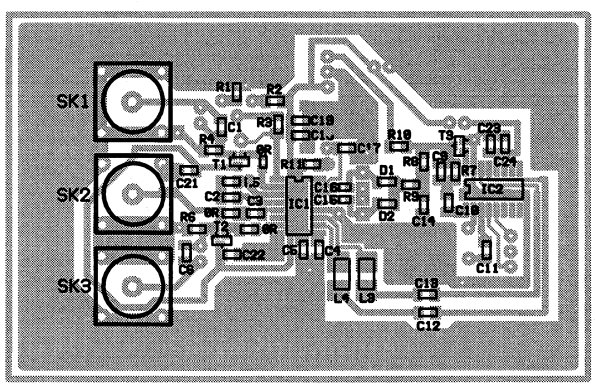


Fig.10 Demonstration PCB bottom view

Section 3
Teletext

GEC PLESSEY
SEMICONDUCTORS

MV1815

SINGLE CHIP TELETEXT DECODER FOR 625 LINE OPERATION

(Supersedes Version in April 1994 Consumer IC Handbook,HB3120–2.0)

The MV1815 is an advanced CMOS single chip Teletext decoder for 625 line World System Teletex. The MV1815 has an on–chip data slicer circuit, dual page acquisition circuits, and direct memory addressing which allow a low cost Teletext decoder to be built with a minimum number of additional components.

FEATURES

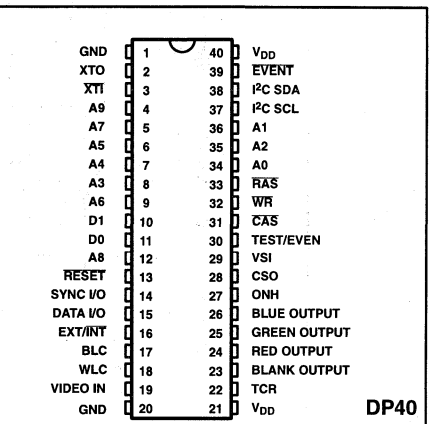
- On–Chip data slicing
- Up to 254 display pages stored, using low cost 150ns DRAMS
- Low external component count
- I^2C Bus for low cost interfacing
- Multi–language capability for fourteen European languages
- Special parity inhibit for TOP 8–bit data
- Non–display packets stored for linked page operation, video programming, etc.
- high resolution characters typically 12 dots wide on a 15 by 10 matrix
- Accepts all non–display packets
- On–chip video switch
- Advanced CMOS technology gives low power disipation and high reliability

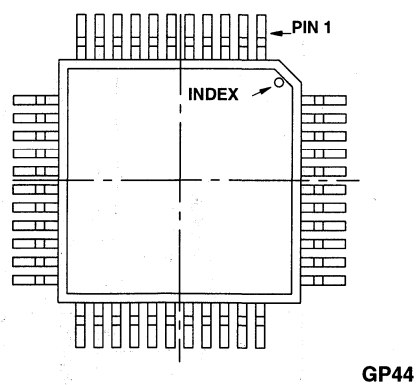
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	–0.3V to +7.0V
All inputs	–0.3V to V_{DD} + 0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	–65°C to + 150°C

ORDERING INFORMATION

MV1815–2A BA DP	West European version
MV1815–2 BA GP	West European version
MV1815–2A BA GPTS	West European version (Tape & reel)





PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	A1	16	D1	31	BLANK
2	SCL	17	D0	32	RED
3	SDA	18	A8	33	GREEN
4	N/C	19	N/C	34	BLUE
5	EVENT	20	RESET	35	ONH
6	V_{DD}	21	SYNC I/O	36	CSO
7	GND	22	DATA I/O	37	VSI
8	XTO	23	EXT/INT	38	N/C
9	XTI	24	BLC	39	TEST/EVEN
10	A9	25	WLC	40	CAS
11	A7	26	VIDEO	41	WR
12	A5	27	GND	42	RAS
13	A4	28	V_{DD}	43	A0
14	A3	29	TCR	44	A2
15	A6	30	N/C		

Fig. 1 Pin connections – top view

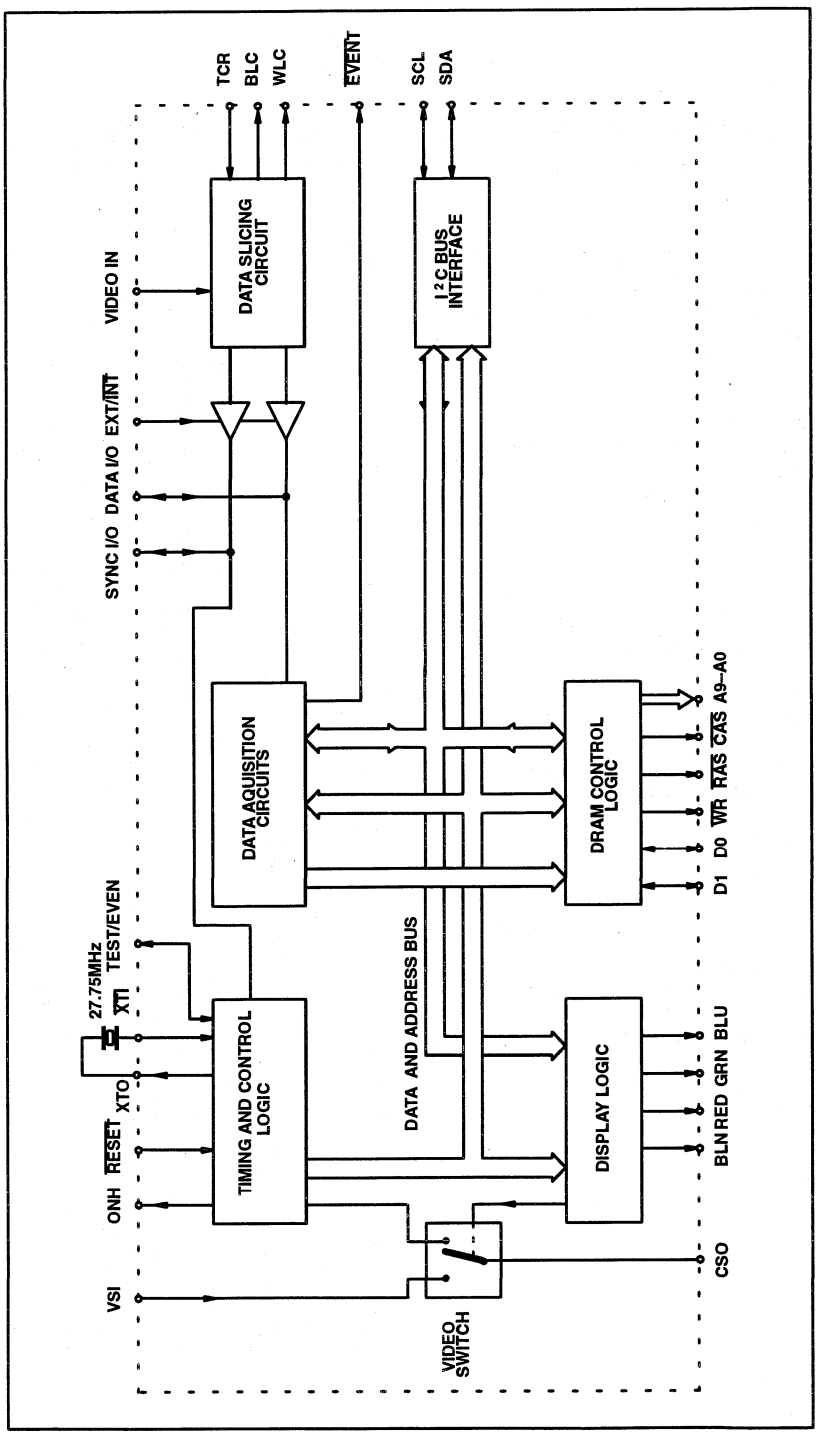


Fig. 2 MV1815 block diagram

<table>
<tr><th>Section</th><th>Specification</th></tr>
<tr><td>Data Acquisition Logic
Line Standard
Teletext data rate
Data line content
TV lines used VBI
TV lines used full field
Packets accepted
Page numbers
Page subcodes</td><td>
625 Lines 50 Fields/second
6.9375 Mbits/sec ±25ppm
360 bits as 45 bytes of 8 bits each
Lines 6 to 22 and 318 to 335
All TV Lines
×/0 to ×/25, ×/26, ×/27, ×/28, ×/29, ×/30 (all formats), ×/31
000 to 7FF
0000 to 3F7F</td></tr>
<tr><td>Display Logic
Characters per row
Teletext rows displayed

TV lines used

Character definition
Character Sets

Spacing control characters

Data boxing into picture

Displayable page stores

Display options</td><td>
40, occupying 43.24µs of the 52µs display time
0 to 23 with 24 and 25 software programmable

<table><tr><th rowspan="2">Rows Displayed</th><th colspan="2">TV Lines</th></tr><tr><th>Start</th><th>Finish</th></tr><tr><td>24</td><td>48</td><td>287</td></tr><tr><td>25 or 26</td><td>38</td><td>297</td></tr></table>
15×10 dot matrix
English, German, Swedish, Italian, French, Spanish,Czechoslovakian, Polish, Romanian, Hungarian, Turkish, Danish, Serbo–Croat, ASCII
Standard Level One Range

Page Number – Row 0 characters 1 to 8
Page Header – Row 0 characters 9 to 32
Clock Time – Row 0 characters 33 to 40
Rows 24 and 25
Up to 254 pages, each of 1k bytes, depending on the size of the DRAM being used

Mix of text foreground and picture background
Three part magnify – display rows 0 to 11 double height
display rows 6 to 17 double height
display rows 12 to 23 double height
Boxing of Newsflash and Subtitles into picture
Boxing of picture into text</td></tr>
<tr><td>Dynamic RAM Control Logic
Memory Configuration

Maximum access time (t_{RAC})
Refresh period for complete memory</td><td>
All sizes: Page or nibble mode types
254 pages – 2 off 1M×1 or 1 off 1M×4
62 pages – 2 off 256k×1 or 1 off 256k×4
14 pages – 2 off 64k× 1 or 1 off 64k×4
150ns
2.048ms
Refresh occurs during the line flyback period. Contents of any memory location may be accessed by the microprocessor via the I²C Bus Interface</td></tr>
<tr><td>I²C Bus Interface</td><td>
Standard implementation of a slave transmitter/receiver Control of the MV1815 is via the I²C Bus Interface</td></tr>
<tr><td>I²C Bus Address</td><td>
0010 001 R/$\overline{W}$</td></tr>
</table>

Table 1. MV1815 System specification

PIN DESCRIPTION		
Symbol	Pin No (DP 40)	Pin name and Description
GND	1, 20	Ground, both pins must be connected
XTO	2	Crystal out 27.75MHz fundamental crystal with an on–chip 1MΩ bias resistor to $\overline{XTI}$
$\overline{XTI}$	3	Crystal input
A9, A7, A5, A4, A3, A6, A8, A0, A2, A1	4 – 9 12, 34, 35, 36	DRAM address outputs
D1, D0	10, 11	DRAM data lines. Internal 100kΩ pull – up resistors are included.
$\overline{RESET}$	13	Active low reset input. Includes 100kΩ pull – up resistor.
SYNC I/O	14	Sliced sync input / output.
DATA I/O	15	Teletext data input / output
EXT/$\overline{INT}$	16	Control pin for SYNC and DATA I/O. Includes 100kΩ pull–down resistor. When low or not connected internal SYNC and DATA are used, pins 14 & 15 are outputs. When high supply SYNC and DATA from an external source, pins 14 & 15 are inputs.
BLC	17	Black level capacitor.
WLC	18	White level capacitor
VIDEO IN	19	Input for composite video signal with negative going SYNCS.
VDD	21, 40	+5V Supply. Both pins must be connected.
TCR	22	Time constant resistor controlling discharge rate of black and white level capacitor voltages.
BLANK	23	Blanking output, high power push–pull driver.
RED	24	Red output, high power push–pull tri–state driver.
GREEN	25	Green output, high power push–pull tri–state driver.
BLUE	26	Blue output, high power push–pull tri–state driver.
ONH	27	On hours indicator. When high CSO is locked to Video In. When low CSO is not locked.
CSO	28	Generated composite sync output during text, video input is switched through to CSO during modes that contain picture content. See Fig. 6.
VSI	29	Video switch input.
TEST/EVEN	30	Used for factory testing. Even output is enabled by bits IOE and EOE in SYNCSW register. If EVEN output is not used, the pin should be left open–circuit. A 100kΩ pull–down resistor is included.
$\overline{CAS}$	31	DRAM column address strobe.
$\overline{WR}$	32	DRAM read/not write signal.
$\overline{RAS}$	33	DRAM row address strobe.
I^2C SCL	37	I^2C bus serial clock.
I^2C SDA	38	I^2C bus bi–directional data port.
$\overline{EVENT}$	39	Active low open drain output interrupt signal to microprocessor.

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency 27.750000MHz. AT cut

Tolerance overall ±100ppm.
Nominal load capacitance 20pF
Equivalent series resistance <20Ω

A variable capacitor is provided internally on pin XTI and controlled by a phase locked loop to provide exact trimming of the frequency. This will provide compensation for temperature variation and crystal ageing.

			BIT POSITION									
ADDRESS		REGISTER	7	6	5	4	3	2	1	0	R/W	RESET STATE
DEC	HEX											HEX
		RADD	A17	A16	IAI	RA4	RA3	RA2	RA1	RA0	W	00
0	0	ACONA	ACQ	MGC	PBC	PAC	SDC	SCC	SBC	SAC	W	F0
1	1	STORA	STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0	W	02
2	2	PGS1A	SCS3	SCS2	SCS1	SCS0	SAS3	SAS2	SAS1	SAS0	W	00
3	3	PGS2A	MS2	MS1	MS0	SDS1	SDS0	SBS2	SBS1	SBS0	W	20
4	4	PGS3A	PBS3	PBS2	PBS1	PBS0	PAS3	PAS2	PAS1	PAS0	W	00
5	5	ACONB	$\overline{\text{HLD}}$	MGC	PBC	PAC	SDC	SCC	SBC	SAC	W	F0
6	6	STORB	STB7	STB6	STB5	STB4	STB3	STB2	STB1	STB0	W	03
7	7	PGS1B	SCS3	SCS2	SCS1	SCS0	SAS3	SAS2	SAS1	SAS0	W	00
8	8	PGS2B	MS2	MS1	MS0	SDS1	SDS0	SBS2	SBS1	SBA0	W	00
9	9	PGS3B	PBS3	PBS2	PBS1	PBS0	PAS3	PAS2	PAS1	PAS0	W	88
10	A	RECON	WI0	WI24	WI25	PIN B	PIN A	FF	CDB	CDA	W	00
11	B	DISCON1	INV	RLH	DSB	CLS	CUR	BLC	LS3	UDI	W	00
12	C	DISCON2	LSO	LS1	LS2	MGS	IHD	SPH	BX1	BX0	W	00
13	D	DISCON3	TXT	MIX	INT	REV	UDK	SPOS	ST2	ST1	W	00
14	E	DISCON4	BXP	BXH	BXT	BXS	DHT	DHB	SG2	SG1	W	00
15	F	HADD	A15	A14	A13	A12	A11	A10	A9	A8	W	00
16	10	LADD	A7	A6	A5	A4	A3	A2	A1	A0	W	00
17	11	WDATA	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	W	00
19	13	SCROLL	WI29	MV	CRL	SRA4	SRA3	SRA2	SRA1	SRA0	W	00
20	14	SYNCSW	ESS	–	–	–	IOE	EOE	SEN	SVS	W	00
0	0	EVENTA	NPR	VHR	830A	X/29	X/28	X/27	X/26	C8	R	–
1	1	EVENTB	NPR	VHR	830B	X/29	X/28	X/27	X/26	C8	R	–
2	2	CBITSA	C14	C13	C12	C11	C10	C7	C6	C5	R	–
3	3	PGR1A	SCR3	SCR2	SCR1	SCR0	SAR3	SAR2	SAR1	SAR0	R	–
4	4	PGR2A	MR2	MR1	MR0	SDR1	SDR0	SBR2	SBR1	SBR0	R	–
5	5	PGR3A	PBR3	PBR2	PBR1	PBR0	PAR3	PAR2	PAR1	PAR0	R	–
6	6	CBITB	C14	C13	C12	C11	C10	C7	C6	C5	R	–
7	7	PGR1B	SCR3	SCR2	SCR1	SCR0	SAR3	SAR2	SAR1	SAR0	R	–
8	8	PGR2B	MR2	MR1	MR0	SDR1	SDR0	SBR2	SBR1	SBR0	R	–
9	9	PGR3B	PBR3	PBR2	PBR1	PBR0	PAR3	PAR2	PAR1	PAR0	R	–
10	A	HAMMC	HC7	HC6	HC5	HC4	HC3	HC2	HC1	HC0	R	FF
17	11	RDATA	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	R	–

Table 2 MV1815 Register details

Note. Write register addresses 18, and 21–31 (12, and15–1F HEX) are reserved for future development and should not be used.

WRITE REGISTERS

RADD (W)

A16 / A17	Memory quadrant select
IAI	Inhibit auto increment
RA$	Register address ($=0 to 4)

ACON A/B (W 0 & 5)

ACQ	Acquisition on
MGC	Magazine compare
PAC	Page units compare
PBC	Page tens compare
SAC	Page subcode compare digit A
SBC	Page subcode compare digit B
SCC	Page subcode compare digit C
SDC	Page subcode compare digit D
HLD	Not hold display acquisition circuit

STOR A/B (W 1 & 6)

STA$	Store number for acquisition A ($=0 to 7)
STB$	Store number for acquisition B ($=0 to 7)

PGS /1/2/3 A/B (W 2,3 4 & 7,8,9)

SAS$	Subcode digit A ($=0 to 3) select
SBS$	Subcode digit B ($=0 to 2) select
SCS$	Subcode digit C ($=0 to 3) select
SDS$	Subcode digit D ($=0 or 1) select
PAS$	Page number (units) ($=0 to 3) select
PBS$	Page number (tens) ($=0 to 3) select
MS$	Magazine number ($=0 to 2) select

RECON (W 10)

WI0	Write inhibit of packet 0
WI24	Write inhibit of packet 24
WI25	Write inhibit of packet 25
PIN B	Parity check inhibit acquisition circuit B
PIN A	Parity check inhibit acquisition circuit A
FF	Full field Teletext
CDB	Clear store disable acquisition circuit B
CDA	Clear store disable acquisition circuit A

DISCON1 (W 11)

INV	Invert display
RLH	Roll headers
DSB	Display acquisition circuit B (A if zero)
CLS	Clear current display store
CUR	Cursor enable
BLC	Block cursor
LS3	Language group select
UDI	Display update indicator

DISCON2 (W 12)

LS$	Language select ($=0 to 2)
MGS	Magazine serial
IHD	Inhibit display, rows 2 to 26 disabled
SPH	Suppress header
BX$	Box control bits ($=0 or 1)

DISCON3 (W 13)

TXT	Text / not picture
MIX	Mix text and picture
INT	Display text in interlace mode (see Figure 6)
REV	Reveal hidden text
UDK	Update key, rows 1 to 26 disabled.
SPOS	Status line position
ST2	Display Status line 2 (row 26)
ST1	Display Status line 1 (row 25)

WRITE REGISTERS

DISCON4 (W 14)

BXP	Box page number
BXH	Box header
BXT	Box time
BXS	Box status rows
DHT	Double height top half
DHB	Double height bottom half
SG$	Separate graphics control bits ($=0 or 1)

HADD and **LADD** (W 15 & 14)

A$	Memory address ($=0 to 15)

WDATA (W 17)

WD$	Data to be written to memory ($=0 to 7)

SCROLL (W 19)

WI29	Write inhibit of packet 29
MV	Majority vote on framing code
CRL	Cursor lock at last HADD. LADD setting
SRA$	Scroll display row up ($=0 to 4)

SYNCSW (W 20)

ESS	External sync source
IOE	Internal output enable
EOE	Even output enable
SEN	Select enable – SVS bit
SVS	Select VSI as sync source

READ REGISTER

EVENT A/B (R 0 & 1)

NPR	New page received
VHR	Valid header received
830$	Packet 30 received acquisition $ ($=A or B)
X/29	Packet 29 received
X/28	Packet 28 received
X/27	Packet 27 received
X/26	Packet 26 received
C8	Update Indicator

CBITS A/B (R 2 & 6)

C14	Language select bit
C13	Language select bit
C12	Language select bit
C11	Magazine serial
C10	Inhibit display
C7	Supress header
C6	Sub–title
C5	Newsflash

PGR/1/2/3/A/B (R 3,4,5 & 7,8,9)

SAR$	Subcode digit A ($=0 to 3) received
SBR$	Subcode digit B ($=0 to 2) received
SCR$	Subcode digit C ($=0 to 3) received
SDR$	Subcode digit D ($=0 or 1) received
PAR$	Page number (units) ($=0 to 3) received
PBR$	Page number (tens) ($=0 to 3) received
MR$	Magazine number ($=0 to 2) received

HAMMC (R 10)

HC$	Hamming error counter ($=0 to 7)

RDATA (R 17)

RD$	Data read from memory ($=0 to 7)

I²C BUS

Device Address **0010 001 R/W**

The circuit works as a slave transmitter with bit eight set high or as a slave receiver with bit eight low. In receive mode, the first data byte is written to the RADD register, where the least significant five bits form the sub–address for the next register to be written. The most significant three bits of RADD are data bits, see Table 2.

Automatic incrementing of registers allows successive data bytes to be written to or read from the registers. The automatic incrementing can be disabled by setting bit 5 of the sub–address register (RADD) to one.

If the sub–address is set to write or read from DRAM, the auto incrementing allows access to successive bytes of data. All DRAM addresses may be accessed via the I²C bus register. A stop condition resets the sub–address to zero.

Example of I²C Bus Messages

Write operation – MV1815 as a slave receiver

S	MV1815 ADD	W	A*	RADD (n)	A*	DATA (reg n)	A*	DATA (reg n + 1)	A*	P

Read operation – MV1815 as a slave transmitter

S	MV1815 ADD	R	A*	DATA * (reg 0)	A	DATA * (reg 1)	A	DATA * (reg 2)	NA	P

S Start Conditions
P Stop Condition
A Acknowledge
NA No Acknowledge
W Write (=0)
R Read (=1)
* MV1815 output

Write/read operation – MV1815 as a slave transmitter sending data from register n etc.

S	MV1815 ADD	W	A*	RADD (reg n)	A*	S	MV1815 ADD	R	A*	DATA* (reg n)	A	DATA * (reg n + 1)	NA	P

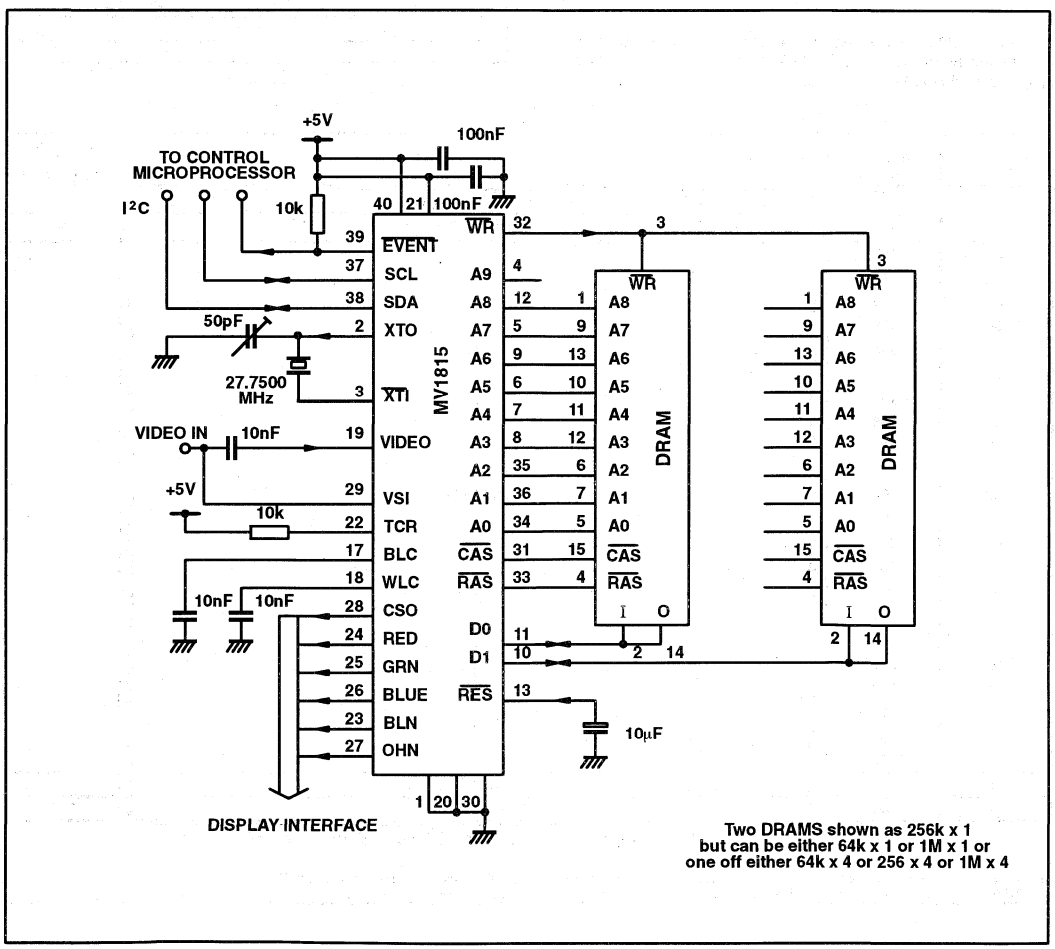


Fig. 3. MV1815 Typical application

DRAM Memory Organisation

The DRAM as viewed from the I²C Bus is organised in 1024 byte blocks. Each 1024 bytes (400 HEX) block is referred to as a store. Stores 0 and 1 are reserved for the non–display packets from acquisition A and B respectively. Stores 2 and above are used for display pages, one page per store.

The display page number, first 8 bytes on row 0, are held in Store 0 bytes 0 to 7. The Time display, last 8 bytes on row 0 are also held in store 0 bytes 8 to F (HEX). See Figs. 4 and Figs. 5

To calculate the values of the start address in RADD, HADD and LADD for any store simply multiply the store number (HEX) by 400 (HEX)

e.g. Decimal store 160 = A0

A0 x 400 = 2 80 00 (HEX)
RADD HADD LADD

To find the address of any particular location in the store add the value of the relative address from Fig. 4 or 5.

Table 3 gives examples of the start addresses of stores expressed as values of A17, A16 from RADD, A15–A8 from HADD and A7–A0 from LADD.

STORE NUMBER HEX	START ADDRESS IN HEX		
	RADD	HADD	LADD
00	0	00	00
01	0	04	00
02	0	08	00
03	0	0C	00
04	0	10	00
05	0	14	00
06	0	18	00
07	0	1C	00
08	0	20	00
:		:	
0F	0	3C	00
10	0	40	00
:		:	
40	1	00	00
41	1	04	00
:		:	
7F	1	FC	00
80	2	00	00
:		:	
F0	3	C0	00
:		:	
FF	3	FC	00

Table 3

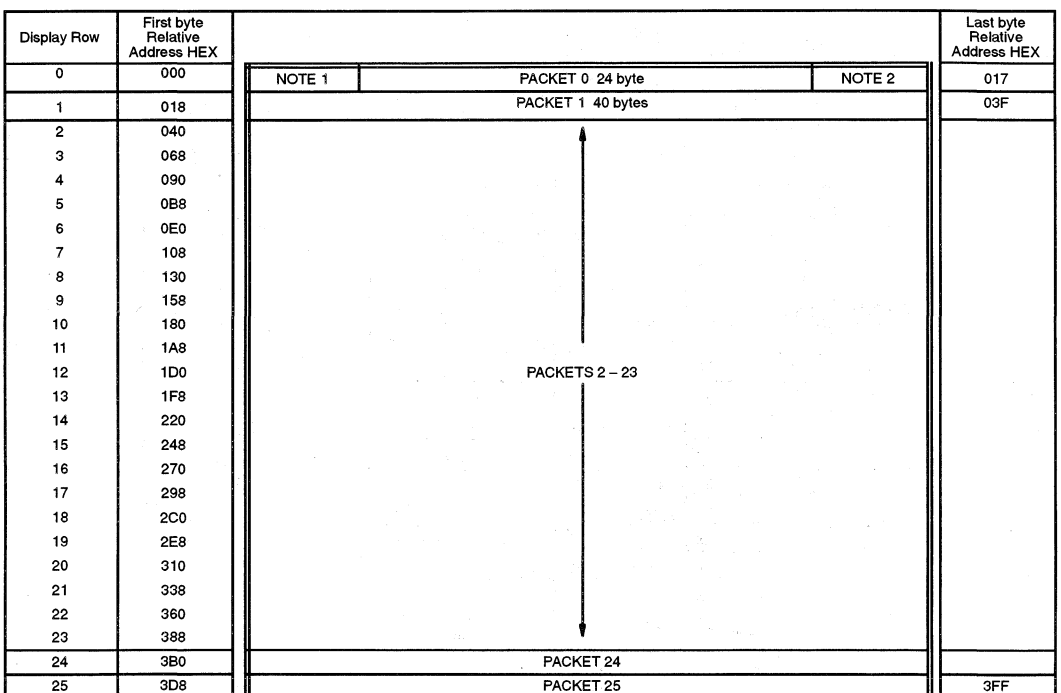


Fig. 4 Organisation of Display Memory. Stores 2 to 256

NOTE 1. Display of page number here, 8 bytes which are located in store 0 with absolute addresses 000 to 007.
NOTE 2. Display of time here, 8 bytes which are located in store 0 with absolute addresses 008 to 00F

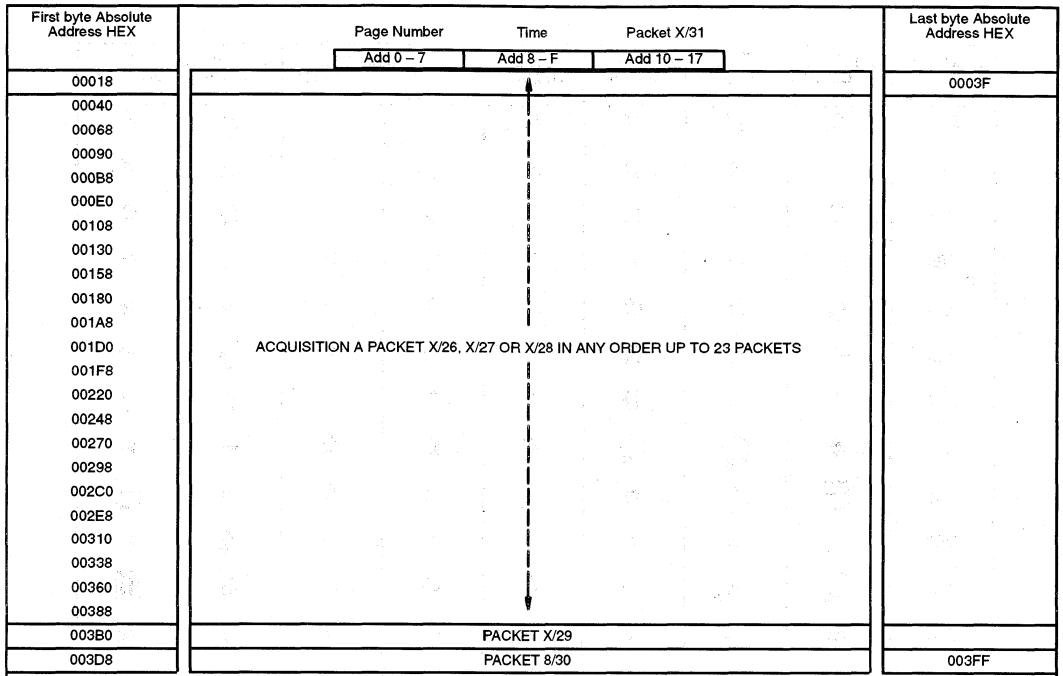


Fig. 5. Store 0 memory organisation

Packet 8/30 designation codes 0,1,4,5,8,9, C and D are written to store 0.

NOTE: Store 1 is organised similarly except that it accepts acquisition circuit B packets X/26, etc. The starting address is 00400 (HEX) and bytes 00400 to 00417 (HEX) are not used by the MV1815. All addresses shown in Fig. 5 add 00400 (HEX).
Packet 8/30 designation codes 2,3,6,7, A,B,E and F are written to store 1.

	0	1
0	Alpha Black	Graphic Black
1	Alpha Red	Graphic Red
2	Alpha Green	Graphic Green
3	Alpha Yellow	Graphic Yellow
4	Alpha Blue	Graphic Blue
5	Alpha Magenta	Graphic Magenta
6	Alpha Cyan	Graphic Cyan
7	Alpha White[1]	Graphic White
8	Flash	Conceal Display [2]
9	Steady [1]	Contiguous Graphics [1 2]
A	End Box [1]	Separated Graphics [2]
B	Start Box [3]	No action
C	Normal Height [1 2]	Black Background [1 2]
D	Double Height	New Background [2]
E	No action	Hold Graphics
F	No action	Release Graphics [1]

Table 4 Control codes

Notes: 1. Presumed set at the start of each display row.

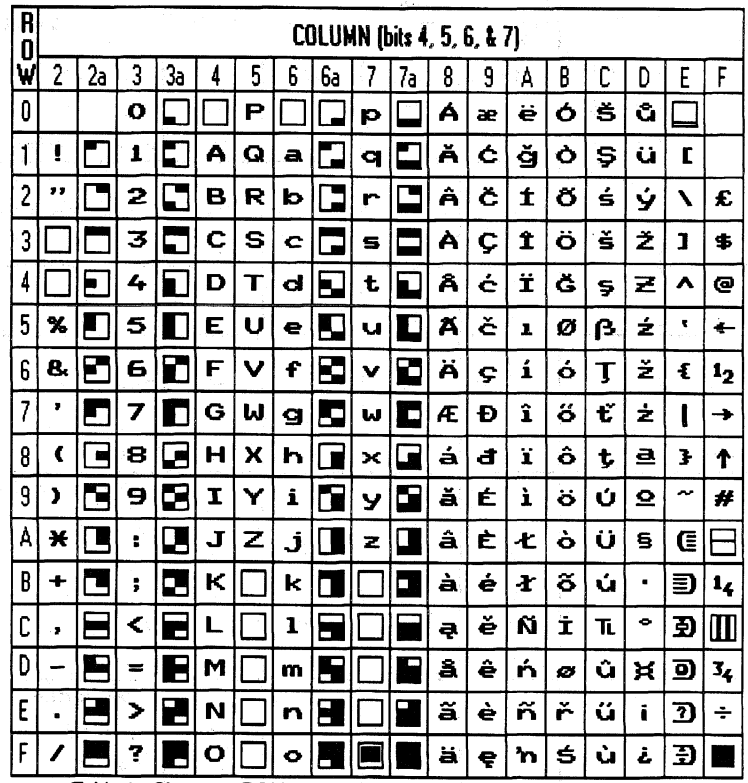
2 Action "set at the current space", others are "set after the current space".

3. Two consecutive codes are transmitted, action takes place between them.

LS(3210) TABLE POSITION	0000 ENGLISH	0001 GERMAN	0010 SWEDISH FINNISH	0011 ITALIAN	0100 FRENCH (BELGIAN)	0101 SPANISH	0110 CZECH	0111 ENGLISH
2/3	£	#	#	£	é	ç	#	£
2/4	$	$	¤	$	ï	$	ů	$
4/0	@	§	É	é	à	ì	č	@
5/B	←	Ä	Ä	°	ë	á	ť	←
5/C	½	Ö	Ö	ç	ê	é	ž	½
5/D	→	Ü	Å	→	ù	í	ý	→
5/E	↑	^	Ü	↑	î	ó	ì	↑
5/F	#	_	_	#	#	ú	ř	#
6/0	■	°	é	ù	è	¿	é	■
7/B	¼	ä	ä	à	â	ü	á	¼
7/C	▮	ö	ö	ò	ô	ñ	ě	▮
7/D	¾	ü	å	è	û	è	ú	¾
7/E	÷	ß	ü	ì	ç	à	š	÷

LS(3210) TABLE POSITION	1000 POLISH	1001 ROMANIAN	1010 HUNGARIAN	1011 TURKISH	1100 DANISH	1101 SERBO CROAT	1110 ASCII	1111 SOUTH AFRICAN
2/3	#	#	#	₺	£	#	#	£
2/4	ń	¤	ú	ğ	$	$	$	$
4/0	ą	Ţ	É	İ	@	Č	@	ħ
5/B	Ż	Â	í	Ş	Æ	Ć	[	ë
5/C	ś	Ş	ö	ö	Ø	Ž	\	ê
5/D	ł	Ă	Á	Ç	Å	Đ	]	ü
5/E	ć	î	ű	ü	↑	Š	^	é
5/F	ó	ı	ő	ğ	#	ë	_	ï
6/0	ę	ţ	é	ı	■	č	`	š
7/B	ż	â	ó	ş	æ	ć	{	ä
7/C	ś	ş	ö	ö	ø	ž	▯	ô
7/D	ł	ă	á	ç	å	đ	}	û
7/E	ź	î	ü	ü	÷	š	~	ö

Table 5. Western European national optional variations - MV1815-2.



ROW	COLUMN (bits 4, 5, 6, & 7)																	
	2	2a	3	3a	4	5	6	6a	7	7a	8	9	A	B	C	D	E	F
0			0			P			p		Á	æ	ë	ó	š	û		
1	!		1		A	Q	a		q		Ă	ć	ğ	ò	Ş	ü	[	
2	"		2		B	R	b		r		Â	č	ţ	ő	ś	ý	\	£
3			3		C	S	c		s		Ä	Ç	Ţ	ö	š	ž	]	$
4			4		D	T	d		t		Ĺ	ć	Ť	ğ	ş	ź	^	@
5	%		5		E	U	e		u		Ć	č	ı	ø	ß	ż	'	←
6	&		6		F	V	f		v		Ä	ç	í	ó	Ţ	ž	€	½
7	'		7		G	W	g		w		Æ	Đ	î	ő	ť	ż	|	→
8	(		8		H	X	h		x		á	đ	ï	ô	ţ	ą	ł	↑
9	)		9		I	Y	i		y		ă	É	ì	ö	ú	ọ	~	#
A	*		:		J	Z	j		z		â	Ę	Ł	ò	Ü	ş	(	⊟
B	+		;		K		k				à	é	ł	ő	ú	·	)	¼
C	,		<		L		l				ą	ě	Ń	ı	Ţ	°	Ð	▥
D	–		=		M		m				ă	ę	ń	ø	ů	¤	Đ	¾
E	.		>		N		n				ã	è	ň	ř	ú	ı	Ð	÷
F	/		?		O		o				ä	ę	ň	ś	ù	¿	Ð	■

Table 6. Character ROM contents as viewed by the display - MV1815-2.

Notes: Character positions F0 and F1 will be displayed as spaces, but are actually spacing control codes, like the control columns 0 and 1 listed in table 10.
F0 is UNDERLINE start / stop code.
F1 is INVERT display colours start / stop code.
FF is displayed as all foreground.
☐ Characters in these positions are displayed according to the setting of LS(0-3) bits, see table 5. When graphics mode is set, columns 2a, 3a, 6a & 7a are displayed as the graphic symbols shown. All other columns are displayed normally. The graphic symbols are shown above with a border which is not present when the symbol is displayed on the screen.

ELECTRICAL CHARACTERISTICS

T_{amb}= 0°C to +70°C, V_{CC}= +5V to ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply Voltage	21 & 40	4.5	5.0	5.5	V	XTI=27.75MHz All outputs open
Supply Current	21 & 40		25		mA	circuit
	21 & 40		15		mA	XTI=0Hz All outputs open circuit
Video Input, VSI	19 & 29					
Voltage Amplitude		0.8		3.0	Vpp	Bottom of Sync to White (pk–pk)
Source Impedance				250	Ω	
TCR Input	22					
External Resistance		5	10	200	kΩ	Connected to V_{DD}
BLC and WLC	17 & 18					
Capacitor Value			10		nF	Connected to GND
Capacitor Tolerance		–10		+10		
Effective Series Resistance				5	Ω	1MHz
Sync I/O	14					100K (nom) pull up resistor
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}–1.0		V_{DD}	V	
Input Current Low		–22	–50	–220	µA	V_{IN}=V_{SS}
Input Current High		–30		+30	µA	V_{IN}=V_{DD}
Data I/O	15					No pull–up resistor
Output voltage High		2.4	4.5		V	I_{OH}=–1.2mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
Input voltage Low		0		1.0	V	
Input Voltage High		V_{DD}–1.0		V_{DD}	V	
Input current	–30		+30		µA	V_{IN}=V_{DD} or V_{SS}
$\overline{EXT}$/INT (Note 1)	16					100kΩ (nom) pull–down resistor
Input current Low		–10		+10	µA	V_{IN}=V_{SS}
Input current High		22	50	220	µA	V_{IN}=V_{DD}
XTI (Note 1)	3					1M (nom) resistor to XTO
Input current Low		–5.0	–5.0	–20	µA	–0.3 <V_{IN} <V_{IL} max
Input current High		0.5	5.0	20	µA	V_{IH} min <V_{IN} <(V_{DD}+0.3)
XTO output	2					See note 2
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–1.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Frequency			27.750		MHz	±100ppm

Notes.

1. Input voltage low and input voltage high for these are as specified for Data I/O
2. When $\overline{RESET}$ is held low, A9 (pin 4) will output F_{OSC}/2. If required, adjust capacitor on XTO for a frequency of 13.875MHz.

ELECTRICAL CHARACTERISTICS (continued)

T_{amb}= 0°C to +70°C, V_{CC}=+5V to ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
ON HOUR INDICATOR ONH	27					
Output voltage V_{OH}		V_{DD}–1.0	4.5		V	I_{OH}=–1.2mA
Output voltage V_{OL}			0.2	0.4	V	I_{OL}=2.4mA
I²C bus SCL, SDA I/Ps	37, 38					100kΩ (nom) pull–up resistor
Input voltage Low		0		1.5	V	
Input voltage High		3.5		V_{DD}	V	
Output voltage Low		0	0.1	0.40	V	I_{OL}=3mA
SCL clock frequency	37		100	1000	kHz	
RED, GREEN, BLUE	24, 25, 26					
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–12.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=24.0mA
Tri–state output leakage current		–60		60	µA	V_{OH}=V_{SS} or V_{DD}
EVENT	39					100kΩ (nom) pull–up resistor
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
BLANK	23					
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–12.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=24.0mA
CSO	28					With typical load of 360Ω
Output voltage swing			0.5		Vpp	Text mode only, see note 3
Output voltage High		V_{DD}–0.5			V	Load of 4.3kΩ to V_{DD}
Output voltage Low				V_{DD}+0.5	V	
TEST/EVEN	30					100kΩ (nom) pull–down resistor
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–1.2mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}–1.0		V_{DD}	V	
Input current Low		–30		+30	µA	V_{IN}=V_{SS}
Input current High		22	50	220	µA	V_{IN}=V_{DD}

Note 3.

CSO output voltage when in picture or mix mode will depend on size of Video signal applied to VSI pin 29, together with attenuation due to internal transmission switch (60Ω nom) and external load on pin 28. In these states the video signal at pin 29 is switched straight through to pin 28.

ELECTRICAL CHARACTERISTICS

T_{amb}= 0°C to +70°C, V_{CC}= +5V to ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
MEMORY INTERFACE						100kΩ (nom) pull–up resistor
DATA D0,D1	11,10					
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–1.2mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}–1.0		V_{DD}	V	
Input current Low		–22	–50	–220	µA	V_{IN}=V_{SS}
Input current High		–30		+30	µA	V_{IN}=V_{DD}
ADDRESS A0–A9 RAS, CAS, WR	See Fig. 1					
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–1.2mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
RESET (Schmitt input)	13					100kΩ (nom) pull–up resistor
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}–1.0		V_{DD}	V	
Input current Low		–22	–50	–220	µA	V_{IN}=V_{SS}
Input current High		–10		+10	µA	V_{IN}=V_{DD}
Hysteresis voltage			0.8		V	(Rising threshold) – (falling threshold) voltages

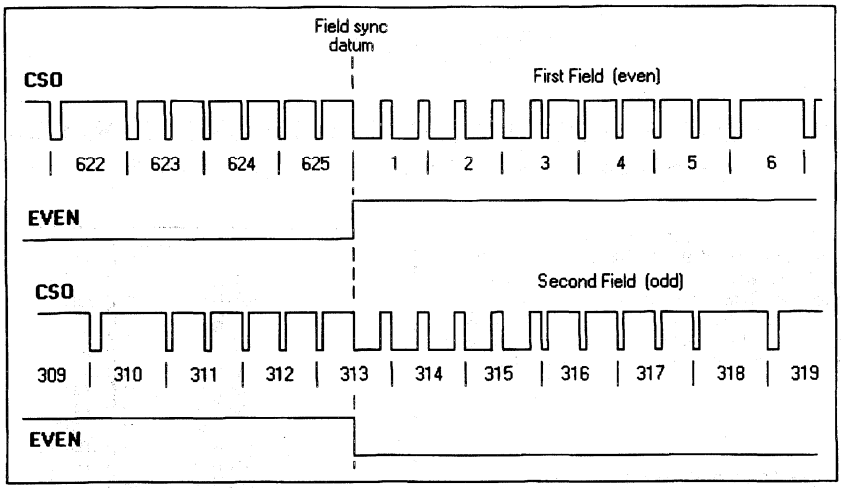


Fig. 6a. Composite sync output (interlaced) and EVEN output.

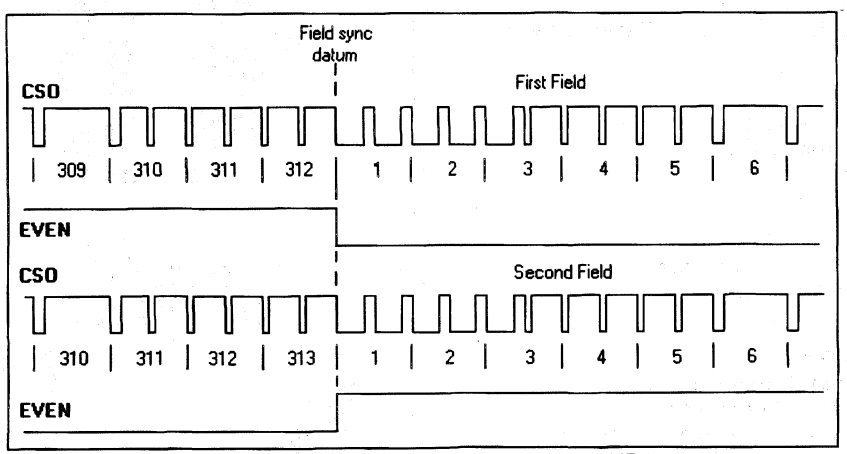


Fig. 6b. Composite sync output (non-interlaced) and EVEN output.

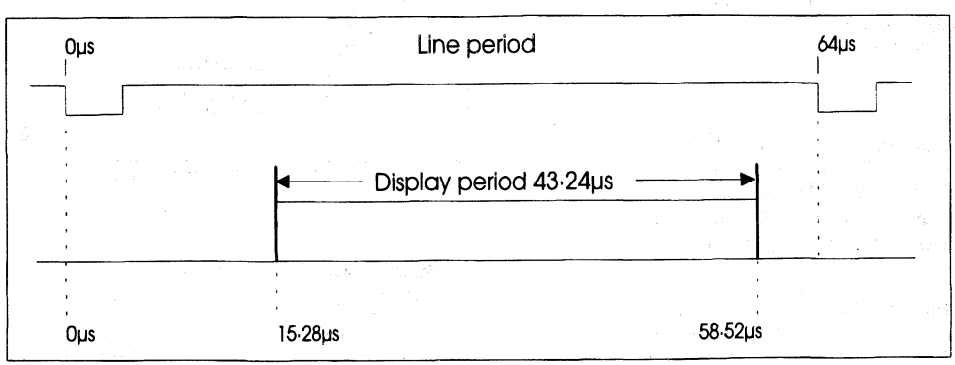


Fig. 7. Timing of display for RGB outputs related to composite sync output.

MV1817

SINGLE CHIP TELETEXT DECODER FOR 625 LINE OPERATION

(Supersedes version in April 1994 Consumer IC Handbook, HB3120–2.0)

The MV1817 Television Data Service, TDS, IC incorporates all the features of the MV1815 with identical registers, so that MV1815 register control is software compatible. Additional TDS features are controlled by registers with addresses above those of the MV1815. A 2K/page system is included to enable extension packets to be stored with the display page data and page header data.

FEATURES

Acquisition

- Two page related data acquisition circuits
- On chip adaptive slicers for data and sync
- Accepts all data packets
- Advanced Header and Instant Page Clear working

Display

- High resolution 15x10 pixel characters
- Multi–lingual capability
- 26 display rows

Memory

- Up to 510 pages in one 4 bit organised DRAM
- 2K or 1K bytes per page

Synchronisation

- Three vertical time base modes:–
  - 312½–312½ interlaced
  - 312 – 312 non–interlaced – default
  - 312 – 313 non–interlaced
- Line (H) and field (V) sync inputs
- Full field operation
- On chip video switch

I²C bus etc.

- I²C bus interface bus to microcontroller
- I²C bus is released during power down
- Software compatible with MV1815
- Software maskable EVENT interrupts
- Register to indicate language variant

ORDERING INFORMATION

MV1817–3 CG DPAS – All Europe version
MV1817–3 CG GPBR – All Europe version

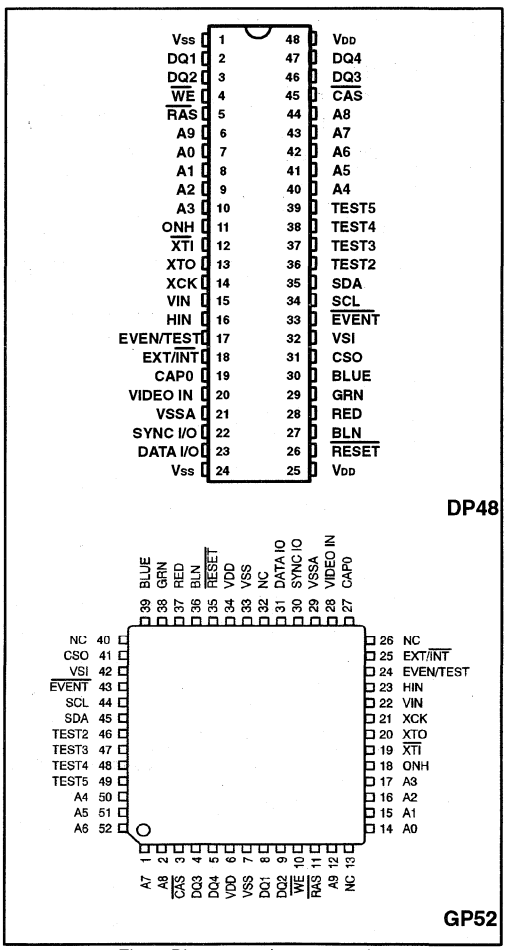


Fig. 1 Pin connections – top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	–0.3V to +7.0V
All inputs	–0.3V to V_{DD}+0.3V
Operating temperature	0°C to +70°C
Storage temperature	–65°C to 150°C

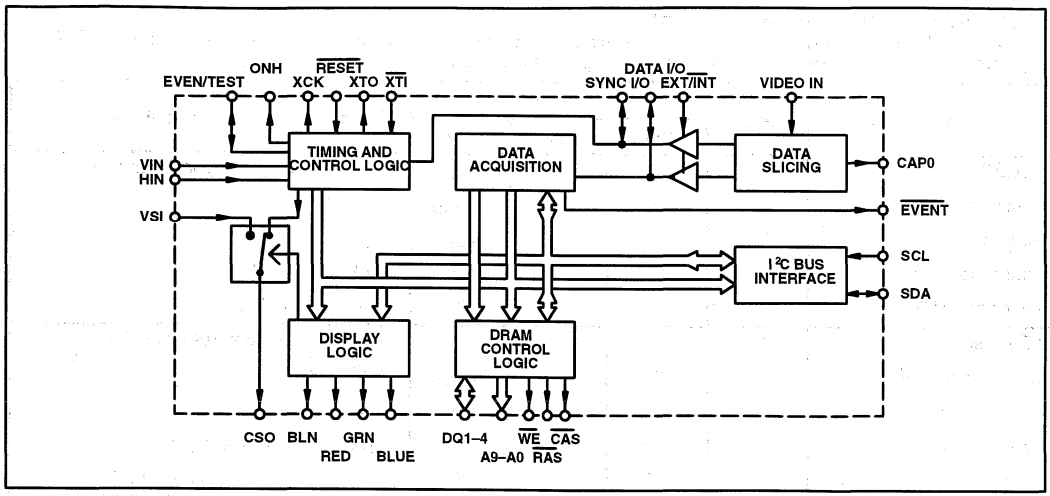


Fig. 2 Functional block diagram

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency (preferred)	6.93750MHz. AT cut
Tolerance over operating temperature range	±50ppm
Tolerance overall	±100ppm
Nominal load capacitance	30pF
Equivalent series resistance	<20Ω

ELECTRICAL CHARACTERISTICS

T_{amb}= 0°C to +70°C, V_{DD}= +5V ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	25, 48	4.5	5.0	5.5	V	
Supply current	25, 48		80	140	mA	V_{DD}=5.5V White test screen
Video input, VSI	20, 32					Acquisition from TV lines 6–22 and 318–335
Voltage amplitude		0.7	1.0	2.0	V_{pp}	Bottom of sync to white (pk to pk)
Source impedance				250	Ω	220nF input capacitor
CAP0	19					
Capacitor value			220		nF	Connected to GND
Capacitor tolerance		−10%		+10%		
Effective series resistance				5	Ω	1MHz
Sync I/O & Data I/O	22, 23					Acquisition from TV lines 2–22 and 314–335, see note 1.
Output voltage High (Data I/O only)		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=−2.0mA Sync I/O is an open drain output.
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Input voltage Low		0		$0.2V_{DD}$	V	
Input voltage High		$0.8V_{DD}$		V_{DD}	V	
Input current Low		−10		+10	µA	V_{IN}=V_{SS} or V_{DD}

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb}= 0°C to +70°C, V_{DD}=+5V ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
EXT/INT	18					75k (nom) pull–down resistor
Input voltage Low		0		$0.2V_{DD}$	V	
Input voltage High		$0.8V_{DD}$		V_{DD}	V	
Input current Low		–10		+10	µA	$V_{IN}=V_{SS}$
Input current High		18	67	275	µA	$V_{IN}=V_{DD}$
XTI input	12					1M (nom) resistor to XTO
Input voltage Low		0		$0.2V_{DD}$	V	
Input voltage High		$0.8V_{DD}$		V_{DD}	V	
Input current Low		–0.5	–5.0	–20	µA	$-0.3 < V_{IN} < V_{IL}$ max
Input current High		0.5	1.5	20	µA	V_{IH} min$<V_{IN}<(V_{DD}+0.3)$
XTO output	13					
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–0.1mA
Output voltage Low			0.2	0.4	V	I_{OL}=0.1mA
Frequency			6.9375		MHz	±100ppm
I²C bus SCL, SDA Schmitt inputs	34, 35					
Input voltage Low		0		1.5	V	
Input voltage High		3.0		V_{DD}	V	
Output voltage Low			0.1	0.6	V	I_{OL}=6.0mA
SCL Clock Frequency			750	775	kHz	
Hysteresis voltage			0.4		V	
EVENT	33					75k (nom) pull–up resistor
Output voltage Low			0.2	0.4	V	I_{OL}=6.0mA open drain
RESET, Schmitt input	26					75k (nom) pull–up resistor
Threshold voltage falling		1.4	1.9			
Threshold voltage rising			3.1	3.8	V	
Hysteresis voltage			1.2		V	
Input current Low		–18	–67	–275	µA	$V_{IN}=V_{SS}$
Input current High		–10		+10	µA	$V_{IN}=V_{DD}$
VIN, HIN, Schmitt input	15, 16					
Threshold voltage falling		1.4	1.9			
Threshold voltage rising			3.1	3.8	V	
Hysteresis voltage			1.2		V	
Input current Low		–10		+10	µA	$V_{IN}=V_{SS}$
Input current High		–10		+10	µA	$V_{IN}=V_{DD}$
VIN pulse width		32			µs	
HIN pulse width		1			µs	at 90% level
VIN rise time				18	µs	10% to 90% level
HIN rise time				6	µs	10% to 90% level

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb}= 0°C to +70°C, V_{DD}=+5V ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
ONH, XCK	11, 14					See note 2
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–2.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Red, Green, Blue	28, 29					
Output voltage High	30	$0.9V_{DD}$	$0.95V_{DD}$		V	I_{OH}=–8mA
Output voltage Low			0.2	0.4	V	I_{OL}=8mA
Tri–state leakage current		–10		10	µA	
Blank	27					
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–12mA
Output voltage Low			0.2	0.4	V	I_{OL}=12mA
CSO	31					With typical ac load of 360Ω
Output voltage swing		0.1		1.5	V_{PP}	Text mode only. See note 3
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–0.2mA with CSOT bit =1
Output voltage Low			0.2	0.4	V	I_{OL}=1.6mA with CSOT bit =1
Even output/Test input (Schmitt)	17					75k (nom) pull–down resistor
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–2.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Threshold voltage falling		1.4	1.9			
Threshold voltage rising			3.1	3.8	V	
Hysteresis voltage		0.6	1.2		V	
Input current Low		–10		–10	µA	V_{IN}=V_{SS}
Input current High		18	67	275	µA	V_{IN}=V_{DD}
Data DQ1 – DQ4	2, 3					75k (nom) pull–up resistor
Output voltage High	46, 47	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–2.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Input voltage Low		0		0.8	V	
Input voltage High		2.0		V_{DD}	V	
Input current Low		–18	–67	–275	µA	V_{IN}=V_{SS}
Input current High		–10		+10	µA	V_{IN}=V_{DD}
Address A0 – A9	4 – 10					See note 4
$\overline{RAS}$, $\overline{CAS}$, WE	40 – 45					
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}= –2.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA

NOTE1. Acquisition window is wider when sliced data is supplied to DATA I/O to accommodate satellite transmissions.
NOTE 2 XCK output will be 6.9375MHz with XCKH=0 in register TADD, or 13.875Mhz with XCKH=1.
NOTE 3. CSO output voltage when in Picture or Mix modes will depend on the size of the video signal applied to VSI pin 32, together with the attenuation due to the internal video switch (30Ω nom) and the external load on pin 31. In these modes the video signal at pin 32 is switched straight through to pin 31. The maximum current allowed through the video switch is 24 mA.
NOTE 4. Capacitive loading on $\overline{RAS}$ and $\overline{CAS}$ should not exceed 20pF per pin.

Output voltage high specification ensures the output will also drive TTL levels of V_{DD}–2.1V at the specified current.

Pin N0	Name	Pin Description
1, 24	V_{SS}	Power ground 0V, both pins must be connected.
2, 3, 46, 47	DQ1–4	DRAM data lines, with internal 75k pull–up resistors.
4	$\overline{WE}$	DRAM write enable.
5	$\overline{RAS}$	DRAM row address strobe.
6–10, 40–44	A9, A0–8	DRAM address outputs.
11	ONH	On hours output.
12	$\overline{XTI}$	Crystal input or external clock input.
13	XTO	Crystal output.
14	XCK	Divided output of VCO clock, default 6.9375MHz. If XCKH bit in TADD register is set high, the output is 13.875MHz.
15	VIN	Vertical sync input positive pulse. If bit VINV in MODE register is set high, the signal may be a negative pulse.
16	HIN	Horizontal sync input positive pulse. If bit HINV in MODE register is set high, the signal may be a negative pulse.
17	EVEN/TEST	Even output is enabled by bits IOE and EOE in SYNCSW register. If EVEN output is not used it should be left open circuit. TEST input is used for factory testing. An internal 75k pull–down resistor is included.
18	EXT/$\overline{INT}$	Control pin for SYNC I/O and DATA I/O, with internal 75k pull–down. When high, supply sliced sync and data.
19	CAP0	Black level reference capacitor.
20	VIDEO IN	PAL composite signal with negative syncs.
21	VSSA	Analog ground.
22	SYNC I/O	Sliced sync input/output, (open drain output).
23	DATA I/O	Sliced data input/output, (push–pull output).
25, 48	V_{DD}	Power, +4.5V to +5.5V, both pins must be connected.
26	$\overline{RESET}$	Active low reset input, with 75k pull up–resistor.
27	BLN	Blanking output, high power push–pull driver.
28	RED	Red output, high power push–pull tri–state driver.
29	GRN	Green output, high power push–pull tri–state driver.
30	BLUE	Blue output, high power push–pull tri–state driver.
31	CSO	Composite sync output generated in text modes. In picture modes, connected to VSI through <30Ω video switch, see Fig. 6.
32	VSI	Composite video switch input.
33	$\overline{EVENT}$	Active low open drain output interrupt to microcontroller, with internal 75k pull–up.
34	SCL	Standard I^2C bus serial clock input.
35	SDA	Standard I^2C bus serial data input/output. Address is 0010 001R/$\overline{W}$ (22hex).
36	TEST2	For factory test only, do not connect.
37	TEST3	For factory test only, do not connect.
38	TEST4	For factory test only, do not connect.
39	TEST5	for factory test only, do not connect.
45	$\overline{CAS}$	DRAM column address strobe.

PINS	TEST	TEST LEVELS	NOTES
SDA &SCL	Human body model	1kV on 100pK through 1k5Ω	<15% LTPD
SDA & SCL	Machine model	100V on 200pF through 0Ω & <500nH	
All others	Human body model	2kV on 100pF through 1k5Ω	Meets Mil Std. 883D class 2 requirements
All others	Machine model	200V on 200pF through 0Ω & <500nH	

LTPD=Lot Tolerant Percent Defective

ESD data

ADDRESS dec/hex	REGISTER NAME	7	6	5	4	3	2	1	0	R/W	DEFAULT hex
	RADD	A17	A16	IAI	RA4	RA3	RA2	RA1	RA0	W	00
0/0	ACONA	ACQ	MGC	PBC	PAC	SDC	SCC	SBC	SAC	W	F0
1/1	STORA	STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0	W	02
2/2	PGS1A	SCS3	SCS2	SCS1	SCS0	SAS3	SAS2	SAS1	SAS0	W	00
3/3	PGS2A	MS2	MS1	MS0	SDS1	SDS0	SBS2	SBS1	SBS0	W	20
4/4	PGS3A	PBS3	PBS2	PBS1	PBS0	PAS3	PAS2	PAS1	PAS0	W	00
5/5	ACONB	$\overline{\text{HLD}}$	MGC	PBC	PAC	SDC	SCC	SBC	SAC	W	F0
6/6	STORB	STB7	STB6	STB5	STB4	STB3	STB2	STB1	STB0	W	03
7/7	PGS1B	SCS3	SCS2	SCS1	SCS0	SAS3	SAS2	SAS1	SAS0	W	00
8/8	PGS2B	MS2	MS1	MS0	SDS1	SDS0	SBS2	SBS1	SBS0	W	00
9/9	PGS3B	PBS3	PBS2	PBS1	PBS0	PAS3	PAS2	PAS1	PAS0	W	88
10/A	RECON	WI0	WI24	WI25	PINB	PINA	FF	CDB	CDA	W	00
11/B	DISCON1	INV	RLH	DSB	CLS	CUR	BLC	LS3	UDI	W	00
12/C	DISCON2	LS0	LS1	LS2	MGS	IHD	SPH	BX1	BX0	W	00
13/D	DISCON3	TXT	MIX	INT	REV	UDK	SPOS	ST2	ST1	W	00
14/E	DISCON4	BXP	BXH	BXT	BXS	DHT	DHB	SG2	SG1	W	00
15/F	HADD	A15	A14	A13	A12	A11	A10	A9	A8	W	00
16/10	LADD	A7	A6	A5	A4	A3	A2	A1	A0	W	00
17/11	WDATA	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	W	00
19/13	SCROLL	WI29	MV	CRL	SRA4	SRA3	SRA2	SRA1	SRA0	W	00
20/14	SYNCSW	ESS	–	BXSDEL	CSOT	IOE	EOE	SEN	SVS	W	00
21/15	MODE	MD3	MD2	MD1	312:313	VHLD	HVEN	HINV	VINV	W	24
22/16	TADD	–	A18	RESET	XCKH	2K/ST	DISC	ADEC	DST8	W	00
23/17	DISPST	DSTI7	DST6	DST5	DST4	DST3	DST2	DST1	DST0	W	00
24/18	DPOS	V3	V2	V1	V0	H3	H2	H1	H0	W	7B
25/19	ENABLE	NPR	VHR	830	X/24A	X/28	X/27	X/26	X/24B	W	EE
26/1A	ACCENT	APA	APB	C8APIA	C8APIB	SCAPIA	SCAPIB	–	AHEN	W	00
0/0	EVENTA	NPR	VHR	830A	X/24	X/28	X/27	X/26	C8	R	–
1/1	EVENTB	NPR	VHR	830B	X/24	X/28	X/27	X/26	C8	R	–
2/2	CBITSA	C14	C13	C12	C11	C10	C7	C6	C5	R	–
3/3	PGR1A	SCR3	SCR2	SCR1	SCR0	SAR3	SAR2	SAR1	SAR0	R	–
4/4	PGR2A	MR2	MR1	MR0	SDR1	SDR0	SBR2	SBR1	SBR0	R	–
5/5	PGR3A	PBR3	PBR2	PBR1	PBR0	PAR3	PAR2	PAR1	PAR0	R	–
6/6	CBITSB	C14	C13	C12	C11	C10	C7	C6	C5	R	–
7/7	PGR1B	SCR3	SCR2	SCR1	SCR0	SAR3	SAR2	SAR1	SAR0	R	–
8/8	PGR2B	MR2	MR1	MR0	SDR1	SDR0	SBR2	SBR1	SBR0	R	–
9/9	PGR3B	PBR3	PBR2	PBR1	PBR0	PAR3	PAR2	PAR1	PAR0	R	–
10/A	HAMMC	HC7	HC6	HC5	HC4	HC3	HC2	HC1	HC0	R	FF
17/11	RDATA	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	R	–
18/12	EXTEND	APIIA	APIIB	RSIND	–	CLSI	ONH	C9B	C9A	R	–
31/1F	STATUS	SL2	SL1	SL0	SR4	SR3	SR2	SR1	SR0	R	–

Table 1. Register details

WRITE REGISTERS

RADD

A17–16	Memory address
IAI	Inhibit auto increment
RA5–0	Register address

ACON A/B

ACQ	Acquisition on
MGC	Magazine compare
PBC	Page tens compare
PAC	Page units compare
SDC	Sub–code compare digit D
SCC	Sub–code compare digit C
SBC	Sub–code compare digit B
SAC	Sub–code compare digit A
HLD	Hold display

PGS 1,2,3 A/B

SAS3–0	Sub–code digit A (LSD) select
SBS2–0	Sub–code digit B select
SCS3–0	Sub–code digit C select
SDS1–0	Sub–code digit D (MSD) select
PAS3–0	Page (units) select
PBS3–0	Page (tens) select
MS2–0	Magazine select

RECON

WI0	Write inhibit packet 0
WI24	Write inhibit packet 24
WI25	Write inhibit packet 25
PINB	Parity check inhibit Acquisition B
PINA	Parity check inhibit Acquisition A
FF	Full Field mode
CDB	Clear store disable Acquisition B
CDA	Clear store disable Acquisition A

DISCON1

INV	Invert display colours
RLH	Roll headers
DSB	Display acquisition circuit B (A if zero)
CLS	Clear current display store
CUR	Cursor enable
BLC	Block cursor
LS3	Language group select
UDI	Display update indicator

DISCON2

LS2–0	Language select
MGS	Magazine serial
IHD	Inhibit display rows 1–25
SPH	Suppress header
BX1–0	Boxing control bits

DISCON3

TXT	Text/ not picture
MIX	Mix text and picture
INT	Text interlace sync mode
REV	Reveal hidden text
UDK	Update key – inhibit rows 0–25
SPOS	Status line 2 position, top if set high
ST2	Display status line 2
ST1	Display status line 1

DISCON4

BXP	Box page number
BXH	Box header
BXT	Box time
BXS	Box status rows
DHT	Double height top
DHB	Double height bottom
SG2–1	Separated graphics control bits

HADD & LADD

A15–0	Memory address

WDATA

WD7–0	Write data byte to memory

SCROLL

WI29	Write inhibit packet 29
MV	Majority vote on framing code
CRL	Cursor lock
SRA4–0	Scroll value 0–23 only

SYNCSW

ESS	External sync source
BXSDEL	Box status delay by one character
CSOT	CSO TTL signal
IOE	Interlace output enable
EOE	Even output enable
SEN	Select enable SVS
SVS	Select VSI input as sync source

MODE

MD3	H sync mode 3
MD2	H sync mode 2
MD1	H sync mode 1
312:313	Non–interlace 312:313 mode
VHLD	Vertical sync half line delay (Fig. 9)
HVEN	H and V inputs enable
HINV	H invert
VINV	V invert

TADD

A18	Memory address
RESET	Reset to default state
XCKH	XCK output 13.875MHz or 6.9375MHz when low
2K/ST	2K/store mode
DISC	Disconnect display from acquisition
ADEC	Automatic memory decrement
DST8	Store number for display bit 8

DISPST

DST7–0	Store number for display bits 7–0

DPOS

V3–0	Vertical position in 2 line steps
H3–0	Horizontal position in 4 pixel steps

ENABLE

NPR	Enable NPR flag in read regs
VHR	Enable VHR flag in read regs
830	Enable 830 flag i read regs
X/24A	Enable X/24A flag in read regs
X/28	Enable X/28 flag in read regs
X/27	Enable X/27 flag in read regs
X/26	Enable X/26 flag in read regs
X/24B	Enable X/24 flag in read regs

ACCENT

APA–B	Accent protection A/B
C8APIA–B	C8 accent protection inhibit A/B
SCAPIA–B	Sub–code accent protection inhibit A/B
AHEN	Advanced headers enable

READ REGISTER

EVENT A/B

NPR	New page received flag
VHR	Valid header received flag
830A	Packet 8/30 format 1 received flag
830B	Packet 8/30 format 2 received flag
X/24	Packet X/24 received flag
X/28	Packet X/28 received flag
X/27	Packet X/27 received flag
X/26	Packet X/26 received flag
C8	Update indicator

PGR 1,2,3 A/B

SAR3–0	Sub–code digit A (LSD) received
SBR2–0	Sub–code digit B received
SCR3–0	Sub–code digit C received
SDR1–0	Sub–code digit D (MSD) received
PAR3–0	Page (units) received
PBR3–0	Page (tens) received
MR2–0	Magazine received

RDATA

RD7–0	Read data byte from memory

CBITS A/B

C14–12	Language select bits (C14 is LSB)
C11	Magazine serial
C10	Inhibit display
C7	Suppress header
C6	Sub–title
C5	News flash

HAMMC

HC7–0	Hamming counter

EXTEND

APII A/B	Accent protection inhibit indication A/B
RSIND	Reset indication
CLSI	Clear screen indicator
ONH	On hours flag
C9 A/B	Interrupted sequence bit Acq A/B

STATUS

SL2–0	Status language indication
SR4–0	Status revision indication
SL2–0=003	All Europe version

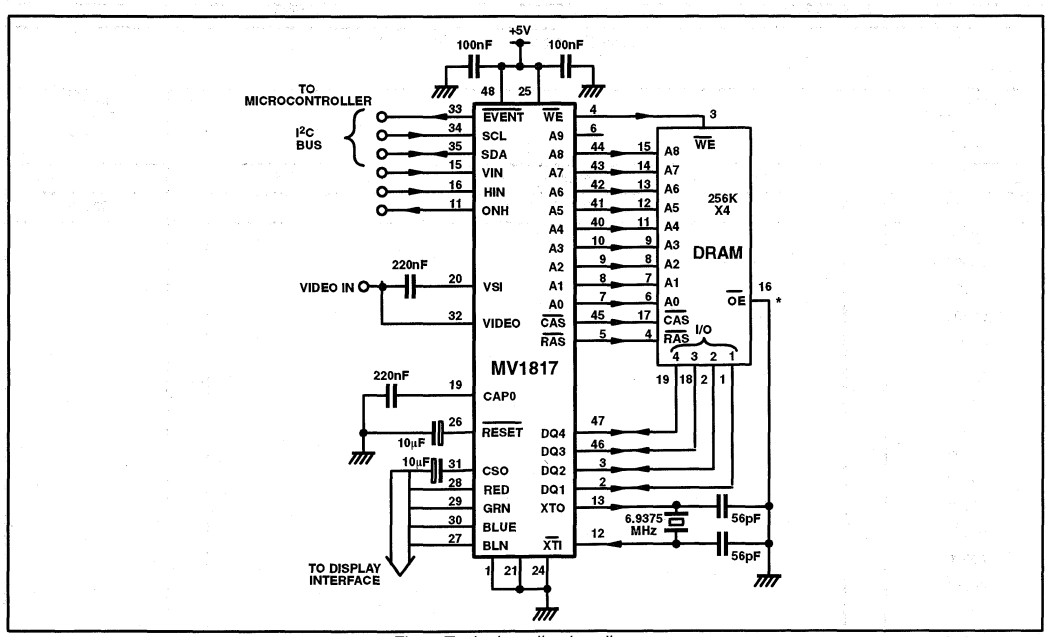


Fig. 3 Typical application diagram

* Note, on some DRAM devices $\overline{OE}$ should not be low during a write cycle. An inverted $\overline{WE}$ can be connected to $\overline{OE}$ in such cases.

I²C bus Interface – SCL and SDA.
Control of the MV1817 registers is through this interface. The I²C bus address is 0010 001 R/W

The circuit works as a slave transmitter with bit eight set high or as a slave receiver with bit eight set low. In receive mode, the first data byte is written to RADD register, where the least significant five bits form the sub–address. The most significant three bits of RADD are data bits, see Table 1.

Automatic incrementing of the registers allows successive data bytes to be written to, or read from the registers. The automatic incrementing can be disabled by setting IAI bit five of RADD to one. Automatic increment can be changed to automatic decrement (for DRAM address NOT registers) by setting ADEC bit high in TADD register. All DRAM addresses may be accessed via the I²C bus interface.

When WDATA or RDATA registers are reached, the automatic incrementing accesses successive bytes of data in the DRAM starting from the current value of HADD and LADD. Automatic incrementing of registers will operate above WDATA from SCROLL register onwards.

MEMORY MAPS

The DRAM memory as viewed from the I²C bus is organised in 1024 (400hex) byte blocks, referred to as a store. Stores 0 and 1 in 1K/store mode are reserved for the non–display packets from acquisition A and B respectively. Stores A0 and B0 in 2K/store mode are reserved for the packets X/29 and 8/30 from acquisition A and B respectively.

The table below shows the start addresses for each store. The store numbers relate to the values in the STORA, STORB and DISPST registers.

1K/store	Start addresses hex TADD, RADD, HADD, LADD	2K/store
STORE 0	0 0 00 00	STORE A0
STORE 1	0 0 04 00	STORE B0
STORE 2	0 0 08 00	STORE 1 DISPLAY
STORE 3	0 0 0C 00	STORE 1 EXT PKTS
STORE 4	0 0 10 00	STORE 2 DISPLAY
STORE 5	0 0 14 00	STORE 2 EXT PKTS
STORE 6	0 0 18 00	STORE 3 DISPLAY
STORE 7	0 0 1C 00	STORE 3 EXT PKTS
	etc. until	
STORE 508	1 3 F0 00	STORE 254 DISPLAY
STORE 509	1 3 F4 00	STORE 254 EXT PKTS
STORE 510	1 3 F8 00	STORE 255 DISPLAY
STORE 511	1 3 FC 00	STORE 255 EXT PKTS

Table 2 Memory organisation

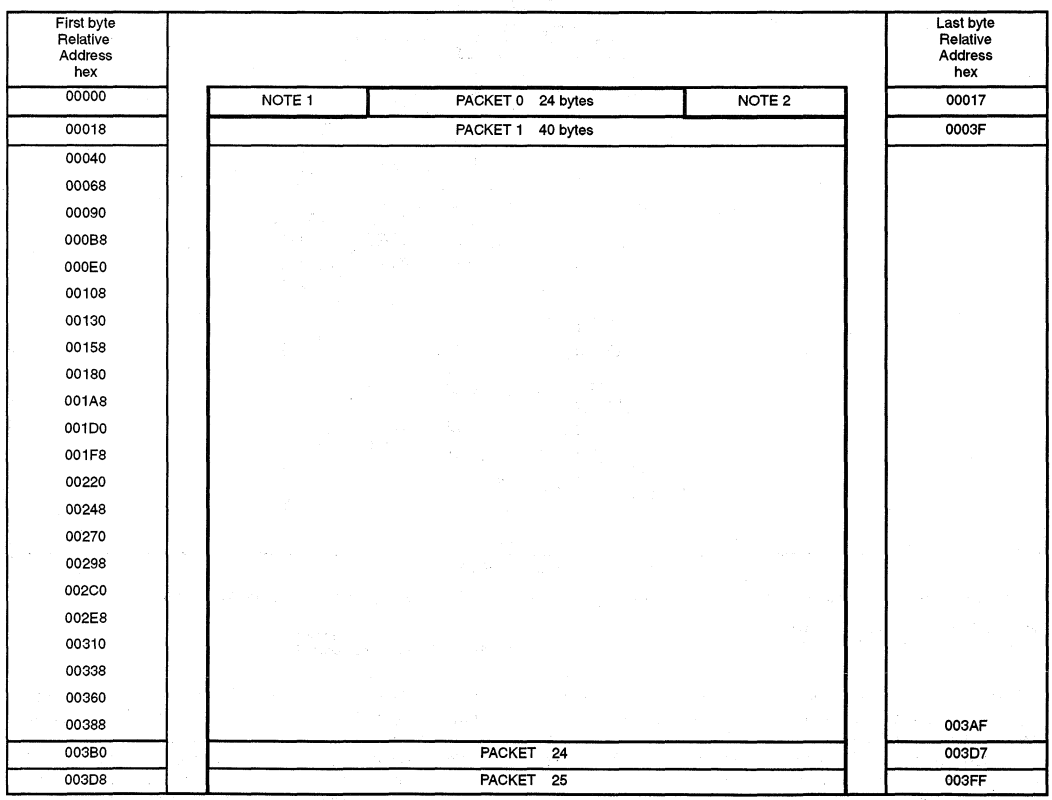


Fig. 4. Organsation of DISPLAY memory

Note 1. Page number, 8 bytes from store 0 (A0) with absolute addresses 000 to 007

Note 2. Time display, 8 bytes from store 0 (A0) with absolute addresses 008 to 00F

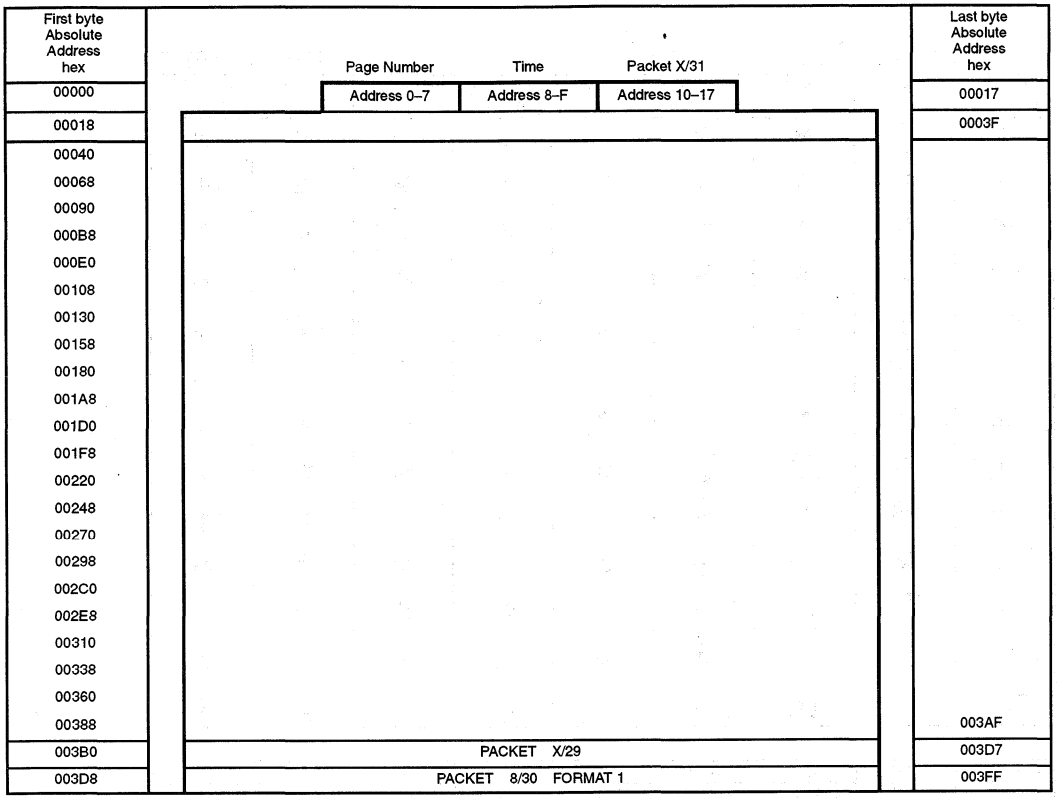


Fig. 5. Store 0 (A0) Memory organisation.

NOTE: Store 1 (B0) is organised similarly except that, in 1K/store mode it accepts acquisition circuit B packets X/26 etc. and packet 8/30 format 2 in the last row. To obtain addresses for store 1 (B0) add 400hex. Bytes 400 to 417hex are not used in store 1 (B0).

In 2K/store mode, all page related extension packets, X/26, X/27 and X/28, are directed to the store adjacent to the display store, see Table 2. Up to 23 of these packets are stored in the order received with no fixed location in the memory. The first four bytes with relative address 000 to 003 contain a copy of the related acquisition circuit data in CBITS and PGR1–3 registers in the same order. Bytes 004 to 017_{hex} are not used by the MV1817. The last two rows will not be used by the MV1817 since X/29 and 8/30 packets only go to stores A0 and B0 (or to stores 0 and 1 in 1K/store mode).

Synchronisation

In the usual configuration where a video signal is applied to the data and sync slicer, a composite sync output (CSO) is generated from the sliced video input. CSO can be modified by register bits to provide 312:312, 312:313 or 312.5:312.5 text syncs, or switch through the video switch input signal direct. If video syncs are selected with SEN=1 and SVS=1 (in SYNCSW register), the action of the 312:313 bit (in MODE register) is inhibited.

When the vertical synchronisation circuit finds a field sync datum, (see Fig. 6) it is disabled for 64 lines so that double field synchronisation is avoided.

If the display is to be synchronised to horizontal and vertical signals via the HIN and VIN pins, the HVEN enable bit in the MODE register must be set high. This will disable the action of interlace (INT) bit in DISCON3 register and also 312:313 bit in MODE register. HIN and VIN signals are normally positive pulses, but inverted signals may be applied provided that the appropriate HINV and VINV bits are set high in the MODE register. The leading edge of VIN pulse is sampled at –4.7µs and +27.3µs with respect to HIN pulse to establish which is the EVEN or ODD field, see Fig. 7. The VIN pulse should be at least 32µs minimum and the HIN pulse 1µs minimum.

If required, the vertical pulse may be delayed by half a line period by setting VHLD bit high in MODE register, see Fig. 8.

LS(3210)	0000	0001	0010	0011	0100	0101	0110	0111
TABLE POSITION	ENGLISH	GERMAN	SWEDISH FINNISH	ITALIAN	FRENCH (BELGIAN)	SPANISH	CZECH	ROMANIAN
2/3	£	#	#	£	é	ç	#	#
2/4	$	$	¤	$	ï	$	ů	$
4/0	@	§	É	é	à	¡	č	Ţ
5/B	←	Ä	Ä	°	ë	á	ť	Â
5/C	½	Ö	Ö	ç	ê	é	ž	Ş
5/D	→	Ü	Å	→	ù	í	ý	Ă
5/E	↑	^	Ü	↑	î	ó	í	ţ
5/F	#	_	_	#	#	ú	ř	ı
6/0	■	°	é	ù	è	¿	é	ţ
7/B	¼	ä	ä	à	â	ü	á	â
7/C	▮	ö	ö	ò	ô	ñ	ě	ş
7/D	¾	ü	å	è	û	è	ú	ă
7/E	÷	ß	ü	ì	ç	à	š	î

LS(3210)	1000	1001	1010	1011	1100	1101	1110	1111
TABLE POSITION	POLISH	GERMAN	HUNGARIAN	TURKISH	DANISH	SERBO CROAT	CZECH	SOUTH AFRICAN
2/3	#	#	#	₺	£	#	#	£
2/4	ń	$	ú	ğ	$	$	ů	$
4/0	ą	§	É	İ	@	Č	č	ŉ
5/B	Ƶ	Ä	í	Ş	Æ	Ć	ť	ë
5/C	ś	Ö	Ö	Ö	Ø	Ž	ž	ê
5/D	ł	Ü	Á	Ç	Â	Đ	ý	ü
5/E	ć	^	ű	Ü	↑	Š	í	é
5/F	ó	_	ő	Ğ	#	ë	ř	ï
6/0	ę	°	é	ı	■	č	é	š
7/B	ż	ä	ó	ş	æ	ć	á	ä
7/C	ś	ö	ö	ö	ø	ž	ě	ô
7/D	ł	ü	á	ç	å	đ	ú	û
7/E	ź	ß	ü	ü	÷	š	š	ö

Table 3 Narional Optional Characters. Language version 003.

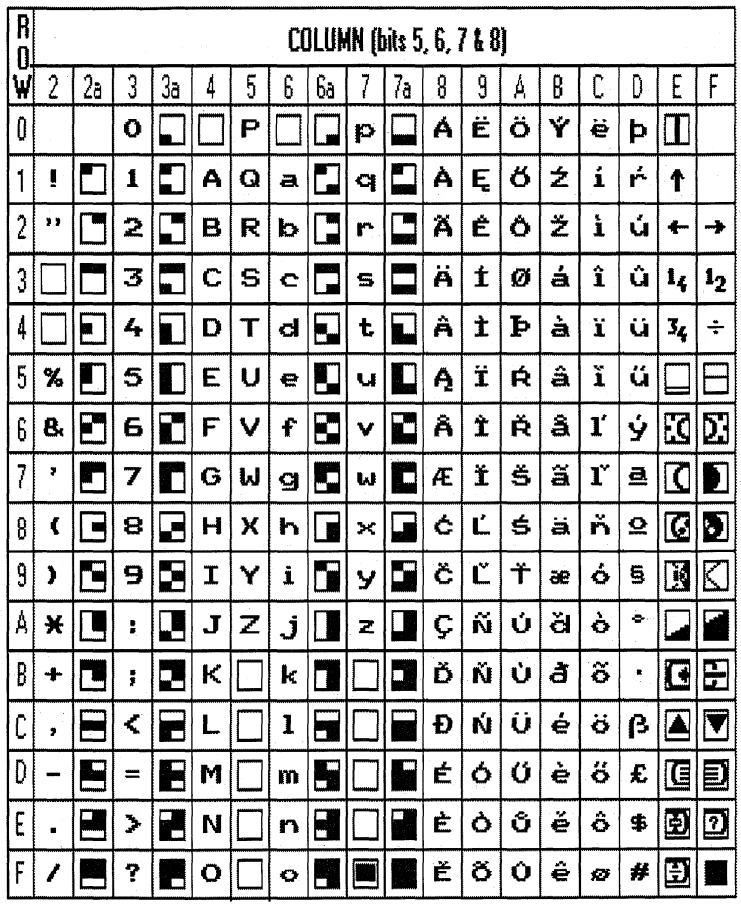


Table 4. Character ROM contents as viewed by the display. Language version 003.

Notes: Character positions F0 and F1 will be displayed as spaces, but are actually spacing control codes, like the control columns 0 and 1 listed in table 6.
F0 is UNDERLINE start / stop code.
F1 is INVERT display colours start / stop code.
FF is displayed as all foreground.
☐ Characters in these positions are displayed according to the setting of LS(0–3) bits, see table 3.
When graphics mode is set, columns 2a, 3a, 6a & 7a are displayed as the graphic symbols shown with black as forground colour. All other columns are displayed normally. The graphic symbols are shown above with a border which is not present when the symbol is displayed on the screen.

Graphic symbols to scale

Page closure.

In serial mode, any header will close a page being received.
In parallel mode, only a header from the selected magazine will close a page being received.

Advanced Header and Instant Page Clear transmission systems.

With these systems, the main page header packet is transmitted in the same VBI, before the associated data packets, without the standard 20ms page clearing interval. The MV1817 can be programmed to protect those associated data packets, in the same VBI, from erasure when the page is cleared. This feature is enabled for both systems by setting AHEN bit high in ACCENT register.

	INCLUDED IN MV1817- 3	NOT INCLUDED
CZECH	Ä Á Č Ď É Ě Í Ĺ Ľ Ň Ö Ó Ô Ŕ Ř Š Ś Ť Ü Ú Ů Ý Ź Ž ß $ ° ä ď ĺ ľ ň ö ó ô ŕ ü	
DENMARK	Æ æ Ø ø	
FRANCE	À Â Ç È É Ê Ë Ï Î Ô Û	Œ œ
HOLLAND	Ë ë	Ĳ ĳ
HUNGARY	Á Í Ó Ő Ú Ű á í ó ő ú ű	
ICELAND	Á Đ Í Ó Ö Þ Ú Ý Æ Ø ð ö þ ý æ ø	
ITALY	À È É Ì Í Ò Ù Ú í ú	
POLAND	Ą Ć Ę Ń Ó Ź $ § _	
ROMANIA	É Ě Ê Ĭ Ó é ě ê ĭ ó	
SPAIN	Á À Ã Ç É È Ï Í Ñ Ó Ò Õ Ŕ Ú Ü # ·ª º → ↑ ã ä â ë ê ï î ô ò ö õ ŕ û	
TURKEY	Â Î Û â î û	

Table 5. Additional characters for the languages shown. Language version 003.

Accented characters added via X/26

These can be automatically locked in place on the screen by the MV1817 hardware, so that further reception of the page will not change accented characters to the level one fall–back characters. Whenever a page is cleared to spaces, the locked characters will be unlocked and also become spaces. Control of this feature is by setting APA/B bits in ACCENT register. The header should be cleared by software the first time a store is used to prevent random characters in the DRAM at power up from being locked. For pages where data is updated with C8 set, but clear page C4 is not set, the accent locking feature may be inhibited during current page reception by setting C8APIA/B bits. For rolling sub–coded pages where clear page C4 is not set, the accent locking feature may be inhibited during current page reception by setting SCAPIA.B bits. When these inhibit mechanisms are active, an indication is provided in EXTEND register by bits APIIA/B set high. They are set low when the current page is closed.

	0	1
0	Alpha Black	Graphic Black
1	Alpha Red	Graphic Red
2	Alph Green	Graphic Green
3	Alpha Yellow	Graphic Yellow
4	Alpha Blue	Graphic Blue
5	Alpha Magenta	Graphic Magenta
6	Alpha Cyan	Graphic Cyan
7	Alpha White [1]	Graphic White
8	Flash	Conceal Display [2]
9	Steady [1 2]	Contiguous Graphics [1 2]
A	End Box [1]	Separated Graphics [2]
B	Start Box [3]	No Action
C	Normal Height [1 2]	Black Background [1 2]
D	Double Height	New Background [2]
E	No Action	Hold Graphics
F	No Action	Release Graphics

Table 6. Control codes.

Notes:
1. Presumed set at the start of each display row.
2. Action "set at the current space", others are "set after the current space".
3. Two consecutive codes are transmitted, action takes place between them.

Sync switch register truth table

ESS	SEN	SVS	CSO output
0	0	X	VSI or digital sync selected by algorithm
0	1	0	Digital syncs
0	1	1	VSI switched through
1	X	X	Digital syncs from SYNC I/O

X=don't care.

Sync switch algorithm

The video signal will be switched through from VSI to CSO when:
TXT = 0 or MIX = 1 or TXT = 1 and BX1 = 1 and BX0 = 1.

EVEN output on TEST pin, truth table

IOE	EOE	CSO	Function
X	0	X	TEST configured as an input with an internal pull down resistor
0	1	INTERLACE	Enables EVEN output, which is held high.
1	1	INTERLACE	Enables EVEN output going high during the first field (lines 1–312½)
X	1	312:313	Enables EVEN output going high during the short field (312 lines)

X = don't care.

Note: CSO is not only dependent upon the state of the INT bit in DISCON4 register, but also on MIX and any other register bits which cause picture to be displayed, for example, UDK, BXP, BXH, BXT, BXS, or BX0–1 if start box codes are present on screen.

BOXING options and MIX mode, truth table

The bits BXP, BXH, BXT and BXS in DISCON4 register will BOX text into the picture when TXT and MIX mode are set, the BOXED text will retain its background colours. However, BOXED text using Box codes 0B in text together with BX0 or BX1 bits in DISCON2 will not override MIX and can be displayed as BOXED text by setting TXT & MIX bits low, or MIXED by setting MIX high. The BOXED STATUS ROWS can start at character position one by setting BXSDEL bit in SYNCSW register.

TXT	BX – 1.0		BX – n (n=P, H, T, S)	MIX	Status Area n	Boxed Text Areas		BASIC MODE
						Outside	Inside	
0	0.0		0	X	Picture	Picture	Picture	PICTURE
0	0.0		1	0	Boxed	Picture	Picture	
0	0.0		1	1	Mixed	Picture	Picture	
0	X.1	1.X	0	0	Picture	Picture	Text	NEWSFLASH
0	X.1	1.X	0	1	Picture	Picture	Mixed	
0	X.1	1.X	1	0	Boxed	Picture	Text	
0	X.1	1.X	1	1	Boxed	Picture	Mixed	
1	0.X	X.0	X	0	Text	Text	Text	TEXT
1	0.X	X.0	0	1	Mixed	Mixed	Mixed	
1	0.X	X.0	1	1	Boxed	Mixed	Mixed	
1	1.1		X	0	Text	Text	Picture	WINDOW
1	1.1		0	1	Mixed	Mixed	Picture	
1	1.1		1	1	Boxed	Mixed	Picture	

X = don't care.

BOX STATUS DELAY

When status rows 1 and/or 2 are enabled to be boxed into a picture or MIX text display, the first character in the row may be omitted and replaced by picture by setting the BXSDEL bit 5 in SYNCSW register high

SCROLL

A value in the range 0–23 can be used to move the text rows 1–23 up the screen, the rows 0, 24 and 25 remain fixed. A scroll value of 3 will cause text row 4 to be displayed in row 1. Text rows 1–3, in this example will appear in rows 21, 22 and 23 respectively. If half page expand is also used, by setting DHT in DISCON3 register, the text screen can be made to scroll through the expanded top half window. The position of the text in memory, is not affected by scroll, only the row addressing is changed to effect the display.

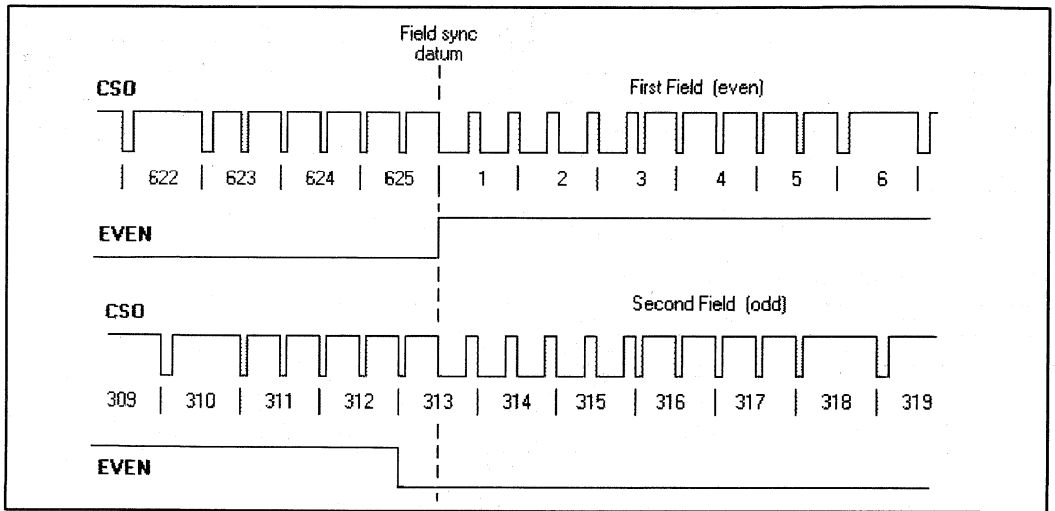


Fig. 6a. Composite sync output (interlaced) and EVEN output.

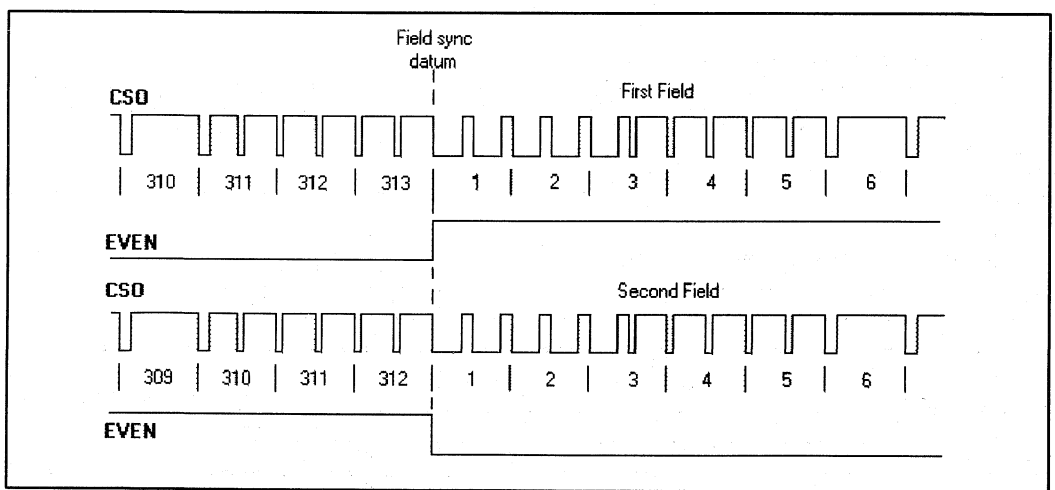


Fig. 6b. Composite sync output (non–interlaced 312:313) and EVEN output.

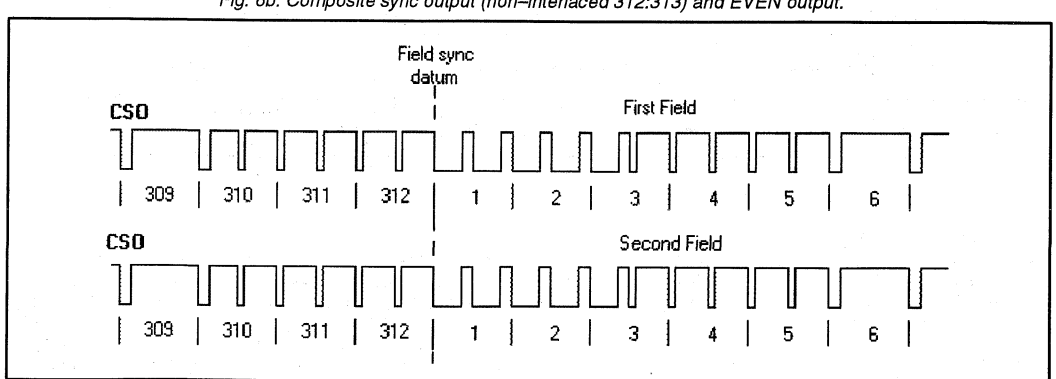


Fig. 6c. Composite sync output (non–interlaced 312:312).

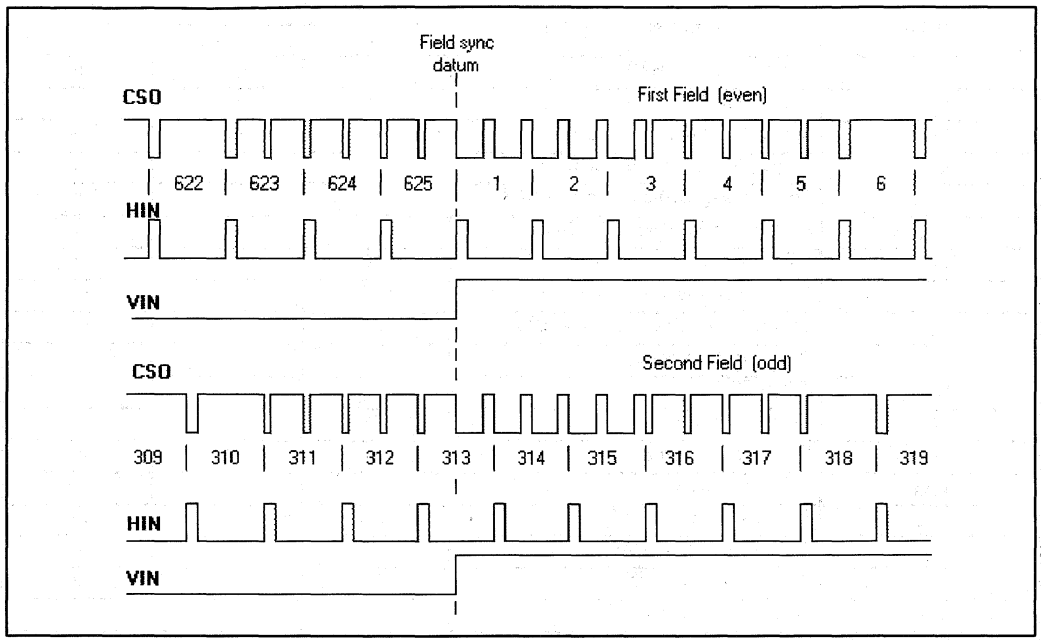


Fig. 7. Horizontal and Vertical input waveforms.

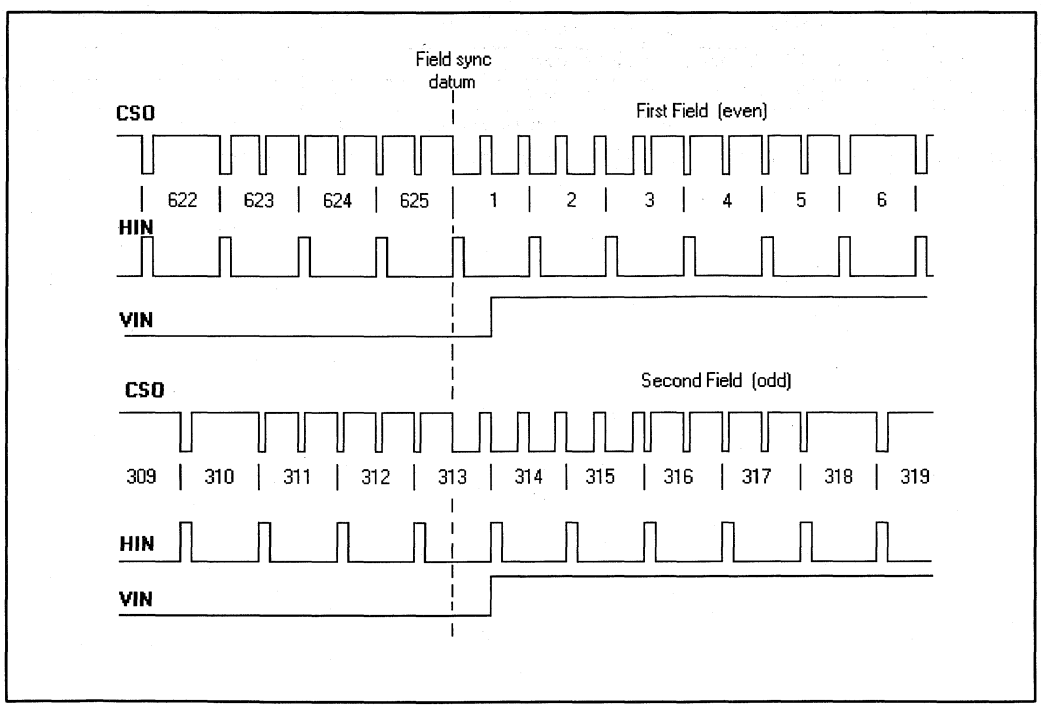


Fig. 8. Horizontal and Vertical input waveforms with Vertical Half Line Delay bit set.

Symbol	Parameters Description	Value for DRAM		Units
		Min	Max	
t_{RAC}	Access time from $\overline{RAS}$		<106	ns
t_{CAC}	Access time from $\overline{CAS}$		<43	ns
t_{CAA}	Access time from column address		<61	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge		<72	ns
t_{ASR}	Row address set–up time before $\overline{RAS}$	<27		ns
t_{RAH}	Row address hold time after $\overline{RAS}$	<45		ns
t_{RSH}	$\overline{RAS}$ hold time	<36		ns
t_{ASC}	Column address set–up time before $\overline{CAS}$	<18		ns
t_{CAH}	Column address hold time after $\overline{CAS}$	<54		ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	<72		ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay	<63		ns
t_{RP}	$\overline{RAS}$ precharge time	<81		ns
t_{CP}	$\overline{CAS}$ precharge time	<27		ns
t_{CAS}	$\overline{CAS}$ low pulse width	<45		ns
t_{RAS}	$\overline{RAS}$ low pulse width	<171		ns
t_{DS}	Data set–up before $\overline{CAS}$	<18		ns
t_{DH}	Data hold time after $\overline{CAS}$	<54		ns
t_{WCS}	Write set–up before $\overline{CAS}$	<72		ns
t_{WCH}	Write hold time after $\overline{CAS}$	<72		ns
t_{PC}	Page mode cycle time	<72		ns
t_{REF} – 64Kx4	Refresh cycle time per $\overline{RAS}$ address		>1.033	ms
t_{REF} – 256Kx4	Refresh cycle time per $\overline{RAS}$ address		>2.066	ms
t_{REF} – 1Mx4	Refresh cycle time per $\overline{RAS}$ address		>4.133	ms

Table 7. Timing parameter required for DRAM.

NOTE: Timings are for nominal center points on edges, so care should be taken not to load the pins.

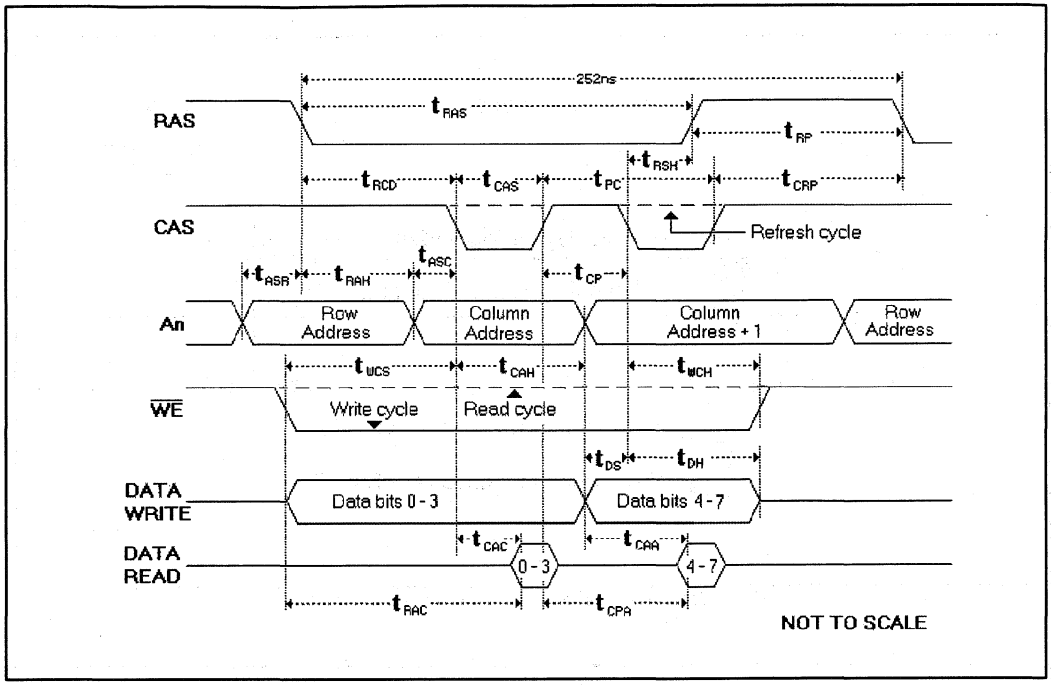


Fig. 9 DRAM interface.

DISPLAY STORE

The MV1817 has two modes of operation defined by the setting of DISC bit in TADD register.

1. With DISC set low, the display store is tied to acquisition circuit A, if DSB bit in DISCON1 register is low, or to acquisition circuit B if DSB bit is set high. STORA or STORB defines the working store for both acquisition and display.

2. With DISC set high, the display store is disconnected from the acquisition circuits and controlled independently by the DISPST register, together with DST8 in TADD register.

The store number programmed into STORA, STORB or DISPST registers is internally adjusted to take account of 2K/STORE working, see table 2. However, the I^2C bus addresses for the DRAM data are NOT internally adjusted in 2K/STORE mode, see again table 2.

DISPLAY POSITION

This may be adjusted by changing the value in the DPOS register. The lower 4 bits control the horizontal position. The default state is Bhex and the step size is four pixels (0.288 µs). Incrementing by one moves the display right by four pixels. This means the display can be moved 16 pixels (1.153 µs) right and 44 pixels (3.171 µs) left from the default position 15.28µs from leading negative edge of the Composite Sync Output horizontal sync pulse, see Fig. 10.

The upper 4 bits control the vertical position and the line numbers are referred to the Field Sync Datum on the Composite Sync Output, see Fig. 6. The default state is 7hex and the step size is 2 TV lines. Incrementing by one moves the display up two TV lines. The default start position is TV line 46 for a 24 row display and TV line 36 for a 25 or 26 row display. The range of movement is 16 TV lines up and 14 TV lines down from the default starting position, see Fig. 11.

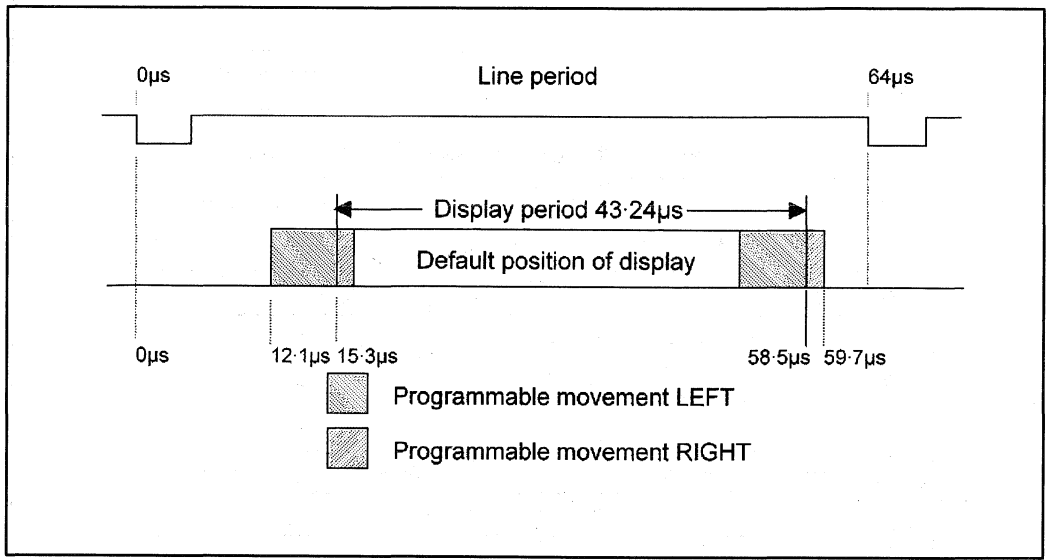


Fig. 10 Horizontal position and movement of text display.

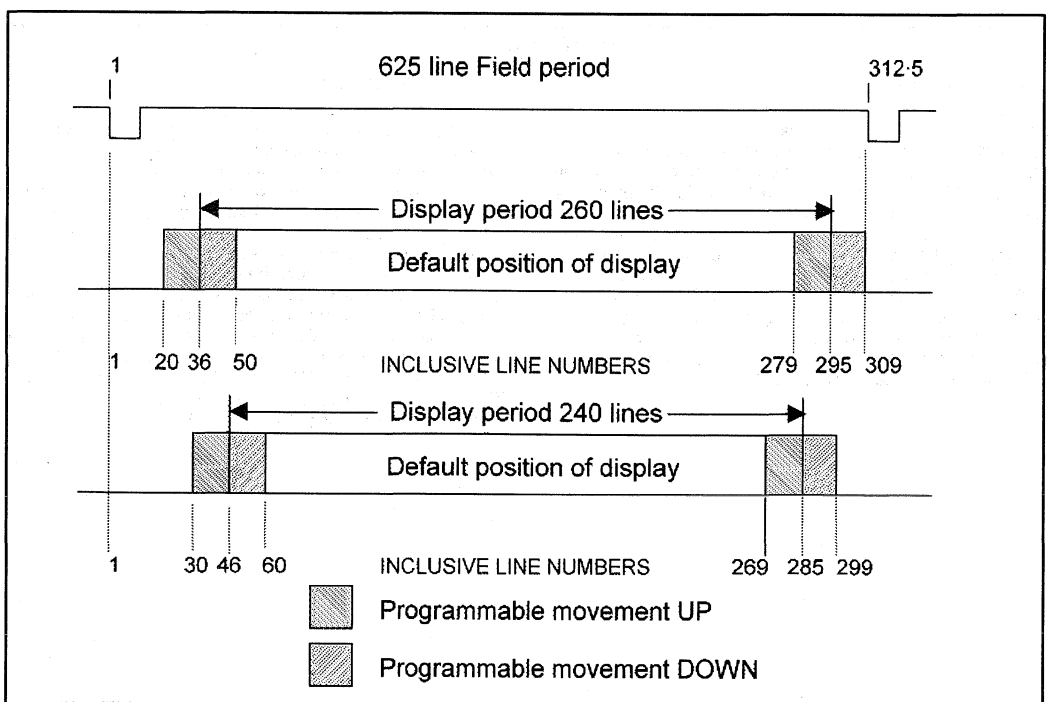


Fig. 11 Vertical position and movement of text display.

MV1820

VIDEO PROGRAMME DELIVERY CONTROL INTERFACE CIRCUIT

(Supersedes version in October 1995 Media IC Handbook, HB3120 - 3.0)

The MV1820 is a high speed CMOS receiver for Programme Delivery Control (PDC) messages broadcast in World System Teletext (WST) Format Two Broadcast Service Data Packets (BSDP). The PDC message can be read on an I²C bus with data format similar to standard Video Programming Service (VPS) decoders. Additional data is appended to include new PDC features.

It is intended for use in Video Cassette Recorders to provide automatic recording of suitably labelled Television programmes requested by the user.

FEATURES

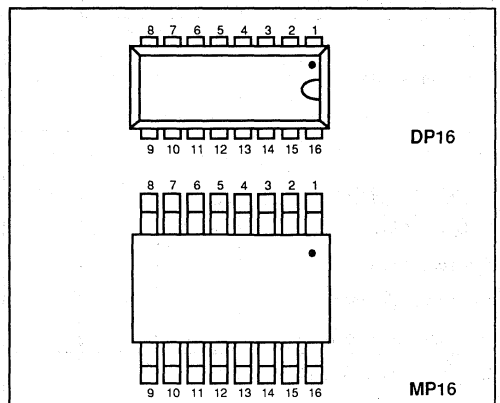
- On chip data slicing
- Low external component count
- I²C bus for low cost interfacing
- Advanced CMOS technology gives low power dissipation and high reliability

ABSOLUTE MAXIMUM RATINGS

Supply voltage	0.3V to 7V
All inputs	-0.3 to V_{DD} +0.3V
Operating temperature	0 to +70°C
Storage temperature	-55 to 125°C

ORDERING INFORMATION

MV1820F/CG/DPAS
MV1820F/CG/MPES



PIN	DESCRIPTION	PIN	DESCRIPTION
1	$\overline{\text{RESET}}$	16	$\overline{\text{XTI}}$
2	$\overline{\text{EXT/INT}}$	15	XTO
3	BLC	14	$\overline{\text{DAV}}$
4	WLC	13	SDA
5	VIDEO	12	VDD
6	GND	11	SCL
7	TCR	10	SYNC I/O
8	AS	9	DATA I/O

Fig.1 Pin connections - top view

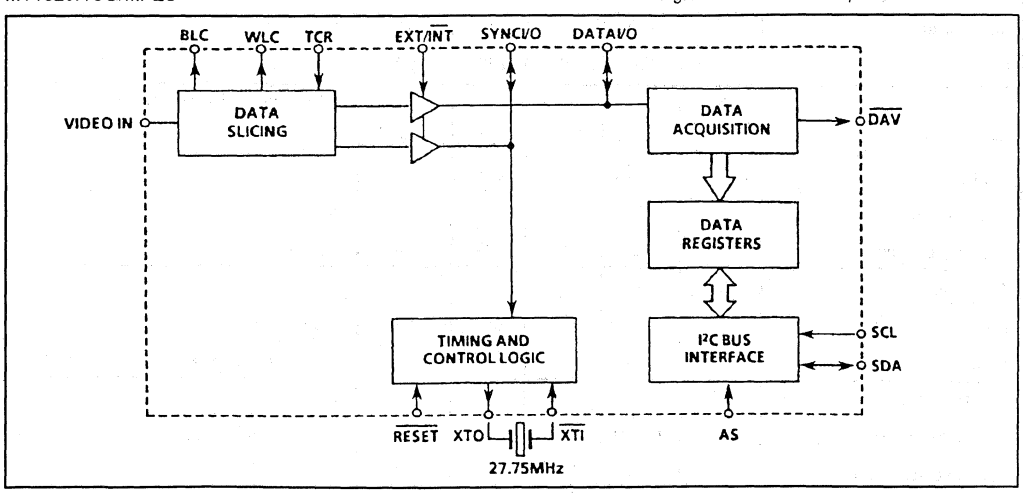


Fig.2 MV1820 block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)
T_{amb} = 0 to 70°C, V_{DD} = 5V ± 10%

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	12	4.5	5.0	5.5	V	
Supply current	12		20	25	mA	
Video input	5					
Video amplitude		0.8	1.8	3.0	Vpp	Bottom of sync to white (pk to pk)
Source impedance				250	Ω	
TCR input	7					
External resistance		4.7	4.7	200	kΩ	Connected to V_{DD}
BLC and WLC	3 & 4					
Capacitor value			10		nF	Connected to GND
Capacitor tolerance		-10%		+10%		
Effective series resistance				5	Ω	1MHz
DATA I/O and SYNC I/O	9 & 10					
Output voltage High		V_{DD}-1.0	4.5		V	I_{OH} = -1.2mA
Output voltage Low			0.2	0.4	V	I_{OL} = 2.4mA
Input voltage Low		0		0.8	V	
Input voltage High		V_{DD}-1.0		V_{DD}	V	
Input current		-30		+30	µA	V_{IN} = V_{SS} or V_{DD}
EXT/INT	2					100k (nom) pull-down resistor
Input voltage Low		0		0.8	V	
Input voltage High		V_{DD}-1.0		V_{DD}	V	
Input current Low		-10		+10	µA	V_{IN} = V_{SS}
Input current High		22	50	220	µA	V_{IN} = V_{DD}
AS	8					100k (nom) pull-down resistor
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}-1.0		V_{DD}	V	
Input current Low		-10		+10	µA	V_{IN} = V_{SS}
Input current High		22	50	220	µA	V_{IN} = V_{DD}
$\overline{XTI}$ Input	16					
Input current Low		-0.5	-5.0	-20	µA	-0.3<V_{IN}<V_{IL} max
Input current High		0.5	5.0	20	µA	V_{IH}min<V_{IN}<(V_{DD} + 0.3)
XTO Output	15					
Output voltage High		V_{DD}-1.0	4.5		V	I_{OH} = -1.0mA
Output voltage Low			0.2	0.4	V	I_{OL} = 2.0mA
Frequency			27.750		MHz	±100ppm

ELECTRICAL CHARACTERISTICS (continued)

These characteristics are guaranteed over the following conditions (unless otherwise stated)
T_{amb} = 0 to 70°C, V_{DD} = 5V ± 10%

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
I2C bus						
SCL, SDA Schmitt inputs	11, 13					Not clamped when V_{DD} = 0V
Input voltage Low		0		1.5	V	
Input voltage High		3.5		V_{DD}	V	
Output voltage Low			0.1	0.4	V	I_{OL} = 3.0mA
SCL clock frequency	11		100	1000	kHz	
$\overline{DAV}$ data available						100k (nom) pull-up resistor
Output voltage low			0.2	0.4	V	I_{OH} = 2.4mA
$\overline{RESET}$ Schmitt input	1					100k (nom) pull-up resistor
Input voltage Low		0		0.8	V	
Input voltage High		V_{DD}-1.0		V_{DD}	V	
Input current Low		-22	-50	-220	µA	V_{IN} = V_{SS}
Input current High		-10		+10	µA	V_{IN} = V_{DD}

NOTE
Input voltage low and input voltage high for $\overline{EXT/INT}$, AS and $\overline{XTI}$ are as specified for DATA I/O.

PIN DESCRIPTION Symbol	Pin	Pin Name and Description
$\overline{RESET}$	1	**Active Low Reset.** Includes a 100kΩ pull - up resistor
$\overline{EXT/INT}$	2	**Control Pin for SYNC I/O and DATA I/O.** Includes a 100kΩ pull - down resistor. When low or not connected, internal SYNC and DATA are used, pins 9 and 10 are outputs. When high, supply SYNC and DATA from an external source, pins 9 and 10 are inputs.
BLC	3	**Black level capacitor.**
WLC	4	**White level capacitor.**
VIDEO	5	**Input for composite video signal with negative going syncs**
GND	6	**Ground 0 volts.**
TCR	7	**Time constant resistor.** Controlling discharge rate of black and white level capacitor voltages.
AS	8	**Address select for I²C bus.** [0010 0001] with AS set high, or [0010 0011] with AS set low. Includes 100kΩ pull - down resistor.
DATA I/O	9	**Data input/output.**
SYNC I/O	10	**Sync input/output.**
SCL	11	**I²C bus serial clock.**
VDD	12	**Positive supply voltage +5V ± 10%**
SDA	13	**I²C bus bi-directional data port.**
$\overline{DAV}$	14	**Active low open drain output data available signal to microprocessor.** Includes 100kΩ pull - up resistor
XTO	15	**Crystal out,** 27.75MHz fundamental crystal with on-chip 1MΩ resistor to $\overline{XTI}$.
$\overline{XTI}$	16	**Crystal input.**

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency 27.750000MHz. AT cut.
Tolerance at -10°C to 60°C ± 50ppm.
Tolerance overall ± 100ppm.
Nominal load capacitance 20pF.
Equivalent series resistance <20Ω.

FUNCTIONAL DESCRIPTION

The video signal is sliced to produce data and synchronising signals. Timing circuits monitor the sync signal to enable the MV1820 to lock onto the broadcast signal. A timing window, for the Vertical Blanking Interval (VBI) lines 6 - 22 and 318 - 335, is established to enable the acquisition circuit to monitor the sliced data signal for valid teletext data.

The framing code is checked for valid World System Teletext (WST) data. Magazine, packet and designation code bytes are checked and valid Broadcast Service Data Packets (BSDP) format two type only are accepted. These are known as packet 8/30. Format two is signalled by byte six, data bit two being set high and bits 3 and 4 set low. Bytes 13 to 25 inclusive are Hamming decoded (8,4) and stored in seven registers each of eight bits. If the complete message is correctly received with no uncorrectable Hamming errors, an interrupt to the microprocessor is signalled by the DAV (bar) pin going low. At the same time the data is transferred to a second bank of registers, reorganised with original numbered bytes 14, 15, 24, 25 and 13 placed after byte 23, to be read out on the I²C bus when so requested. Subsequent valid messages will continue to be transferred to the output registers overwriting any existing data. In this way the output registers always contain the latest PDC message.

The MV1820 is configured as an I²C bus slave transmitter with a selectable address. The I²C bus address is 0010 0001 (20 + 1 hex) with the address select (AS) pin set high, or 0010 0011 (22 + 1 hex) with the AS pin set low. The read bit (LSB) must always be set, it is not possible to write to the MV1820.

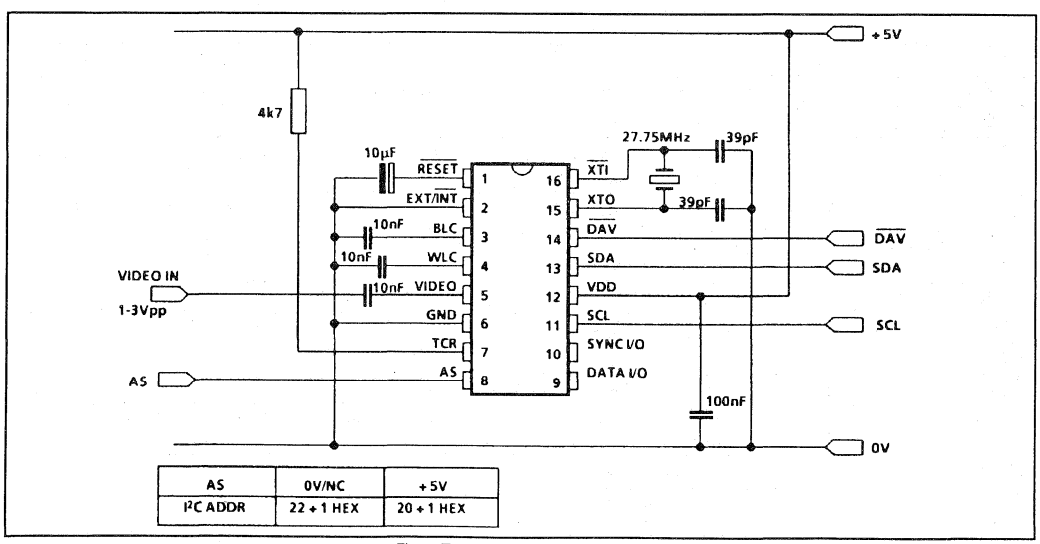
On recognising its address, the MV1820 will send an acknowledge and then transmit on the SDA line the first byte from the output registers (decoded byte 16 and 17) most significant bit (MSB) first. It will then monitor the SDA line for an acknowledge from the microprocessor. If the microprocessor does NOT send an acknowledge, the MV1820 will release the data line to allow the microprocessor to send a stop condition. If the microprocessor does send an acknowledge, the following bytes of the message will be output provided each byte is acknowledged. The final data will be byte 13 followed by the four '1's.

When readout is complete, the DAV (bar) pin is reset high and the output registers are all set high. If the microprocessor continues to send clocks on the SCL line, the MV1820 will output FF bytes on the SDA line. Also, if the MV1820 is re-addressed before another PDC message is received, the MV1820 will output FF bytes on the SDA line. The microprocessor can prematurely stop the message by NOT sending an Acknowledge followed by a STOP condition after any byte has been sent by the MV1820. The registers will then be reset to FF bytes and the $\overline{\text{DAV}}$ pin will be reset high.

To prevent any corruption of the data in the output registers during I²C bus activity, valid PDC messages are held in the incoming registers until I²C bus activity ceases. Here they may be overwritten by new PDC messages until the I²C bus activity ceases and they can then be transferred to the output registers.

System clock is provided by an on - chip 27.75MHz oscillator together with an external parallel resonant fundamental frequency AT cut crystal.

Following a reset, $\overline{\text{RESET}}$ pulled low, the output I²C bus registers will contain FF bytes and the $\overline{\text{DAV}}$ pin will be set high. When the power supply is removed, the I²C bus will not be clamped to ground, leaving it free for other I²C bus traffic.



AS	0V/NC	+5V
I²C ADDR	22 + 1 HEX	20 + 1 HEX

Fig.3 Typical application diagram

ORDER OF DATA OUTPUT ON THE I²C BUS

Bit Order		EBU Numbering		Bit Value		VPS Equivalence
byte 1	bit 7	byte 16	bit 0 - CNI b9		reserved	[byte 11
	bit 6		bit 1 - CNI b10	64	network (or programme provider)	I
	bit 5		bit 2 - PIL b1	16		I
	bit 4		bit 3 - PIL b2	8		I
	bit 3	byte 17	bit 0 - PIL b3	4	day	I
	bit 2		bit 1 - PIL b4	2		I
	bit 1		bit 2 - PIL b5	1		I
	bit 0		bit 3 - PIL b6	8		[
byte 2	bit 7	byte 18	bit 0 - PIL b7	4		[byte 12
	bit 6		bit 1 - PIL b8	2	month	I
	bit 5		bit 2 - PIL b9	1		I
	bit 4		bit 3 - PIL b10	16		I
	bit 3	byte 19	bit 0 - PIL b11	8		I
	bit 2		bit 1 - PIL b12	4	hour	I
	bit 1		bit 2 - PIL b13	2		I
	bit 0		bit 3 - PIL b14	1		[
byte 3	bit 7	byte 20	bit 0 - PIL b15	32		[byte 13
	bit 6		bit 1 - PIL b16	16		I
	bit 5		bit 2 - PIL b17	8		I
	bit 4		bit 3 - PIL b18	4	minute	I
	bit 3	byte 21	bit 0 - PIL b19	2		I
	bit 2		bit 1 - PIL b20	1		I
	bit 1		bit 2 - CNI b5	8		I
	bit 0		bit 3 - CNI b6	4		[
byte 4	bit 7	byte 22	bit 0 - CNI b7	2	country	[byte 14
	bit 6		bit 1 - CNI b8	1		I
	bit 5		bit 2 - CNI b11	32		I
	bit 4		bit 3 - CNI b12	16		I
	bit 3	byte 23	bit 0 - CNI b13	8	network (or programme provider)	I
	bit 2		bit 1 - CNI b14	4		I
	bit 1		bit 2 - CNI b15	2		I
	bit 0		bit 3 - CNI b16	1		[
byte 5	bit 7	byte 14	bit 0 - PCS b1	2	status (define the analog sound	[byte 5
	bit 6		bit 1 - PCS b2	1	transmission system)	I
	bit 5		bit 2 - unallocated			I
	bit 4		bit 3 - unallocated			I
	bit 3	byte 15	bit 0 - CNI b1	128		I
	bit 2		bit 1 - CNI b2	64		I
	bit 1		bit 2 - CNI b3	32	country	I
	bit 0		bit 3 - CNI b4	16		[
byte 6	bit 7	byte 24	bit 0 - PTY b1	128		[byte 15
	bit 6		bit 1 - PTY b2	64		I
	bit 5		bit 2 - PTY b3	32		I
	bit 4		bit 3 - PTY b4	16	programme type	I
	bit 3	byte 25	bit 0 - PTY b5	8		I
	bit 2		bit 1 - PTY b6	4		I
	bit 1		bit 2 - PTY b7	2		I
	bit 0		bit 3 - PTY b8	1		[
byte 7	bit 7	byte 13	bit 0 - LCI b1	2	Label Channel Identifier	
	bit 6		bit 1 - LCI b2	1	Interleave up to four PIL messages	
	bit 5		bit 2 - LUF	1	Label Update Flag (LUF)	
	bit 4		bit 3 - unallocated			
	bit 3		-set to 1			
	bit 2		-set to 1		NOTE: Data is output on the	
	bit 1		-set to 1		I²C bus MSB first	
	bit 0		-set to 1			

MV1821

VIDEO CASSETTE RECORDER PDC AND VPS INTERFACE CIRCUIT

(Supersedes version in October 1995 Media IC Handbook, HB3120–3.0)

The MV1821 is a member of the Enhanced Video Automation (EVA) family for receiving Programme Delivery Control (PDC) messages broadcast in World System Teletext (WST) format two Broadcast Service Data Packets (BSDP). It will also receive Video Programme System (VPS) data from TV line 16 in Manchester bi–phase format. The data from either service can be read via the I²C bus connections in a standard format (see page 7). Additional data is appended to include new PDC features and differentiate between data sources.

It is intended for use in Video Cassette Recorders to provide automatic recording of suitably labelled Television programmes requested by the user.

FEATURES

- Fully automatic PDC/VPS switching
- Full error checking of both data formats
- Low external component count
- I²C Bus for low cost Interfacing
- I²C Bus and $\overline{DAV}$ released during power down
- Low frequency 6·9375MHz oscillator
- Full decoding of Hamming data (PDC)
- Supports 'fast mode' I²C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	–0·3V to +7·0V
All inputs	–0·3 to V_{DD}+0·3V
Operating temperature	–10°C to +75°C
Storage temperature	–65°C to +150°C

ORDERING INFORMATION

MV1821C/KG/DPAS
MV1821C/KG/MPES
MV1821C/KG/MPEE (Tape and reel)

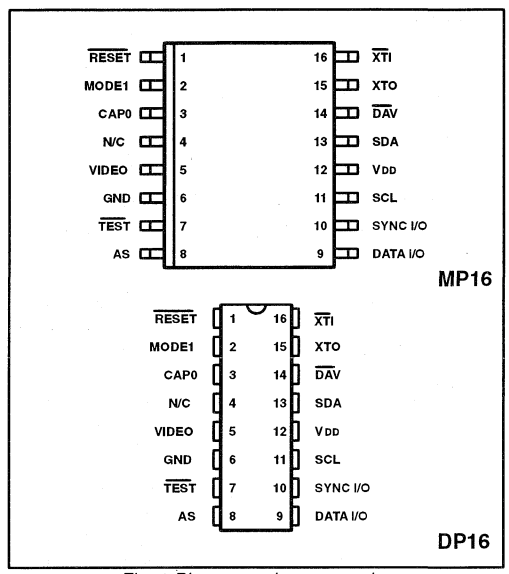


Fig. 1 Pin connections – top view

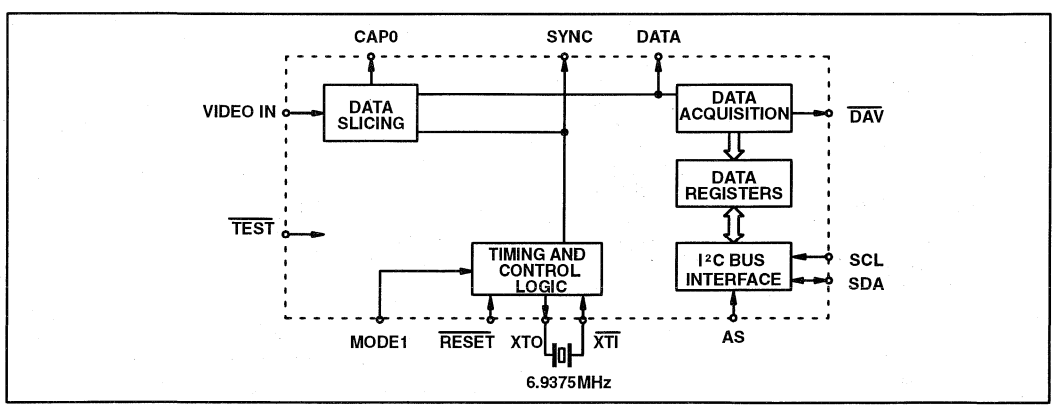


Fig. 2 MV1821 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = –10 to +75°C, V_{DD} = 5V ±10%

Characteristics	Pin	Min	Typ	Max	Units	Conditions
Supply voltage	12	4·5	5·0	5·5	V	
Supply Current	12		20		mA	
Video input	5					
Voltage amplitude		1·0	1·8	2·5	Vpp	Bottom of sync to white (pk to pk)
Source impedance				250	Ω	220nF input capacitor
CAP0	3					
Capacitor value			220		nF	Connected to GND
Capacitor tolerance		–10%		+10%		
Effective series resistance				5	Ω	1MHz
DATA & SYNC OUTPUTS	9 & 10					
Output voltage High		$0·8V_{DD}$	$0·95V_{DD}$		V	I_{OH} = –2·0mA
Output voltage Low			0·1	0·4	V	I_{OL} = 2·0mA
MODE1 & AS	2 & 8					75k (nom) pull–down resistor
Input voltage Low		0		$0·2V_{DD}$	V	
Input voltage High		$0·8V_{DD}$		V_{DD}	V	
Input current Low		–10		+10	µA	$V_{IN} = V_{SS}$
Input current High		18	67	275	µA	$V_{IN} = V_{DD}$
$\overline{\textbf{XTI}}$ input	16					1M (nom) resistor to XTO
Input voltage Low		0		$0·2V_{DD}$	V	
Input voltage High		$0·8V_{DD}$		V_{DD}	V	
Input current Low		–0·5	–5·0	–20	µA	$-0·3 < V_{IN} < V_{IL}$ max
Input current High		0·5	1.5	20	µA	V_{IH} min $< V_{IN} < (V_{DD} + 0·3)$
XTO output	15					
Output voltage High		$0·8V_{DD}$	$0·9V_{DD}$		V	I_{OH} = –0·1mA
Output voltage Low			0·1	0·4	V	I_{OL} = 0·1mA
Frequency			6·9375		MHz	±100ppm
I^2C bus						
SCL, SDA Schmitt inputs	11, 13					
Input voltage Low		0		1·5	V	
Input voltage High		3·0		V_{DD}	V	
Output voltage Low (SDA only)			0·1	0·6	V	I_{OL} = 6·0mA
SCL Clock Frequency	11		400	775	kHz	
Hysteresis voltage		0·2	0·4		V	
$\overline{\textbf{DAV}}$ Data available	14					
Output voltage Low			0·1	0·4	V	I_{OL} = 2·0mA

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = −10 to +75°C, V_{DD} = 5V ±10%

Characteristics	Pin	Min	Typ	Max	Units	Conditions
RESET Schmitt input	1					75k (nom) pull–up resistor
Threshold voltage falling		1·4	2·0		V	
Threshold voltage rising			3·0	3·8	V	
Hysteresis Voltage		0·6	1·0		V	
Input current Low		−18	−67	−275	µA	$V_{IN} = V_{SS}$
Input current High		−10		+10	µA	$V_{IN} = V_{DD}$

Table 1

Pins	Test	Test Levels	Notes
SDA & SCL	Human body model	1kV on 100pF through 1k5Ω	< 15% LTPD
SDA & SCL	Machine model	100V on 200pF through 0Ω & <500nH	
All others	Human body model	4kV on 100pF through 1k5Ω	Meets Mil. Std. 883D class 3 requirements
All others	Machine model	400V on 200pF through 0Ω & <500nH	

LTPD=Lot Tolerant Percent Defective

Table 2 ESD data

PIN DESCRIPTION

Symbol	Pin No	Pin Name and Description
$\overline{\text{RESET}}$	1	Active low reset. Includes a 75kΩ pull–up resistor
MODE1	2	When low or not connected, both PDC and VPS data are received automatically. When high during reset positive going edge VPS ONLY mode is forced. The pin must be returned low after reset for proper operation. Includes a 75kΩ pull–down resistor. (See †)
CAP0	3	Capacitor zero. Storage for reference voltage.
N/C	4	No connection.
VIDEO	5	Input for composite video signal with negative going syncs.
GND	6	Ground 0 volts.
$\overline{\text{TEST}}$	7	Test pin, for factory use only, leave open circuit or connected to V_{DD}.
AS	8	Address select for I^2C bus, 0010 0001 if set high, or 0010 0011 if set low.
DATA	9	Data output
SYNC	10	Sync output
SCL	11	I^2C bus serial clock input
V_{DD}	12	Positive supply voltage +5V
SDA	13	I^2C bus bi–directional data port
$\overline{\text{DAV}}$	14	Active low open drain output data available signal to microprocessor
XTO	15	Crystal out, 6·9375MHz fundamental crystal with on–chip 1MΩ resistor to $\overline{\text{XTI}}$
$\overline{\text{XTI}}$	16	Crystal input

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency 6·9375000MHz. AT cut.

Tolerance at –10°C to 60°C	±50ppm
Tolerance overall	±100ppm
Nominal load capacitance	30pF
Equivalent series resistance	<20Ω

FUNCTIONAL DESCRIPTION

The video signal is sliced to produce data and synchronising signals. Timing circuits monitor the sync signal to enable the MV1821 to lock to the broadcast signal. A timing window, for the Vertical Blanking Interval (VBI) lines 6–22 and 318–335, is established to enable the acquisition circuit to monitor the sliced data signal for valid teletext or VPS line 16 data.

PDC reception

The framing code is checked for valid World System Teletext (WST) data. Magazine, packet and designation code bytes are checked and valid Broadcast Service Data Packets (BSDP) format two type only are accepted. These are also known as packet 8/30. Format two is signalled by byte six, data bit two being set high and bits 3 and 4 set low. Bytes 13 to 25 inclusive are Hamming decoded (8, 4) and stored in seven registers each of eight bits. If the complete message is received with no uncorrectable Hamming errors, an interrupt to the microprocessor is signalled by setting the $\overline{DAV}$ pin low. At the same time the data is transferred to a second bank of registers, provided there is no I²C bus activity at the time, reorganised with original numbered bytes 14, 15, 24, 25 and 13 placed after byte 23, to read out on the I²C bus when so requested. See page 7.

VPS reception

The VPS data consists of 15 eight bit words encoded in Manchester bi–phase format with a data rate of 2.5Mbits/sec. It is only transmitted in TV line 16, so similar data on other TV lines is excluded. A data low to high transition indicates a binary zero and a high to low transition indicates a binary one. Word 1 acts as a clock run (10/10/10/10/10/10/10/10) to synchronise the decoder. Word 2 is a start code (10/00/10/10/10/01/10/01) to verify the required data. Note, the second element 00 contains a deliberate violation of the Manchester bi–phase format which is only permitted in word 2. Words 5, 11, 12, 13, 14 and 15 are Manchester bi–phase decoded and if verified are stored in the input registers. When all the message is correctly received, an interrupt to the microprocessor is signalled by the $\overline{DAV}$ pin going low. At the same time the data is transferred to a second bank of registers, provided there is no I²C bus activity at the time, reorganised into the word sequence11, 12, 13, 14, 5, 15, followed by 11111110, to be read out on the I²C bus when requested, see page 7.

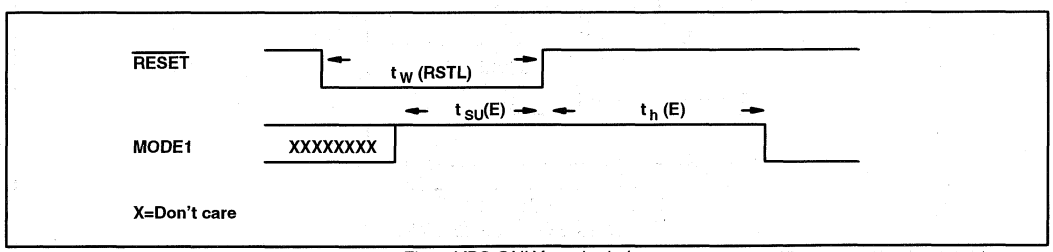


Fig. 3 VPS ONLY mode timing

PARAMETER		FROM POWER UP			FROM RESET		
		MIN	NOM	MAX	MIN	NOM	MAX
t_w(RSTL)	Pulse duration $\overline{RESET}$ low	300ms			150ns		
t_{su}(E)	MODE1 set–up time before $\overline{RESET}$ high	150ns			150ns		
t_h(E)	MODE1 hold time after $\overline{RESET}$ high	150ns			150ns		

† VPS ONLY mode

In an area where VPS is the only form of Programme Delivery Control then because of the algorithm employed by MV1821 when searching for the presence of either packet 8/30 format 2 or VPS in the broadcast signal, a delay of approximately 2·5 seconds would occur at power–up, reset and whenever a channel change occurred. This mode alleviates this problem in VPS only areas.

To force the MV1821 into VPS ONLY mode the following events must occur:

At power–up/reset the $\overline{RESET}$ pin must be low and the MODE1 pin must be high, the reset pin is then taken high after which the MODE1 pin is taken low. (see Fig. 3).

The ideal way of generating the timing shown in Fig.3 is under microcontroller or microprocessor control using output pins or some from of decoder e.g. 74HCT138.

In order to return to AUTO PDC/VPS mode it is only necessary to perform a reset with MODE1 held low.

I²C bus interface

The MV1821 is configured as an I²C bus slave transmitter with a selectable address. The I²C bus address is 0010 0001 (20+1 hex) with the address select (AS) pin set high, or 0010 0011(22+1 hex) with the AS pin set low. The read bit (LSB) must be set, it is not possible to write to the MV1821.

On recognising its address, the MV1821 will send an acknowledge, and then transmit on the SDA line the first byte from the output registers most significant bit (MSB) first. It will then monitor the SDA line for an acknowledge from the microprocessor. If the microprocessor does NOT send an acknowledge, the MV1821 will release the data line to allow the microprocessor to send a stop condition and the output registers are all set high. If the microprocessor does send an acknowledge, the following bytes of the message will be output provided each byte is acknowledged. The final data will be either, PDC byte 13 followed by1111, or 1111110 for VPS messages, see page 7. The last bit of the message serves to indicate the source of data: 1=PDC, 0=VPS.

When readout is complete, the $\overline{DAV}$ pin is reset high and the output registers are all set high. If the microprocessor continues to send clocks on the SCL line, the MV1821 will output FF bytes on the SDA line. Also, if the MV1821 is re–addressed before another PDC message is received, the MV1821 will output FF bytes on the SDA line. The microprocessor can prematurely stop the message by NOT sending an acknowledge followed optionally by a STOP condition after any byte has been sent by the MV1821. The registers will then be reset to FF and the $\overline{DAV}$ pin will be reset high. Also, if after a partial readout, the microprocessor sends a repeat START condition followed by the MV1821 I^2C bus address, the registers will be reset to FF, $\overline{DAV}$ pin will be reset high and the MV1821 will output FF bytes on the SDA line.

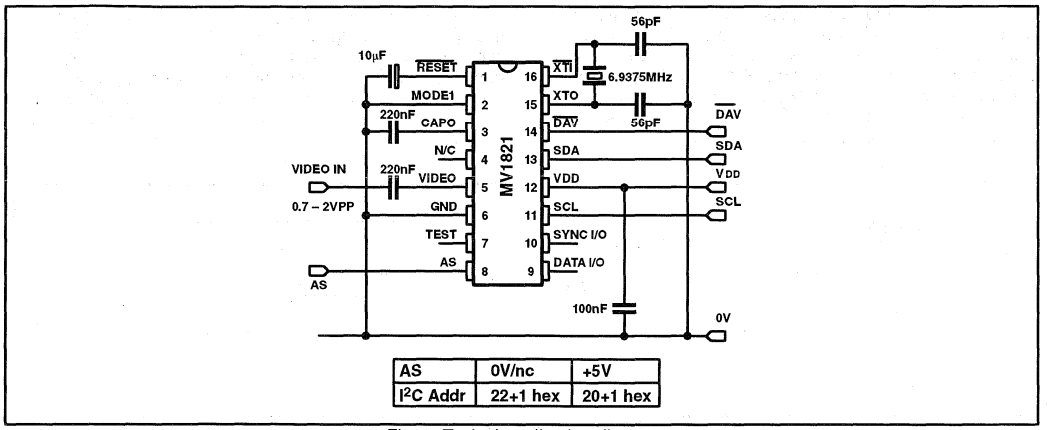
To prevent any corruption of the data in the output registers during I^2C bus activity, valid PDC or VPS messages are held in the incoming registers until I^2C bus activity ceases. Here they may be over written by new PDC or VPS messages until the I^2C bus activity ceases and they can be transferred to the output registers. In the absence of I^2C bus reads, subsequent valid messages will continue to be transferred to the output registers over–writing any existing data. In this way the output registers always contain the latest PDC or VPS message.

General information

PDC data transmitted via Teletext packets 8–30 Format 2, will take precedence over VPS data. A 64 state frame counter is reset by every valid PDC packet, which will inhibit VPS reception until the counter reaches maximum. This will ensure that if receiving both signals on a given transmission, the PDC data will dominate, but if it does at any time cease to be received, the VPS data will be enabled within 2.56 seconds of the last PDC packet. This allows for one pkt. 8–30 to be missed without changing to VPS operation. See Fig. 6.

The system clock is provided by an on chip 6·9375MHz oscillator together with an external parallel resonant fundamental frequency AT cut crystal.

Following a reset ($\overline{RESET}$ pulled low), the output I^2C bus registers will contain FF bytes and the $\overline{DAV}$ pin will be set high. When the MV1821 is powered down, the I^2C bus will be released so that it can be used by other devices.



AS	0V/nc	+5V
I^2C Addr	22+1 hex	20+1 hex

Fig. 4. Typical application diagram

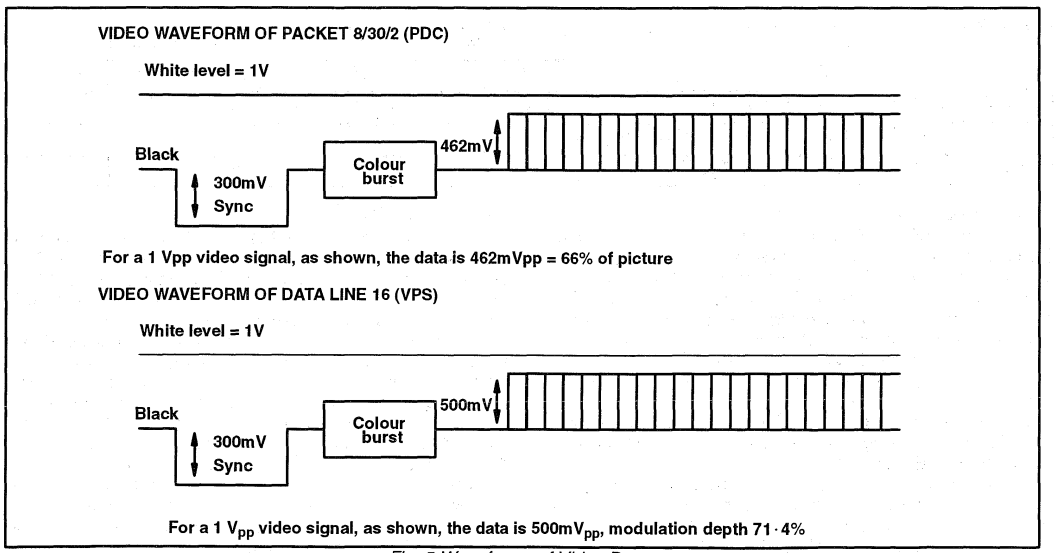


Fig. 5 Waveforms of Video Data

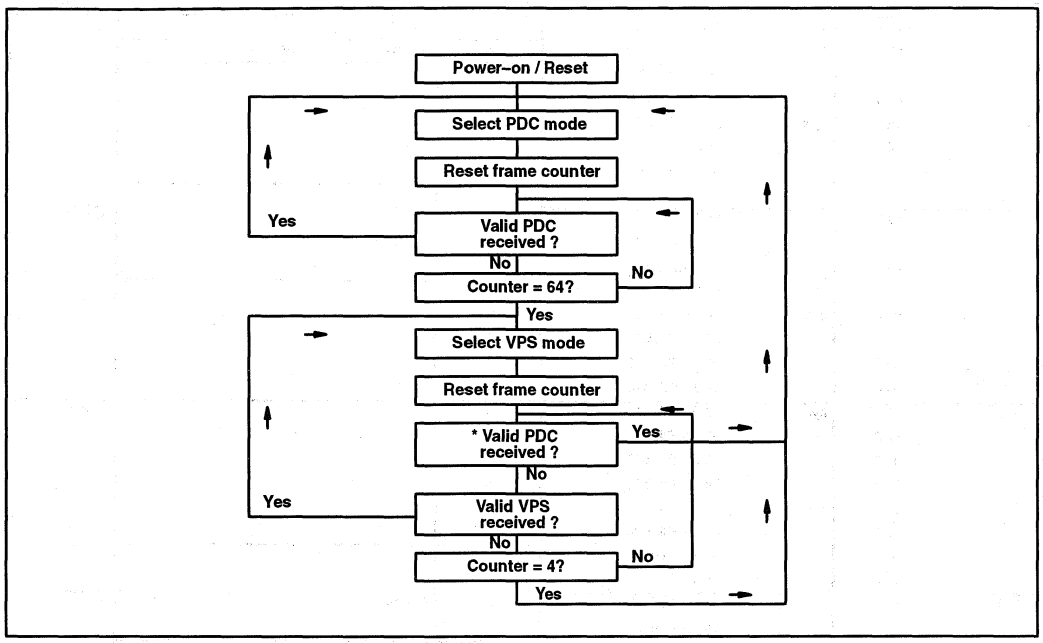


Fig. 6 Flow chart of VPS/PDC Switching

* The operation of the MV1821, in the presence of both Line 16 (VPS) and packet 8/30/2, follows the guidelines of the EBU Code of practice, SPB459 Revision2, February 1992, page 49:

"–When both Line 16 (VPS) and teletext delivered labels are available simultaneously, decoders should default to the teletext delivered service."

The counter is incremented once / frame

One line = 64μs One frame = 625 lines

PDC timeout count =	64 frames =	625 x 64μs x 64 =	2·56s
VPS timeout count =	4 frames =	625 x 64μs x 4 =	160ms

ORDERING INFORMATION

MV1821/KG/DPAS
MV1821/KG/MPES
MV1821/KG/MPEE (Tape and Reel)

ORDER OF DATA OUTPUT ON THE I²C BUS

BIT ORDER		PDC DATA		BIT VALUE		VPS data
byte 1	bit 7	byte 16	bit 0 – CNI b9	———	reserved	byte 11
	bit 6		bit 1 – CNI b10	64	Network (or programme provider)	
	bit 5		bit 2 – PIL b1	16		
	bit 4		bit 3 – PIL b2	8		
	bit 3	byte 17	bit 0 – PIL b3	4	Day	
	bit 2		bit 1 – PIL b4	2		
	bit 1		bit 2 – PIL b5	1		
	bit 0		bit 3 – PIL b6	8		
byte 2	bit 7	byte 18	bit 0 – PIL b7	4		byte 12
	bit 6		bit 1 – PIL b8	2	Month	
	bit 5		bit 2 – PIL b9	1		
	bit 4		bit 3 – PIL b10	16		
	bit 3	byte 19	bit 0 = PIL b11	8		
	bit 2		bit 1 – PIL b12	4	Hour	
	bit 1		bit 2 – PIL b13	2		
	bit 0		bit 3 – PIL b14	1		
byte 3	bit 7	byte 20	bit 0 – PIL b15	32		byte 13
	bit 6		bit 1 – PIL b16	16		
	bit 5		bit 2 – PIL b17	8		
	bit 4		bit 3 – PIL b18	4	Minute	
	bit 3	byte 21	bit 0 – PIL b19	2		
	bit 2		bit 1 – PIL b20	1		
	bit 1		bit 2 – CNI b5	8		
	bit 0		bit 3 – CNI b6	4		
byte 4	bit 7	byte 22	bit 0 – CNI b7	2	Country	byte 14
	bit 6		bit 1 – CNI b8	1		
	bit 5		bit 2 – CNI b11	32		
	bit 4		bit 3 – CNI b12	16		
	bit 3	byte 23	bit 0 – CNI b13	8	Network (or programme provider)	
	bit 2		bit 1 – CNI b14	4		
	bit 1		bit 2 – CNI b15	2		
	bit 0		bit 3 – CNI b16	1		
byte 5	bit 7	byte 14	bit 0 – PCS b1	2	Status (define the analog sound	byte 5
	bit 6		bit 1 – PCS b2	1	transmission system)	
	bit 5		bit 2 – MI	1	Mode Indicator	
	bit 4		bit 3 – unallocated			
	bit 3	byte 15	bit 0 – CNI b1	128		
	bit 2		bit 1 – CNI b2	64		
	bit 1		bit 2 – CNI b3	32	Country	
	bit 0		bit 3 – CNI b4	16		
byte 6	bit 7	byte 24	bit 0 – PTY b1	128		byte 15
	bit 6		bit 1 – PTY b2	64		
	bit 5		bit 2 – PTY b3	32		
	bit 4		bit 3 – PTY b4	16	Programme Type	
	bit 3	byte 25	bit 0 – PTY b5	8		
	bit 2		bit 1 – PTY b6	4		
	bit 1		bit 2 – PTY b7	2		
	bit 0		bit 3 – PTY b8	1		
byte 7	bit 7	byte 13	bit 0 – LC1 b1	2	Label Channel Identifier	– set to 1
	bit 6		bit 1 – LC1 b2	1	interleave up to four PIL messages	– set to 1
	bit 5		bit 2 – LUF	1	Label Update Flag	– set to 1
	bit 4		bit 3 – PRF	1	Prepare to Record Flag	– set to 1
	bit 3		– set to 1			– set to 1
	bit 2		– set to 1	NOTE: Data is output on the I²C bus MSB first		– set to 1
	bit 1		– set to 1			– set to 1
	bit 0		– set to 1			– set to 0

MV1822

PDC, VPS AND TIME RECEIVER

(Supersedes version in October 1995 Media IC Handbook, HB3120 –3.0)

The MV1822 is a member of the Enhanced Video Automation (EVA) family for receiving Programme Delivery Control (PDC) messages, packet 8/30 Format 2, broadcast in World System Teletext (WST). It will automatically switch to receiving Video Programme System (VPS) data from TV line 16 in Manchester bi–phase format in the absence of PDC data. Under control of the mode pins, it can also receive Broadcast Service Data Packet format one data to provide Unified Date and Time (UDT) or Time data from headers. The data from a service can be read via the I²C bus connections in a standard format (see pages 7, 8 and 9).

FEATURES

- On–chip analog data slicing
- Low external component count
- Low frequency 6·9375MHz oscillator
- I²C Bus and $\overline{DAV}$ released during power down
- Automatic PDC/VPS operation
- Advanced CMOS technology gives low power dissipation and high reliability
- "Fast–Mode" I²C bus

APPLICATIONS

- Accurate programme recordings via PDC and VPS
- Automatic Date/Time setting of VCR and TV
- Automatic tuning of VCR and TV via station ident

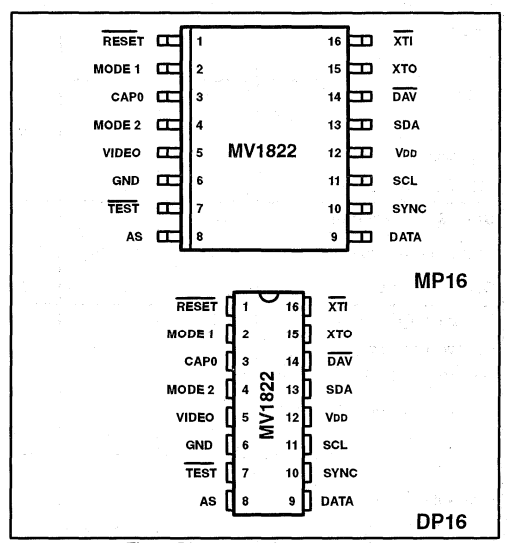


Fig. 1 Pin connections – top view

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0·3 to 7·0V
All inputs	–0·3 to V_{DD} +0·3V
Operating Temperature	–40 to +85°C
Storage Temperature	–65 to 150°C

ORDERING INFORMATION

MV1822 IG DPAS
MV1822 IG MPES
MV1822 IG MPEE (Tape and Reel)

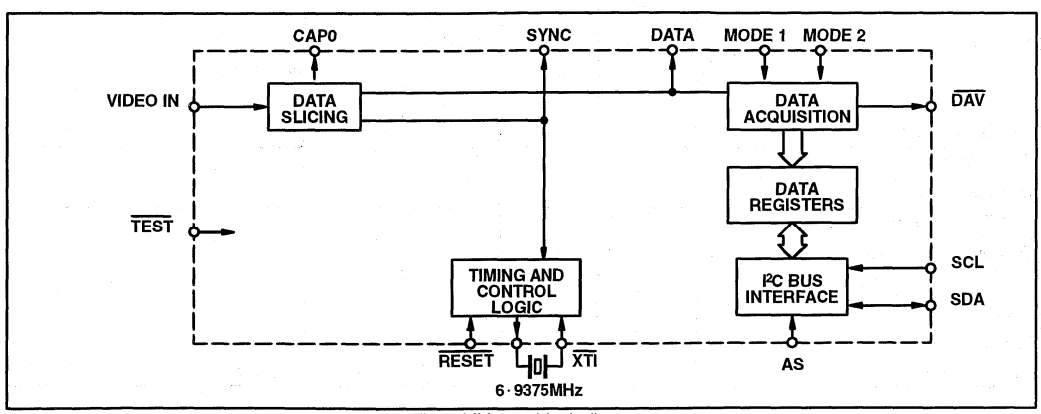


Fig. 2 MV1822 block diagram

ELECTRICAL CHARACTERISTICS

T_{amb}= –40°C to +85°C, V_{DD}=5V ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	12	4·5	5·0	5·5	V	
Supply current	12		20		mA	
VIDEO input	5					220nF ±20% input capacitor
Voltage amplitude		1·0	1·8	2·5	V_{pp}	Bottom of sync to white (pk to pk)
Source impedance				250	Ω	
CAP0	3					
Capacitor value			220		nF	Connected to GND
Capacitor tolerance		–20%		+20%		
Effective series resistance				5	Ω	1MHz
DATA & SYNC outputs	9 & 10					
Output voltage High		0·8V_{DD}	0·95V_{DD}		V	I_{OH} = –2·0mA
Output voltage Low			0·1	0·4	V	I_{OL} = 2·0mA
MODE1, MODE2 & AS	2,4 & 8					75k (nom) pull–down resistor
Input voltage Low		–0·3		0·2V_{DD}	V	
Input Voltage High		0·8V_{DD}		V_{DD}+0·3	V	
Input current Low		–10		+10	µA	V_{IN}=V_{SS}
Input current High		18	67	275	µA	V_{IN}=V_{DD}
XTI input	16					1M (nom) resistor to XTO
Input voltage Low		–0·3		0·2V_{DD}	V	
Input voltage High		0·8V_{DD}		V_{DD}+0.3	V	
Input current Low		–0·5	–5·0	–20	µA	–0·3<V_{IN}<V_{IL} max
Input current High		0·5	1·5	20	µA	V_{IH} min <V_{IN}<(V_{DD}+0·3)
XTO output	15					
Output voltage High		0·8V_{DD}	0·9V_{DD}		V	I_{OH}= –0·1mA
Output voltage Low			0·1	0·4	V	I_{OL}=0·1mA
Frequency			6·9375		MHz	±100ppm
I^2C bus						
SCL, SDA Schmitt inputs	11, 13					
Input voltage Low		–0·3		0·3V_{DD}	V	
Input voltage High		0·7V_{DD}		V_{DD}+0·3	V	
Output Voltage Low			0·1	0·6	V	I_{OL}=6·0mA
SCL Clock Frequency	11	0		400	kHz	
Hysteresis Voltage		0·2	0·4		V	
$\overline{DAV}$ Data available	14					
Output voltage Low			0·1	0·4	V	I_{OL}=2·0mA
$\overline{RESET}$ Schmitt input	1					
Threshold voltage falling		1·4	1·9		V	
Threshold voltage rising			3·1	3·8	V	
Hysteresis Voltage		0·6	1·2		V	
Input current Low		–10		+10	µA	V_{IN}=V_{SS}
Input current High		–10		+10	µA	V_{IN}=V_{DD}

Table 1

Pins	Test	Test Levels	Notes
SDA & SCL	Human body model	1kV on 100pF through 1k5Ω	< 15% LTPD
SDA & SCL	Machine model	100V on 200pF through 0Ω & <500nH	
All others	Human body model	4kV on 100pF through 1k5Ω	Meets Mil. Std. 883D class 3 requirements
All others	Machine model	400V on 200pF through 0Ω & <500nH	

LTPD=Lot Tolerant Percent Defective

Table 2 ESD data

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency	6·937500MHz AT cut.
Tolerance over operating temperature range	±50ppm
Tolerance overall	±100ppm
Nominal load capacitance	30pF.
Equivalent series resistance	<20Ω

PIN DESCRIPTION

Symbol	Pin No	Pin Name and Description
$\overline{\text{RESET}}$	1	Active low reset.
MODE 1	2	Control input see truth table below for function. Includes a 75kΩ pull–down resistor
CAP0	3	Capacitor zero, storage for reference voltage
MODE 2	4	Control input see truth table below for function. Includes a 75kΩ pull–down resistor
VIDEO	5	Input for composite video signal with negative going syncs
GND	6	Ground, 0V
$\overline{\text{TEST}}$	7	Test pin, for factory use only, leave open circuit or connected to V_{DD}
AS	8	Address select for I²C bus, 0010 0001 if set high, or 0010 0011 if set low
DATA	9	Data output
SYNC	10	Sync output
SCL	11	I²C bus serial clock input
V_{DD}	12	Positive supply voltage, +5V
SDA	13	I²C bus bi–directional data port
$\overline{\text{DAV}}$	14	Active low open drain output data available signal to microprocessor
XTO	15	Crystal out, 6·9375MHz fundamental crystal with on–chip 1MΩ resistor to XTI
$\overline{\text{XTI}}$	16	Crystal input

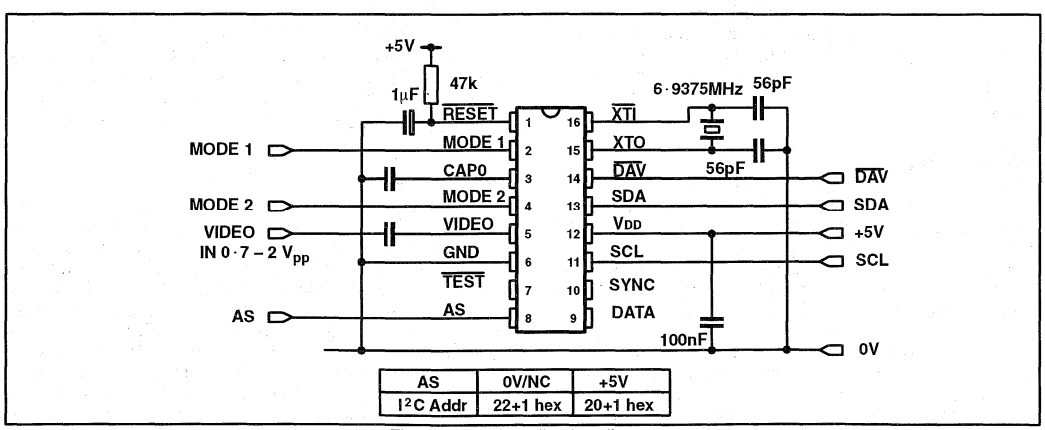


Fig. 3. Typical application diagram

TRUTH TABLE FOR MODE 1 & 2 PINS.

MODE 2 (pin 4)	MODE 1 (pin 2)	FUNCTION
0	0	PDC or VPS
0	1	VPS only
1	0	UDT
1	1	HEADER TIME

Pins MODE 1 and MODE 2 are latched in on the leading edge of sync. When either pin changes state, the contents of the read registers are reset to all 1's and $\overline{DAV}$ is reset off.

FUNCTIONAL DESCRIPTION

The video signal is sliced to produce data and synchronising signals. Timing circuits monitor the sync signal to enable the MV1822 to lock on to the broadcast signal. A timing window, for the Vertical Blanking Interval (VBI) lines 6–22 and 318–335, is established to enable the acquisition circuit to monitor the sliced data signal for valid teletext or VPS line 16 data. In normal use both MODE 1 and MODE 2 pins are set low to receive PDC or VPS data. When UDT data is required, the MODE 1 pin must be low and the MODE 2 pin must be high. When VPS only data is required, the MODE 1 pin must be high and the MODE 2 pin low. When TIME data from the header is required, both MODE 1 and MODE 2 pins are set high. An internal pull–down resistor is provided on each mode pin so that for normal mode of operation, the pins may be left open circuit.

Byte number convention

There are 45 bytes in a teletext data packet, numbered 1 to 45. Bytes 1 and 2 are the clock run in, byte 3 is the framing code, bytes 4 and 5 are the magazine and row address group. In packet 8/30 byte 6 is used to indicate the designation code.

PDC reception

The framing code is checked for valid World System Teletext (WST) data. Magazine, packet and designation code bytes are checked and only valid Broadcast Service Data Packets (BSDP) are accepted. These are also known as packet 8/30. Format two packets, containing the PDC message, are signalled by byte six, data bit two being set high and bits 3 and 4 set low. Bytes 13 to 25 inclusive are Hamming decoded (8, 4) and stored in seven registers each of eight bits. If the complete message is correctly received with no uncorrectable Hamming errors, an interrupt to the microprocessor is signalled by the $\overline{DAV}$ pin going low. At the same time the data is transferred to a second bank of registers, provided there is no I^2C bus activity at the time, reorganised with original numbered bytes 14, 15, 24, 25 and 13 placed after byte 23, to read out on the I^2C bus when so requested, see page 7.

VPS reception

The VPS data consists of 15 eight bit words encoded in Manchester bi–phase format with a data rate of 2·5Mbits/sec. It is transmitted in only TV line 16 so similar data on other TV lines is excluded. A data low to high transition indicates a binary zero and a high to low transition indicates a binary one. Word 1 acts as a clock run in code (10/10/10/10/10/10/10/10) to synchronise the decoder. Word 2 is a start code (10/00/10/10/10/01/10/01) to verify the required data. Note, the second element 00 contains a deliberate violation of the Manchester bi–phase format which is only permitted in word 2. Words 5, 11, 12, 13, 14 and 15 are Manchester bi–phase decoded and if verified are stored in the input registers. When all the message is correctly received, an interrupt to the microprocessor is signalled by the $\overline{DAV}$ pin going low. At the same time the data is transferred to a second bank of registers, provided there is no I^2C bus activity at the time, reorganised into the sequence – Words 11, 12, 13, 14, 5, 15, followed by 11111110, to be read out on the I^2C bus when requested, see page 7.

PDC/VPS arbitration

In normal mode with both MODE 1 and MODE 2 pins low, PDC data transmitted via Teletext packets 8/30 Format 2, will take precedence over VPS data. A 64 state frame counter is reset by every valid PDC packet, which will inhibit VPS reception until the counter reaches maximum. This will ensure that if receiving both signals on a given transmission, the PDC data will dominate, but if it does at any time cease to be received, the VPS data will be enabled within 2·56 seconds of the last PDC packet. This allows for one packet 8/30 format 2 to be missed without changing to VPS operation.

VPS only mode

In this mode there will be no 2·56 second delay before acquiring VPS signals.

UDT reception

When UDT is enabled, PDC and VPS reception is disabled. When packet 8/30 format one is received, the UDT data in 8 bit format, starting with byte 13, is read into the internal registers provided the I^2C bus is not busy. The received UDT data from byte 16 to byte 21 inclusive has had a one added to each data nibble, to ensure transitions exist when the time data contains many zeros. The MV1822 therefore subtracts a one from each nibble in bytes 16 to 21, so that the output will supply actual UDT data. See pages 5 and 8 for details. The data is not Hamming encoded, so when the complete packet to byte 25 has been received, an interrupt to the microcontroller is generated by the $\overline{DAV}$ pin going low.

When $\overline{DAV}$ is low, I^2C bus readout inhibits reception of further UDT data. If readout is attempted before $\overline{DAV}$ goes low, FF bytes will be output and data reception will not be affected.

If readout occurs after the reception of further UDT data has begun then FF bytes will be output and data reception will not be affected. However, if $\overline{DAV}$ is already low when another packet 8/30 format one is received, then $\overline{DAV}$ will be released at byte 13, until all data has been received at byte 25, when a new interrupt to the microcontroller will be generated by the $\overline{DAV}$ pin going low again. This process will repeat until the data is read via I^2C.

Header TIME

If UDT data is not being broadcast, the time data may be obtained from the last eight bytes of the header packets. If the transmission is in serial mode, C11=1, the last eight bytes of **every** header will be received. Any byte failing parity check will not be written to the registers and the previous value in that location will be retained. As each byte is accepted, numerical data having values 30 to 39 hex (0 to 9 ASCII) will be 30 hex (0 ASCII) subtracted before being written to the registers. All other data will be written as F hex. If the transmission is in parallel mode, C11=0, the last eight bytes of only **magazine 100** headers will be received and processed. When all eight bytes have been received with no errors, an interrupt to the microcontroller is generated by the $\overline{DAV}$ pin going low. At the

same time the data is transferred to a second bank of registers, provided there is no I2C bus activity at the time. Details of the data output format on the I2C bus are given on page 9.

I²C bus interface

The MV1822 is configured as an I²C bus slave transmitter with a selectable address. The I²C bus address is 0010 0001 (20+1hex) with the address select (AS) pin set high, or 0010 0011 (22+1hex) with the AS pin set low. The read bit (LSB) must always be set, it is not possible to write to the MV1822.

On recognising its address, the MV1822 will send an acknowledge and then transmit on the SDA line the first byte from the output registers, most significant bit (MSB) first. It will then monitor the SDA line "for an acknowledge" from the microprocessor. If the microprocessor does NOT send an acknowledge, the MV1822 will release the data line to allow the microprocessor to send a stop condition. If the microprocessor does send an acknowledge, the following bytes of the message will be output provided each byte is acknowledged.

In normal mode there will be seven bytes of data available, the final data byte will be either, PDC byte 13 followed by 1111 or 11111110 for VPS messages, see page 7. The last nibble of the message serves to indicate the source of data: 1111=PDC, 1110=VPS

In UDT mode there will be 13 bytes of data available when $\overline{DAV}$ has gone low, the last byte contains the second half of the 2nd Short Programme Label, see page 8.

In header TIME mode there will be four bytes of data available when $\overline{DAV}$ has gone low, see page 9.

When readout is complete, the $\overline{DAV}$ pin is released. If the microprocessor continues to send clocks on the SCL line, the MV1822 will output FF bytes on the SDA line. Also if the MV1822 is re–addressed before further data is received and $\overline{DAV}$ goes low, the MV1822 will output FF bytes on the SDA line. The microprocessor can prematurely stop the message by NOT sending an Acknowledge (followed optionally by a STOP condition) after any byte has been sent by the MV1822. The $\overline{DAV}$ pin will then be released. Also, if after a partial readout, the microprocessor sends a repeat START condition followed by the MV1822 I²C bus address, or the mode pins are changed state, $\overline{DAV}$ pin will be released and the MV1822 will output FF bytes on the SDA line.

To prevent any corruption of the data in the output registers during I²C bus activity, valid PDC or VPS messages are held in the incoming registers until I²C bus activity ceases. Here they may be over–written by new PDC or VPS messages until the I²C bus activity ceases and they can be transferred to the output registers. In the absence of I²C bus reads, subsequent valid messages will continue to be transferred to the output registers over–writing any existing data. In this way the output registers always contain the latest PDC or VPS message, see page 7.

When $\overline{DAV}$ goes low I²C bus readout inhibits reception of further UDT data. If readout is attempted before $\overline{DAV}$ goes low, FF bytes will be output and data reception will not be affected.

General information

System clock is provided by an on chip 6·9375MHz oscillator together with an external parallel resonant fundamental frequency AT cut crystal.

Following a reset ($\overline{RESET}$ pulled low), the $\overline{DAV}$ pin will be released. When the MV1822 is powered down, the I²C bus and $\overline{DAV}$ pins will be released so that the lines can be used by other devices.

Example of UDT packet 8/30 format one data

	Network Ident		LTO	Modified Julian Date (MJD)			Co–ordinated Universal Time (UTC)			SPL 1		SPL 2	
Byte number	13	14	15	16	17	18	19	20	21	22	23	24	25
Data received	5F	F6	85	F5	99	52	25	23	54	54	45	D3	54
I²C bus Data out	5F	F6	85	E4	88	41	14	12	43	54	45	D3	54

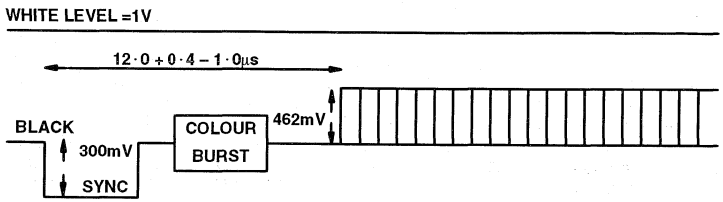
Notes: The I²C bus data in bytes 16 to 21 has had a one subtracted from each nibble to obtain actual data.
The example decodes to BBC 1, 7 August 1992, 15 hours, 12 minutes, 43 seconds British Summer Time or 14:12:43 Greenwhich Mean Time. The Local Time Offset (LTO) is + 1 hour.
SPL 1 & 2 decode as "TEST" when parity is removed.

Calendar date	Modified Julian Date	Day	Number
17:11:1858	00000	Wednesday	0
31:01:1982	45000	Sunday	4
01:01:1992	48622	Wednesday	0
01:01:1993	48988	Friday	2
13:01:1993	49000	Wednesday	0
01:01:1994	49353	Saturday	3
01:01:1995	49718	Sunday	4
10:10:1995	50000	Tuesday	6

Table 3. Modified Julian Date for various calendar dates

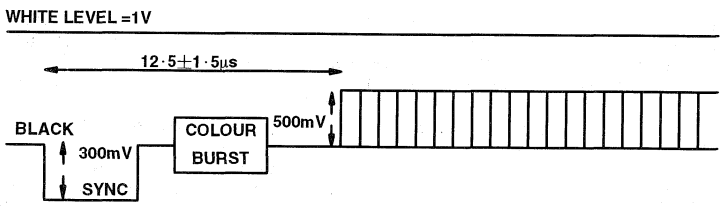
The day number is found from the equation MJD mod (7), i.e. divide by 7 and keep the integer remainder.

Video waveform of packet 8/30/2 (PDC)



For a $1V_{pp}$ signal, as shown, the data is $462mV_{pp}$ = 66% of picture. Time is measured from the negative sync edge to the peak of the seventh clock run–in pulse.

Video waveform of data line 16 (VPS)



For a $1V_{pp}$ video signal, as shown, the data is $500mV_{pp}$, modulation depth 71·4%. Time is measured from the negative sync edge to the start of data.

ORDER OF DATA OUTPUT ON THE I²C BUS

BIT ORDER		PDC DATA		BIT VALUE		VPS data
byte 1	bit 7	byte 16	bit 0 – CNI b9	———	reserved	byte 11
	bit 6		bit 1 – CNI b10	64	network (or programme provider)	
	bit 5		bit 2 – PIL b1	16		
	bit 4		bit 3 – PIL b2	8		
	bit 3	byte 17	bit 0 – PIL b3	4	day	
	bit 2		bit 1 – PIL b4	2		
	bit 1		bit 2 – PIL b5	1		
	bit 0		bit 3 – PIL b6	8		
byte 2	bit 7	byte 18	bit 0 – PIL b7	4		byte 12
	bit 6		bit 1 – PIL b8	2	month	
	bit 5		bit 2 – PIL b9	1		
	bit 4		bit 3 – PIL b10	16		
	bit 3	byte 19	bit 0 – PIL b11	8		
	bit 2		bit 1 – PIL b12	4	hour	
	bit 1		bit 2 – PIL b13	2		
	bit 0		bit 3 – PIL b14	1		
byte 3	bit 7	byte 20	bit 0 – PIL b15	32		byte 13
	bit 6		bit 1 – PIL b16	16		
	bit 5		bit 2 – PIL b17	8		
	bit 4		bit 3 – PIL b18	4	minute	
	bit 3	byte 21	bit 0 – PIL b19	2		
	bit 2		bit 1 – PIL b20	1		
	bit 1		bit 2 – CNI b5	8		
	bit 0		bit 3 – CNI b6	4		
byte 4	bit 7	byte 22	bit 0 – CNI b7	2	country	byte 14
	bit 6		bit 1 – CNI b8	1		
	bit 5		bit 2 – CNI b11	32		
	bit 4		bit 3 – CNI b12	16		
	bit 3	byte 23	bit 0 – CNI b13	8	network (or programme provider)	
	bit 2		bit 1 – CNI b14	4		
	bit 1		bit 2 – CNI b15	2		
	bit 0		bit 3 – CNI b16	1		
byte 5	bit 7	byte 14	bit 0 – PCS b1	2	status (define the analog sound	byte 5
	bit 6		bit 1 – PCS b2	1	transmission system)	
	bit 5		bit 2 – MI	1	mode indicator	
	bit 4		bit 3 – unallocated			
	bit 3	byte 15	bit 0 – CNI b1	128		
	bit 2		bit 1 – CNI b2	64		
	bit 1		bit 2 – CNI b3	32	country	
	bit 0		bit 3 – CNI b4	16		
byte 6	bit 7	byte 24	bit 0 – PTY b1	128		byte 15
	bit 6		bit 1 – PTY b2	64		
	bit 5		bit 2 – PTY b3	32		
	bit 4		bit 3 – PTY b4	16	programme type	
	bit 3	byte 25	bit 0 – PTY b5	8		
	bit 2		bit 1 – PTY b6	4		
	bit 1		bit 2 – PTY b7	2		
	bit 0		bit 3 – PTY b8	1		
byte 7	bit 7	byte 13	bit 0 – LC1 b1	2	Label Channel Identifier	– set to 1
	bit 6		bit 1 – LC1 b2	1	Interleaved up to four PIL messages	– set to 1
	bit 5		bit 2 – LUF	1	Label Update Flag (LUF)	– set to 1
	bit 4		bit 3 –PRF	1	Prepare to Record Flag	– set to 1
	bit 3		– set to 1			– set to 1
	bit 2		– set to 1			– set to 1
	bit 1		– set to 1			– set to 1
	bit 0		– set to 1			– set to 0

NOTE: Data is output on the I²C bus MSB first

Format 1. Order of UDT data output on the I²C bus

OUTPUT		INPUT				
byte 1	bit 7	byte 13	bit F–			
	bit 6		bit E–			
	bit 5		bit D–			
	bit 4		bit C–			
	bit 3		bit B–			
	bit 2		bit A–			
	bit 1		bit 9–			
	bit 0		bit 8–	**Network**		
byte 2	bit 7	byte 14	bit 7–	**Identification**		
	bit 6		bit 6–	**Code**		
	bit 5		bit 5–			
	bit 4		bit 4–			
	bit 3		bit 3–			
	bit 2		bit 2–			
	bit 1		bit 1–			
	bit 0		bit 0			
byte 3	bit 7	byte 15	bit 7–	reserved		
	bit 6		bit 6–	sign 0 = + 1 = –		
	bit 5		bit 5–	8		
	bit 4		bit 4–	4	**Time**	
	bit 3		bit 3–	2	**Offset**	
	bit 2		bit 2–	1	**Code**	
	bit 1		bit 1–	0·5		
	bit 0		bit 0–	reserved		
byte 4	bit 7	byte 16	bit 7–	reserved		
	bit 6		bit 6–			
	bit 5		bit 5			
	bit 4		bit 4			
	bit 3		bit 3–			
	bit 2		bit 2–	ten thousands		
	bit 1		bit 1–			
	bit 0		bit 0–			**M**
byte 5	bit 7	byte 17	bit 7–			
	bit 6		bit 6–	thousands		
	bit 5		bit 5–			
	bit 4		bit 4–			**J**
	bit 3		bit 3–			
	bit 2		bit 2–	hundreds		
	bit 1		bit 1–			
	bit 0		bit 0–			**D**
byte 6	bit 7	byte 18	bit 7–			
	bit 6		bit 6–	tens		
	bit 5		bit 5–			
	bit 4		bit 4–			
	bit 3		bit 3–			
	bit 2		bit 2–	units		
	bit 1		bit 1			
	bit 0		bit 0–			

NOTE: Data is output on the I²C bus MSB first

OUTPUT		INPUT				
byte 7	bit 7	byte 19	bit 7–			
	bit 6		bit 6–	hours tens		
	bit 5		bit 5–			
	bit 4		bit 4–			
	bit 3		bit 3–			
	bit 2		bit 2–	houts units		
	bit 1		bit 1–			
	bit 0		bit 0–			**U**
byte 8	bit 7	byte 20	bit 7–			
	bit 6		bit 6–	minutes tens		
	bit 5		bit 5–			
	bit 4		bit 4–			
	bit 3		bit 3–			**T**
	bit 2		bit 2–	minutes units		
	bit 1		bit 1–			
	bit 0		bit o–			
byte 9	bit 7	byte 21	bit 7–			
	bit 6		bit 6–	seconds tens		
	bit 5		bit 5–			**C**
	bit 4		bit 4–			
	bit 3		bit 3–			
	bit 2		bit 2–	seconds units		
	bit 1		bit 1–			
	bit 0		bit 0–			
byte 10	bit 7	byte 22	bit F–			
	bit 6		bit E–			
	bit 5		bit D–			
	bit 4		bit C–			
	bit 3		bit B–			
	bit 2		bit A–			
	bit 1		bit 9–			
	bit 0		bit 8–	**Short Programme**		
byte 11	bit 7	byte 23	bit 7–	**Label 1**		
	bit 6		bit 6–			
	bit 5		bit 5–			
	bit 4		bit 4–			
	bit 3		bit 3–			
	bit 2		bit 2–			
	bit 1		bit 1–			
	bit 0		bit 0–			
byte 12	bit 7	byte 24	bit F–			
	bit 6		bit E–			
	bit 5		bit D–			
	bit 4		bit C–			
	bit 3		bit B–			
	bit 2		bit A–			
	bit 1		bit 9–			
	bit 0		bit 8–	**Short Programme**		
byte 13	bit 7	byte 25	bit 7–	**Label 2**		
	bit 6		bit 6–			
	bit 5		bit 5–			
	bit 4		bit 4–			
	bit 3		bit 3–			
	bit 2		bit 2–			
	bit 1		bit 1–			
	bit 0		bit 0–			

Order of header TIME data output on the I²C bus

OUTPUT		INPUT		
byte 1	bit 7	byte 38	bit 3	**Most**
	bit 6		bit 2	**Significant**
	bit 5		bit 1	**Digit**
	bit 4		bit 0	
	bit 3	byte 39	bit 3	
	bit 2		bit 2	
	bit 1		bit 1	
	bit 0		bit 0	
byte 2	bit 7	byte 40	bit 3	
	bit 6		bit 2	
	bit 5		bit 1	
	bit 4		bit 0	
	bit 3	byte 41	bit 3	
	bit 2		bit 2	
	bit 1		bit 1	
	bit 0		bit 0	
byte 3	bit 7	byte 42	bit 3	
	bit 6		bit 2	
	bit 5		bit 1	
	bit 4		bit 0	
	bit 3	byte 43	bit 3	
	bit 2		bit 2	
	bit 1		bit 1	
	bit 0		bit 0	
byte 4	bit 7	byte 44	bit 3	
	bit 6		bit 2	
	bit 5		bit 1	
	bit 4		bit 0	
	bit 3	byte 45	bit 3	**Least**
	bit 2		bit 2	**Significant**
	bit 1		bit 1	**Digit**
	bit 0		bit 0	

NOTE: Data is output on the I²C bus MSB first

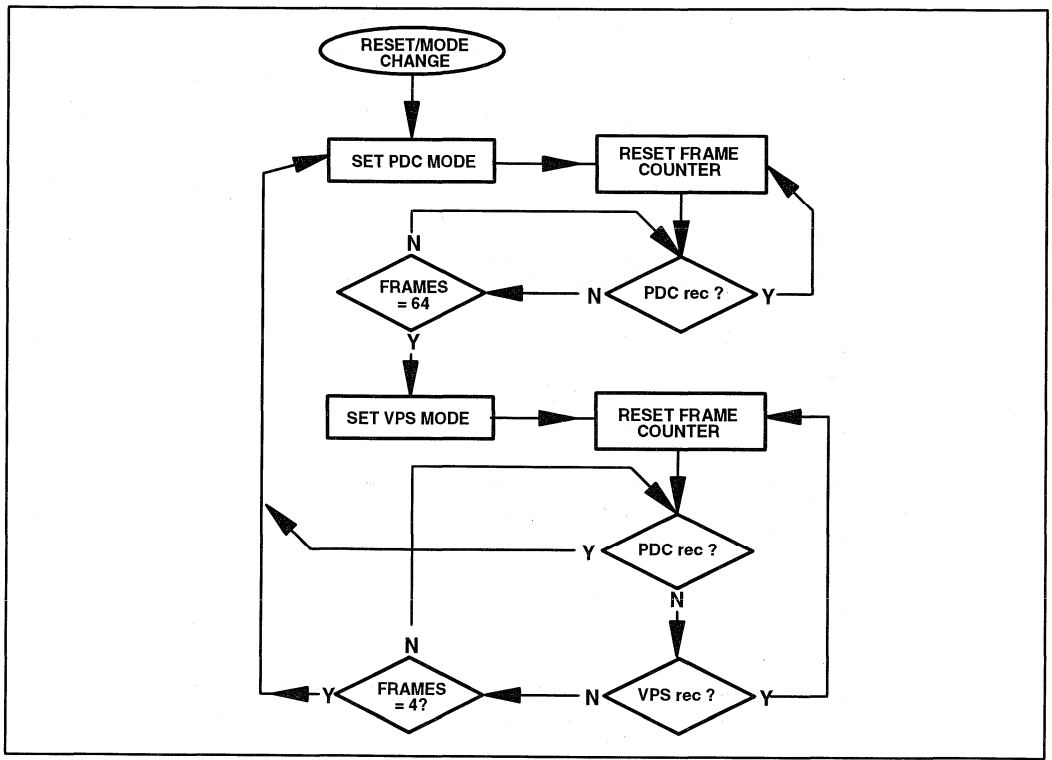


Fig. 4 Normal mode PDC/VPS switching

* The operation of the MV1822, in the presence of both Line 16 (VPS) and packet 8/30/2, follows the guide lines of the EBU Code Of Practice, SPB 459 Revision 2, February 1992, page 49:

"–when both Line 16 (VPS) and teletext delivered labels are available simultaneously, decoders should default to the teletext delivered service."

The counter is incremented once/frame.

One line =64μs One frame = 625 lines

PDC timeout count = 64 frames = 625 x 64μs x 64 = 2·65s
VPS timeout count = 4 frames = 625 x 64μs x 4 = 160ms

VPS only mode

The flow diagram above is not relevant.

Section 4
Video Compression

GEC PLESSEY
SEMICONDUCTORS

VP2611

H.261 ENCODER

(Supersedes January 1996 Edition, DS3478 - 3.0)

FEATURES

- Fully integrated H261 video encoder
- Up to full CIF resolution and 30 Hz frame rates
- Inputs YUV data in 8 x 8 sub block format
- Outputs run length coded coefficients
- On chip motion vector estimator with +/-7 pixel search window
- Addresses and control generated internally for DRAM frame store
- QFP package

ASSOCIATED PRODUCTS

- VP510 Colour Space Converter
- VP520S CIF/QCIF Converter
- VP2612 Video Multiplexer
- VP2614 Video Demultiplexer
- VP2615 H.261 Decoder

DESCRIPTION

The VP2611 Video Compression Source Coder forms part of a chip set used in video conferencing, video telephony and multimedia applications. It produces data which conforms to the H261 standard for video compression with rates between 64K and 2M bits per second. With a 27 MHz clock the device will accept data produced to full CIF resolution at 30 Hz frame rates. The pipeline latency through the device is only 3 macro block periods.

The VP2611 contains all the elements necessary for the compression algorithm. It incorporates a Motion Vector Estimator which performs a +/- 7 pixel search. The decision to use inter or intra frame compression is made by the device, and the selected data blocks are read from the frame store. New or difference data is then passed through a Discrete Cosine Transformer and quantized. Data from the quantizer is also inverse quantized and passed through an Inverse Discrete Cosine Transformer. This re-constructed data is then written to the frame store for use in the next frame period. This frame store is managed by an internal DRAM controller, and no external logic is needed.

The input data must be in YUV space, and must also conform to the six sub blocks per macro block format defined by H261. Any conversion from RGB format is performed by the VP510 Colour Space Converter. Any reduction in spatial resolution, down to CIF or QCIF requirements, is done by the VP520 Three Channel Video Filter.

The quantized data is zig-zag scanned and run length coded before being output, together with block information and motion vectors.

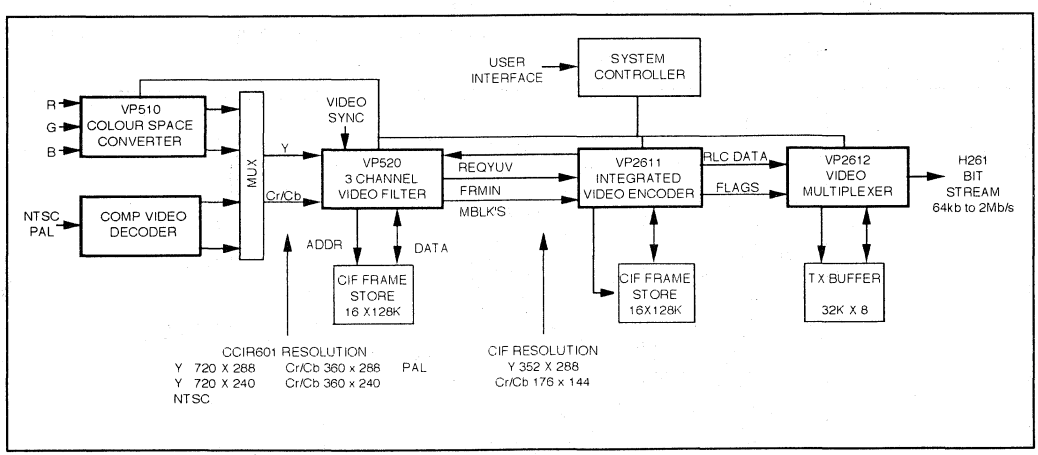


Fig 1 : Typical Video Conferencing Transmission System

PIN DESCRIPTIONS

YUV7:0	This input bus accepts YUV data one pixel at a time from the preprocessor, clocked in on the rising edge of PCLK.
PCLK	This signal is used to strobe in data at the YUV port and must be derived by dividing SYSCLK with an integer greater than one.
FRMIN	This input should be pulled high to prepare the VP2611 to code a new frame. It must be held high for at least one SYSCLK cycle and then must be pulled low again before the next frame begins. The VP2611 will respond to the rising edge of FRMIN by asserting REQYUV appproximately 184 SYSCLK cycles later.
REQYUV	This output is pulled high to request that YUV data be input for a new MacroBlock. It is pulled low again 1871 SYSCLK cycles later. It remains low during Dummy MacroBlocks and during the lay period between frames.
DBUS7:0	This output bus serves several functions as defined by DMODE3:0. In addition to providing the quantized coefficients and motion vectors, it is used to output control information.
DMODE3:0	Output flag port for DBUS7:0 bus. The value at this port identifies the data type appearing on DBUS7:0 during the same period.
DCLK	This output pulses high for a minimum of 37ns each time new data is output on DBUS or DMODE. It can be used as an edge sensitive strobe signal or a level sensitive "valid" signal.
SW15:0	This bidirectional port is connected to the frame store.
RAS	Row Address Strobe output for the external DRAMs.
CAS	Column Address Strobe output for the external DRAMs.
R/W1	Read/Write control for external DRAM 1.
R/W2	Read/Write control for external DRAM 2. N/C if 256k DRAMs.
OE1	Output Enable control for external DRAM 1 or ADR8.
OE2	Output Enable control for external DRAM 2. N/C if 256k DRAMs.
ADR7:0	Address output for the external DRAMs.
CBUS7:0	Bi-directional data bus for use by a Microprocessor. Data and insructions are clocked on and off the chip on the rising edge of CSTR.
CSTR	Data strobe for the CBUS port.
CEN	An enabling signal for the CBUS port.
CADR	When high, this signal defines CBUS as a data bus, and when low as an instruction input.
SYSCLK	System clock, run at 27MHz maximum. The clock must be high for between 35% and 65% of each clock cycle. This clock is used for all internal operations.
RESET	Active low power on reset which must be held low for at least 2064 cycles.
TCK	Test clock for JTAG.
TMS	Test Mode Select for JTAG.
TDI	Input JTAG test data.
TDO	Output JTAG test data.
TRST	Reset JTAG controller (active low).

NOTE:
"Barred" active low signals do not appear with a bar in the main body of the text.

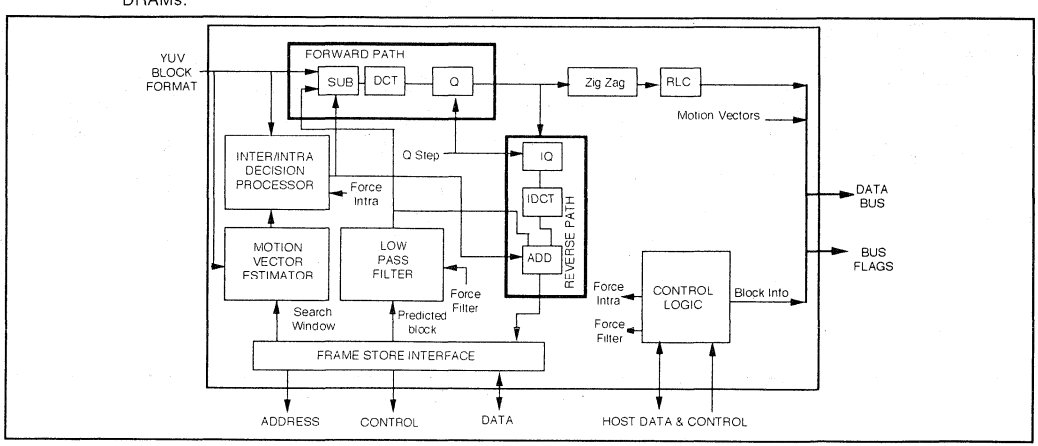


Fig 2 : Simplified Block Diagram

OPERATION OF MAJOR BLOCKS

Motion Vector Estimator

The motion estimator calculates the mean absolute error (MAE) for each possible position of the combined luminance block in a search window from the previous frame. The combined luminance block consists of 16 x 16 pixels, and in the search window this is displaced between -7 to +7 vertically, and -8 to +7 horizontally. The two lsb's of each pixel are discarded and the MAE value is contained within 14 bits.

The minimum MAE value, representing the best match between the previous and current block, is passed to the motion compensation decision block, together with the position of this best fit in the search window. The zero displacement MAE value is also passed to this block, which then decides whether the best fit is sufficiently better than the zero displacement fit. It uses the characteristic shown in Figure 3, where the 14 bit MAE is a Hex value. In the area to the right of the line all points defined by the two MAE values will cause motion compensation to be applied. In this case the best fit MAE value is used by the inter/intra decision processor, otherwise the zero displacement value is used.

Inter/Intra Decision Processor

The MAE value passed by the motion compensation decision block is compared to the simplified variance of the current block. This simplified variance is calculated by summing the moduli of the differences between each luminance pixel and the mean luminance value over the whole macroblock. Eight bit pixels are used, and the variance value is expressed in 14 bits by discarding the two lsb's from the actual 16 bit result. It can then be directly compared to the 14 bit MAE value.

If the MAE value is below a user defined threshold inter mode coding is always selected. The default threshold is 3, on a scale from 0 to 255 using the 8 msb's from the 14 bit value. Above this threshold inter mode is only selected if the variance of the current block is greater than or equal to the MAE value in use.

In order to avoid gradual picture degredation, every 61st Macroblock input to the VP2611 is coded in intra mode regardless of the above decision. As 61 is a prime number, this will ensure that each macroblock will be transmitted in intra mode at least once in every 61 transmissions. If FIX MACROBLOCK or SKIP PICTURE is invoked this 'Force Intra' counter will be disabled.

The user may overide the internal Inter/Intra decision at any time using the CBUS control port. A user generated forced inter mode will overide an internally generated 'Force Intra'.

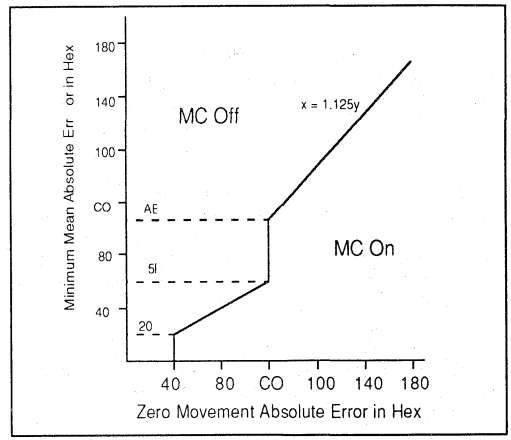


Fig 3 : MC Decision Slope

Low Pass Filter

The macroblock selected from the previous frame in motion compensated inter mode coding, will be filtered before it is subtracted from the current block. This decision can be overidden externally by the system controller. The Filter uses a simple [1 2 1] characteristic in both vertical and horizontal dimensions as specified in H.261 on the macroblock boundaries [010] is used.

SYMBOL	PARAMETER	MINIMUM	MAXIMUM
t RAC	Access time from RAS	-	105ns or under
t CAC	Access time from CAS	-	25ns or under
t RP	RAS precharge time	50ns or under	-
t CP	CAS precharge time	15ns or under	-
t RAS	RAS pulse width	90ns or under	-
t CAS	CAS pulse width	50ns or under	-
t REF	Time to refresh 256 rows	-	0.25ms or over

N.B. All times are quoted assuming 27MHz operation. For lower clock frequencies increase the above values proportionately.

Table 1 : External DRAM timing requirements

Frame Store Manager

The previous picture is stored in an external CIF DRAM frame store, which is connected by a glueless interface. The internal Frame Store Manager controls all read, write, and refresh operations to these DRAMs. No provision is made to allow the use of smaller DRAM's, if only QCIF operation is required.

During the coding of each macroblock columns of the search window are read from these DRAMs, and finally the "best fit" macroBlock is obtained. At the completion of coding the fully processed new macroblock is written to the DRAM's, after it has been decoded again. In this way the frame store maintains a bit-accurate duplicate of the image seen by the Decoder (excepting transmission errors).

Several configurations are possible to make the required 128Kx16 store. Two 64K x 16 DRAMs could be employed; in this case use the default 1M DRAM mode when setting up the chip. Otherwise, a single 256K x 16 DRAM or four 256K x 4 DRAMs could be used. In these last two cases use OE1 as ADR8, RW1 as R/W, and do not connect RW2 and OE2. Also, use the Setup instruction at the CPORT to put the device into 4M DRAM mode.

Table 1 details the critical timing parameters which the external DRAM must meet with SYSCLK running at 27MHz. Note that, if used at slower speeds, the requirements on the DRAM timing are relaxed with the exception of refresh. The number of refresh cycles the VP2611 produces is directly proportional to the SYSCLK frequency.

Discrete Cosine Transform

This circuit performs a Discrete Cosine Transform on each 8x8 sub block, whether in inter or intra mode. In intra mode, eight bit pixel data is used, with a ninth implied sign bit (all pixel data is positive). In inter mode the difference between the current and best fit previous block is used. This will be a two's complement number. Twelve bit coefficients are produced by the DCT, and passed on to the quantizer.

Quantize

This section quantizes the results of the DCT by dividing the 12 bit output from the DCT with a host supplied value. The 5 bit quantization value supplied corresponds to division of the 12 bit coefficients (range ± 2048) by values from 2 to 62, but in steps of 2. This variable quantization strategy allows the volume of data generated by the encoder to be adjusted dynamically, depending on the fullness of the transmission buffer. For H.261 applications it uses the quantisation value provided at the control port during the previous Macroblock period (or at some earlier time). An option is provided which allows two quantisation values to be used, one for use with inter coded macroblocks, and the other for use with intra coded macroblocks.

As specified in H.261, the DC coefficient of an Intra coded Block is treated differently and the 12 bit value is always divided by 8.

When the quantization value is small, and the DCT coefficient is large, there is a danger of overflow in the eight bit output. To avoid this a clipping circuit is included at the output of the quantizer, which saturates at the maximum values.

Zig Zag Scan

This is essentially an address generator which reorders the DCT coefficients according to the standard zig-zag scan pattern. This has the effect of concentrating the significant coefficients at the beginning of the sub-block, improving the efficiency of the Run Length Coder.

Run Length Coder

Each coefficient output from the zig zag scan is examined. If it is non-zero, then the Run Length Coding circuit will pass the coefficient magnitude to the output port along with its zero count i.e. the number of zero magnitude coefficients preceding it within the same 8x8 sub-block.

Inverse Quantize

This circuit replicates the operation of the inverse quantizer in the decoder. It reconstructs the 12 bit DCT coefficients from the 8 bit quantized inputs, using the 5 bit quantization value. This is achieved using the following formulae.

If QUANT is odd :
REC = QUANT*(2*LEVEL+1) : LEVEL > 0
REC = QUANT*(2*LEVEL-1) : LEVEL < 0

If QUANT is even :
REC = QUANT*(2*LEVEL+1)-1 : LEVEL > 0
REC = QUANT*(2*LEVEL-1)+1 : LEVEL < 0

For Intra Coded DC Coefficients :
REC = 8*LEVEL
except if LEVEL=255 when REC=1024

If LEVEL=0 then REC=0 in all cases.

The reconstructed values (REC) are passed through a Clipping Circuit in case of arithmetic overflow.

Thus, the Inverse Quantizer restores the DCT coefficients to their original value but with quantisation error.

Inverse DCT

This circuit replicates the operation of the Inverse Cosine Transform in the Decoder, and outputs 9 bit signed pixel data (intra mode) or pixel difference data (inter mode). The IDCT fully meets the CCITT specification.

Reconstruction Adder

In Inter Mode, the IDCT data is added to the best fit block from the previous frame store. In Intra mode, the IDCT data is simply added to zero. After the adder, the sign bit is removed from the result to give 8 bit pixels. Clipping circuits ensure that any pixels with values exceeding 255 are clipped to 255, and any with negative values are clipped to zero (such values are possible due to quantization noise).

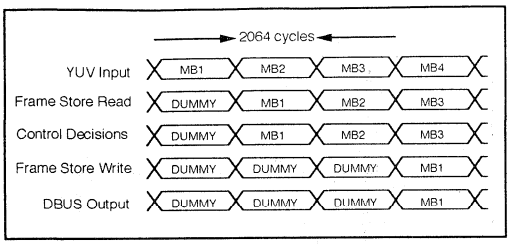


Fig 4: MacroBlock Pipelining

OPERATION OF INTERFACES

Macroblock Delays

The VP2611 has a three macroblock pipeline delay between pixel inputs and run length coded outputs. This is illustrated in Figure 4. Whilst the second macroblock is being input, the best fit macroblock from the previous frame is being identified and then read from the frame store. At this time any Control Decisions which are to effect the first macroblock must be supplied by the host controller. The run length coded outputs for the first macroblock are not available until the fourth macroblock is supplied at the input pins.

YUV Input Port

The YUV port accepts pixel data from the preprocessor in block format as illustrated in Figure 5. Within a complete system the VP2611 is always the master device, and must be supplied with macroblock data when it makes a demand. The order in which pixels are supplied is pre-determined, and must be strictly maintained. There are 64 pixels per sub-block and 4 luminance and 2 chrominance sub-blocks per macroblock. The macroblocks themselves are divided into groups of blocks (GOB's), and the sequence specified in H.261 must also be maintained. Note that, since the chrominance resolution is half the luminance resolution both vertically and horizontally, then the two chrominance blocks cover the same picture area as the four luminance blocks.

The pre-processor producing macroblock data must produce a frame start signal (FRMIN) when it has a complete frame of data available. This resets the input controller within the VP2611, which will then generate sequential GOB and macroblock numbers for the coded outputs referenced to this input.

FRMIN must go high for at least one system clock period, and must go low before the next frame is available. The VP2611 responds to FRMIN with a request for macroblock data (REQYUV), which occurs approximately 184 SYSCLK periods after FRMIN. It must then receive a complete macroblock within 1871 SYSCLK periods, and at the end of this time REQYUV will go inactive. The VP2611 must be provided with a PCLK signal to strobe in the data. This must be derived from SYSCLK, and must only be present when there is valid data at the input. Data must meet the set up and hold times with respect to PCLK as specified in Figure 6.

The maximum peak rate for PCLK is the SYSCLK rate divided by two, but since there are 384 bytes per macroblock

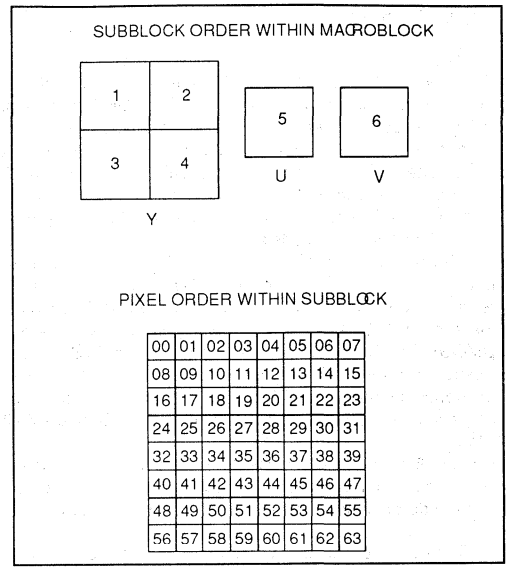


Fig 5 : Ordering of Pixels

then theoretically the average rate need only be 384/1871 times the SYSCLK rate. Note that PCLK must always be obtained by dividing SYSCLK by an integer greater than one. When the VP520 CIF/QCIF Converter is supplying the VP2611 with data, it provides a peak PCLK rate equivalent to SYSCLK divided by two, and an average rate of SYSCLK divided by four.

The mimimum gap between REQYUV going active is 2064 SYSCLK periods. In full CIF mode "dummy" macroblocks are internally inserted between rows, in order to give the chip sufficient time to load a new search window. No new YUV data must be loaded during these dummy macroblocks, and REQYUV will remain inactive. No dummy macroblocks are required in QCIF mode. With a 27MHz SYSCLK all macroblocks will be coded in less than a 30Hz frame rate period, and there will be a period of inactivity before FRMIN goes active again. During this period the output bus will remain static at all ones, and no output strobe (DCLK) will be produced.

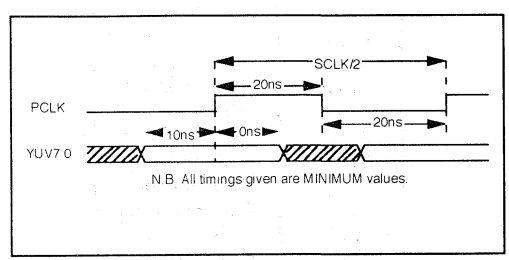


Fig 6 : Timing at YUV Port

DBUS Output Port

The DBUS port is used to pass data and control information directly to the VP2612 Video Multiplexer. The type of data on the output pins is identified by the DMODE 3:0 outputs, using the codes shown in Table 2. An output strobe is also produced (DCLK) which always goes high one system clock period after the data defined by DMODE 3:0 becomes valid. This edge is used to strobe the data into the Video Multiplexer, and thus the data set up time is always one SYSCLK period minus differential output delays.

The number of SYSCLK periods during which data remains valid is dependent on the type of data, and DCLK remains high for this same period. It goes low as the result of the same SYSCLK rising edge which produces a change in DMODE 3:0. The output delays with respect to SYSCLK are illustrated in Figure 8, and Figure 9 shows a typical output sequence during which DCLK remains high for several cycles as the sub-block number (code 7) is produced. During a Wait State
(code 15) no DCLK transitions are produced. The actual sequence of output events which occur for each macroblock, and the duration of each event, are illustrated in Figure 7.

The output events are defined in more detail below;

Control Decisions : This byte shows which control decisions have been taken for the forthcoming macroblock. DBUS0 will be high if a Fixed Macroblock (FIX MB) was enforced i.e. no new data will be transmitted this macroblock. DBUS1 indicates whether Inter (high) or Intra (low) coding was used for the macroblock. DBUS2 will be high if the macroblock was filtered, and DBUS3 will be high if motion compensation was used. DBUS5 will be high if the current frame is being coded in FAST UPDATE mode. In this mode the complete frame will be intra coded. DBUS6 will be high if the current frame is a SKIP FRAME i.e. not being coded - so no coefficients will be transmitted. DBUS4 and DBUS7 are not used.

DMODE3:0	FUNCTION
0000	GOB Number
0001	MB Number
0010	Control Decisions
0011	Quant Value
0100	Horizontal MV
0101	Vertical MV
0110	Coded Blk Pattern
0111	Sub-Block No
1000	Zero Run Count
1001	RLC Coefficient
1010	Not used
1011	Not used
1100	Not used
1101	Not used
1110	Not used
1111	Wait State

Table 2 : DBUS Functions

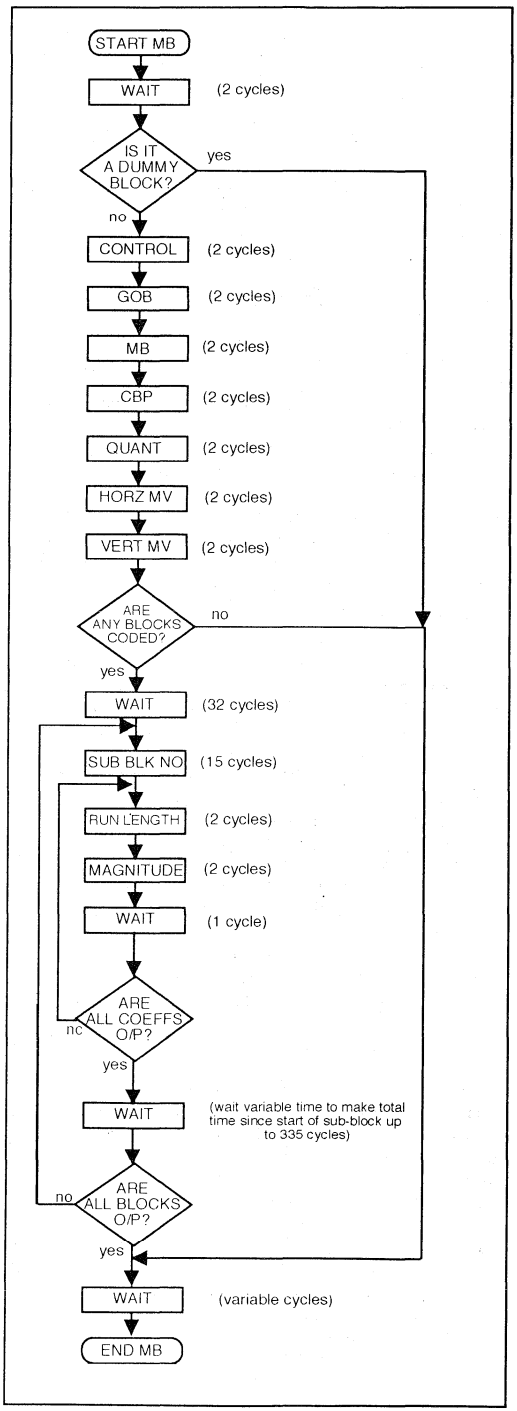


Fig 7 : DBUS Port Flow Chart

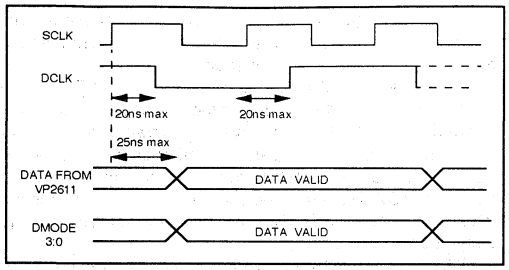


Fig 8: Timing diagram

GOB Number : At the start of each new macroblock, the current GOB Number is output on DBUS3:0. (DBUS3 is MSB).

MB Number : After the GOB Number, the macroblock Number is output on DBUS5:0 (DBUS5 is MSB).

Coded Block Pattern : This byte contains a 6 bit linear code that indicates which of the sub-blocks actually contain coded data. DBUS6 will be high if sub-block 1 contains coded data, through to DBUS 1 being high if sub-block 6 contains coded data. DBUS7 and DBUS0 are not used. Note that if the macro block is not motion compensated and the coded block pattern is all zero's, the fixed macro block bit will be set in the control decisions byte.

Quant Value : The quantisation value used in processing the current macroblock is output on DBUS4:0 (DBUS4 is MSB). This represents an actual quantisation level between 2 and 62, in steps of 2 and as defined in H.261.

Horizontal MV : If motion compensation is used, the horizontal component of the motion vector will be output on DBUS4:0 (DBUS4 is MSB). This 5 bit value represents a two's complement number in the range +/-15 (although only vectors in the range -8 to +7 are currently possible with the VP2611).

Vertical MV : If motion compensation is used, the vertical component of the motion vector will be output on DBUS4:0 (DBUS4 is MSB). This 5 bit value represents a two's complement number in the range ±15 (although only vectors in the range ±7 are currently possible with the VP2611).

CBUS3:0	INSTRUCTION
0000	Input VAR Threshold
0001	Reserved
0010	Input Inter Quantiser
0011	Input Intra Quantiser
0100	Input Setup Data
0101	Input Control Functions
0110	Reserved
0111	Reserved
1000	Output GOB Number
1001	Output MB Number
1010	Reserved
1011	Output Control Decisions
1100	Output Setup Data
1101	Reserved
1110	Reserved
1111	Overide internal clock doubler

Table 3 : CBUS Instruction Codes

Sub-block Number : An identifier for the run length coded coefficients which are about to be made available. DBUS 2:0 contain the coded sub-block number from 1 to 6. All zero sub-blocks will not be produced at the outputs, and their corresponding numbers will not appear.

Zero Run Count : The number of zero valued coefficents preceding the next non zero coefficient is available on DBUS5:0 (DBUS5 is MSB). Normally, DBUS7:6 are low, except to signify the end of a Sub-block, when they will both be high. Zero Run Count is always followed by a coefficient, even at the end of a sub-block.

RLC Coefficient : This byte contains the 8 bit coefficient value. It will always be a non-zero value, except when the previous Zero Run Count signalled the end of sub-Block. A zero value is then possible since, as stated above, the run count is always followed by a coefficient byte, which may be zero if the last coefficient is zero.

Wait State : This indicates that no valid data is being output from the DBUS port during this cycle. No DCLK is produced for this state.

Pins which are "not used" for certain functions will be forced low.

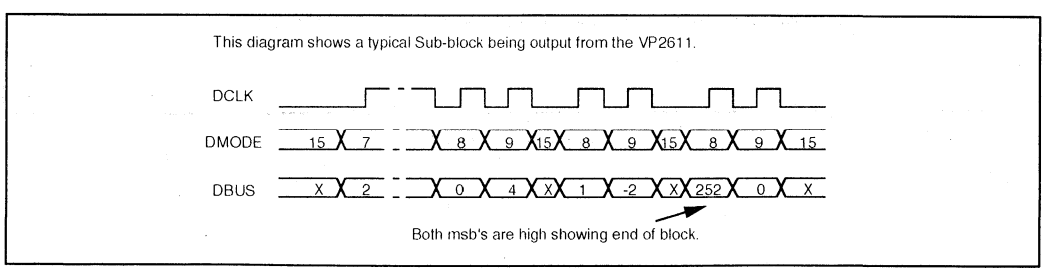


Fig 9: DBUS Timing

CBUS Control Port

The CBUS control port is used to input control and setup information and also to output status information. In order to save on pin count, a microprocessor driving this port is required to execute two I/O instructions in order to transfer a single byte of information to or from the device. The first transfer is always a write operation, with a low level on the single address line which is used by the interface. Data on the bus then defines the instructions listed in Table 3. The second transfer can be a read or write operation as necessary, but the address line must then be high with the set up time given in Figure 10.

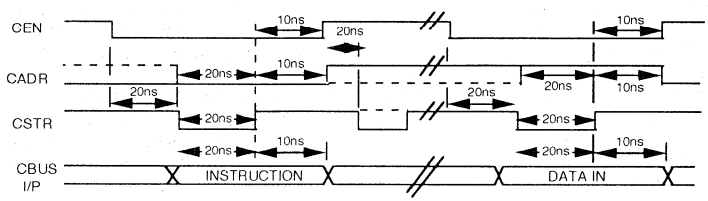
In addition to the single addresss line (CADR), data transfers use a control strobe (CSTR) which is only effective when a chip enable is present (CEN). Detailed timing information is given in Figure 10, and when writing data or instructions to the VP2615 the set up and hold times which are referenced to the rising edge of CSTR must be maintained.

When a write instruction has been defined CADR should be pulled high, valid data presented to CBUS7:0 and then strobed in using CSTR. Other system I/O transfers can occur between defining a write operation and supplying the data to be written, assuming CEN is not active during those other transfers. If CSTR does not go active because of I/O transfers to other devices, then CEN can remain active low between the instruction and data.

When a read instruction has been specified the requested data will then be output on CBUS7:0 after the access time specified from CEN going low, assuming that CADR was already high. Otherwise the data will become valid after the access time specified from CADR going high after CEN was

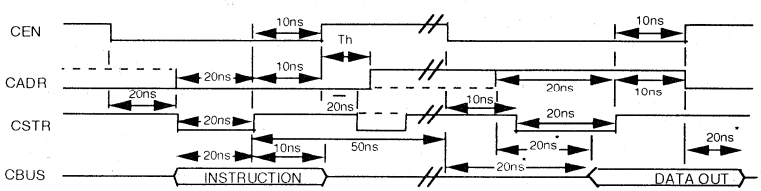
WRITING DATA FROM THE CBUS:

This diagram shows a typical instruction and associated data field being written to the device.



READING INFORMATION ON CBUS :

This diagram shows a typical instruction and associated data field being read from the device.



If Th is less than 5 ns then CBUS may be driven by the VP2615until CEN going high eventually turns off the drivers. It will not prevent correct data being read when CEN again goes active

N.B. All timings shown are minimum values except those marked * which are maximums.

Fig 10 : Use of the Control Port

low. Note that in the data read phase CADR must always go high before CSTR goes high, with the set up time specified. When CEN goes high, or CADR goes low, the CBUS will go high impedance after the delay specified.

Note that the access times under the conditions given above are only true when the gap between CSTR going high in the instruction phase, and CEN going low in the data phase, is greater than the minimum specified in figure 10.

Only the four LSBs, CBUS3:0, are used when writing instructions to the VP2611. The remaining bits, CBUS7:4, should be pulled low while the instruction is strobed into the VP2611.

The instructions listed in Table 3 are described below in greater detail;

Input VAR Threshold: VAR is the difference between the best fit MAE value and the variance of the current macroblock. The VAR Threshold is the best fit MAE value below which Inter Frame Prediction is always used, no matter what the variance of the current block. Above this threshold inter mode coding is only used if the best fit value is less than the current block variance. The default value is 3, within a range of 0 - 255 using the eight most significant bits of the 14 bit value. In normal operation values below 15 should be used.

Input Inter Quantiser: Coefficents of inter coded macroblocks will be quantized using the value on CBUS4:0 following this instruction. Internally this represents a 6 bit number with the lsb always zero, giving a value between 0 and 62 in steps of two. Where only one quantization value is to be used for both inter and intra cases, this instruction should be used. On reset the value will default to the maximum allowed. See note below.

Input Intra Quantiser: This instruction is similar to the above, except that it defines the quantization level for intra mode coding when it is to be different to that of inter mode coding. See note below.

Input Setup Data: This instruction allows several user defined options to be specified, using individual bits in the following data word. If CBUS0 is LOW the device will work in full CIF mode , if HIGH it uses the QCIF mode. If CBUS3 is HIGH both inter and intra quantization values will be used, otherwise a common value will be used. If CBUS5 is high then the motion compensation circuits will be disabled. If CBUS6 is high, then the device will be configured to use 256K x 16 or 256K x 4 DRAM's, otherwise it will assume the use of two 64K x 16 DRAM's. The default conditions after RESET are those selected by the Low level. CBUS1, CBUS2, CBUS4 and CBUS7 are not used but must be low during the definition phase. This instruction may be used any time after RESET has gone high, but the video input bus must not be active. If a subsequent mode change between CIF and QCIF is made then a further RESET is needed.

Input Control Functions: This instruction specifies several control options using individual bits in the following data word. If CBUS0 is HIGH then the on board Inter/Intra Decision circuitry will be overidden according to CBUS1; if CBUS1 is HIGH then all subsequent macroblocks will be intra coded, if it is LOW they will be inter coded. When CBUS2 is HIGH the on-board Filter Decision circuitry is overidden according to CBUS3; if CBUS3 is HIGH then the filter will be forced on, if it is LOW the filter will be forced off. If CBUS4 is HIGH then FIX MB will be implemented, and no new data from the current macroblock will be coded. A two macroblock delay exists between defining the Force Inter/Intra, Force Filter or FIX MB decisions through the control bus and data being affected at the outputs. These decisions will stand for all subsequent macroblocks until they are again changed. If CBUS5 is HIGH a FAST UPDATE will be performed on the next frame and all blocks will be coded in intra mode. If CBUS6 is HIGH then the next frame will not be transmitted (SKIP FRAME). Note that these two global frame bits do not take effect until the start of the next frame, and stay in effect for all frames until they are removed. If CBUS7 is HIGH, then the on-board Force Update Controller will be overidden, and the user will have to enforce their own Force Update policy using the Force Intra command. RESET will cause the options to default to those defined by the LOW state. Note that SKIP FRAME has priority over any other bits and that FIXMB has priority over all bits bar SKIP FRAME. See note below.

Output GOB Number: This instruction will output the GOB Number on CBUS3:0, for the data currently being output on DBUS. CBUS7:4 are not used (always low).

Output MB Number: This instruction will output the macroblock number on CBUS5:0, for the data currently being output on DBUS. If CBUS6 is low it indicates that the macroblock number has just changed, or is about to change. New Quantization Value or Control Function words should not be written at this time since it is uncertain which macroblock they will effect. CBUS7 is not used (always low).

Output Control Decisions: This instruction will output the details of several control decisions on the CBUS. CBUS0 shows whether the MacroBlock currently being output on DBUS was inter or intra coded (0=Intra). CBUS1 shows whether motion compensation was used (1=MC used). CBUS3 shows whether the macroblock was passed through the loop filter or not (1=Filtered). CBUS4 will be high if the FIX MB instruction was enforced. CBUS5 will be high if FAST UPDATE is currently being undertaken. CBUS6 will be high if SKIP FRAME is in force. CBUS2 and CBUS7 are not used.

Output Setup Data: This instruction allows the user to verify the internal setup previously selected. The bits have the same significance as in the Input Setup Data Instruction.

Note

For definitive operation the output MB number should be read first, and these bytes only changed if CBUS b is high.

Initialising the VP2611

On power-up, RESET should be low and must remain low for at least 2064 cycles of SYSCLK. After RESET is pulled high, FRMIN may be activated to start the first frame. Before activating FRMIN for the first time, it is advisable to use the CBUS to implement a FAST UPDATE for the first frame (i.e. all blocks Intra coded).

JTAG Test Interface

The VP2611 includes a test interface consisting of a boundary scan loop of test registers placed between the pads and the core of the chip. The control of this loop is fully JTAG/ IEEE 1149-1 1990 compatible. Please refer to this document for a full description of the standard.

The interface has five dedicated pins: TMS, TDI, TDO, TCK and TRST. The TRST pin is an independent reset for the interface controller and should be pulsed low, soon after power up; if the JTAG interface is not to be used it can be tied low permanently. The TDI pin is the input for shifting in serial instruction and test data; TDO the output for test data. The TCK pin is the independent clock for the test interface and registers, and TMS the mode select signal.

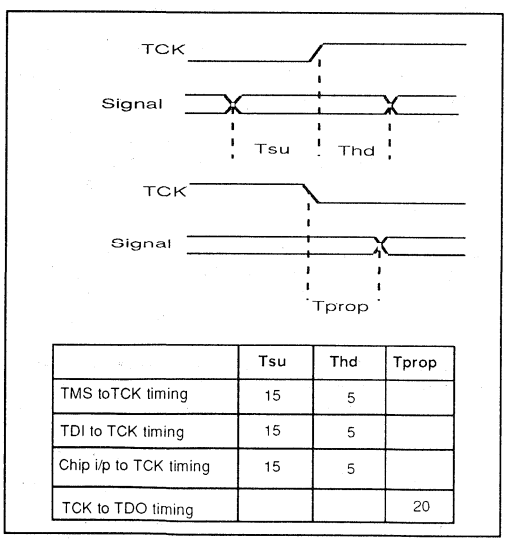
TDI and TMS are clocked in on the rising edge of TCK, and all output transitions on TDO happen on its falling edge.

Instructions are clocked into the 8 bit instruction register (no parity bit) and the following are available.

Instruction Register (MSB first)	Name
11111111	BYPASS
00000000	EXTEST (No inversion)
01000000	INTEST
XX001011	SAMPLE/PRELOAD

Timing details for the JTAG control signals are shown in fig 11. The maximum TCK frequency is 5 MHz.

The test registers, their positions in the boundary loop and the corresponding i/o pad are detailed in Table 4. Note that the three state control signals also have test registers associated with them which are labelled as TRI in Table 4. DHz is an output enable for all signals to the DRAM. The order given in Table 4 determines the serial data stream needed for JTAG testing.



	Tsu	Thd	Tprop
TMS toTCK timing	15	5	
TDI to TCK timing	15	5	
Chip i/p to TCK timing	15	5	
TCK to TDO timing			20

Fig 11 : JTAG Interface timing

Pad	Type	Reg No	Pad	Type	Reg No	Pad	Type	Reg No
RESET	IN	93	DBUS5	OP	62		IN	31
CADR	IN	92	DBUS6	OP	61	SW1	OP	30
CSTR	IN	91	DBUS7	OP	60		IN	29
CEN	IN	90	SW15	OP	59	SW0	OP	28
CBUS0	OP	89		TRI	58		IN	27
	TRI	88		IN	57	DHZ	TRI	26
	IN	87	SW14	OP	56	RAS	OP	25
CBUS1	OP	86		IN	55	CAS	OP	24
	IN	85	SW13	OP	54	RW1	OP	23
CBUS2	OP	84		IN	53	RW2	OP	22
	IN	83	SW12	OP	52	OE1	OP	21
CBUS3	OP	82		IN	51	OE2	OP	20
	IN	81	SW11	OP	50	ADR0	OP	19
CBUS4	OP	80		IN	49	ADR1	OP	18
	IN	79	SW10	OP	48	ADR2	OP	17
CBUS5	OP	78		IN	47	ADR3	OP	16
	IN	77	SW9	OP	46	ADR4	OP	15
CBUS6	OP	76		IN	45	ADR5	OP	14
	IN	75	SW8	OP	44	ADR6	OP	13
CBUS7	OP	74		IN	43	ADR7	OP	12
	IN	73	SW7	OP	42	PCLK	IN	11
DCLK	OP	72		IN	41	YUV7	IN	10
DMODE0	OP	71	SW6	OP	40	YUV6	IN	9
DMODE1	OP	70		IN	39	YUV5	IN	8
DMODE2	OP	69	SW5	OP	38	YUV4	IN	7
DMODE3	OP	68		IN	37	YUV3	IN	6
DBUS0	OP	67	SW4	OP	36	YUV2	IN	5
DBUS1	OP	66		IN	35	YUV1	IN	4
DBUS2	OP	65	SW3	OP	34	YUV0	IN	3
DBUS3	OP	64		IN	33	SYSCLK	IN	2
DBUS4	OP	63	SW2	OP	32	FRMIN	IN	1
						REQYUV	OP	0

Table 4 Pin and JTAG test registers

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage VDD	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to VDD+ 0.5V
Output voltage V_{OUT}	-0.5V to VDD + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HBM)	500V
Storage temperature T_S	-55°C to 150°C
Ambient temperature with power applied T_{AMB}	0°C to 70°C
Junction temperature	125°C
Package power dissipation	3000mW

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation for 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.

STATIC ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise stated)
Tamb = 0 C to +70°C VDD = 5.0v ± 5%

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.0		-	V	V_{DD} -1V for SYSCLK and PCLK
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{DD}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{DD}
Output S/C current	I_{SC}	10		300	mA	V_{DD} = Max

ORDERING INFORMATION

VP2611 CG GH1R (Commercial - Plastic QFP power package)

Pin	Function	Pin	Function	Pin	Function
1	SW3	44	DCLK	87	YUV3
2	NC	45	NC	88	NC
3	SW4	46	CBUS7	89	YUV4
4	SW5	47	VDD	90	YUV5
5	GND	48	CBUS6	91	VDD
6	VDD	49	GND	92	GND
7	SW6	50	VDD	93	YUV6
8	SW7	51	CBUS5	94	YUV7
9	NC	52	GND	95	NC
10	SW8	53	CBUS4	96	PCLK
11	SW9	54	CBUS3	97	NC
12	SW10	55	CBUS2	98	NC
13	SW11	56	CBUS1	99	ADR7
14	NC	57	NC	100	ADR6
15	GND	58	GND	101	ADR5
16	SW12	59	VDD	102	VDD
17	NC	60	CBUS0	103	GND
18	VDD	61	TRST	104	NC
19	SW13	62	CEN	105	ADR4
20	SW14	63	NC	106	ADR3
21	NC	64	NC	107	ADR2
22	SW15	65	CSTR	108	ADR1
23	DBUS7	66	NC	109	GND
24	DBUS6	67	CADR	110	ADR0
25	NC	68	RESET	111	VDD
26	DBUS5	69	VDD	112	GND
27	GND	70	GND	113	NC
28	VDD	71	TCK	114	OE2
29	DBUS4	72	TMS	115	OE1
30	DBUS3	73	TDI	116	VDD
31	NC	74	NC	117	RW2
32	DBUS2	75	TDO	118	RW1
33	NC	76	(CLK54)	119	CAS
34	NC	77	REQYUV	120	RAS
35	DBUS1	78	FRMIN	121	VDD
36	DBUS0	79	VDD	122	GND
37	DMODE3	80	NC	123	NC
38	NC	81	SYSCLK	124	SW0
39	GND	82	GND	125	SW1
40	VDD	83	NC	126	SW2
41	DMODE2	84	YUV0	127	NC
42	DMODE1	85	YUV1	128	NC
43	DMODE0	86	YUV2		

Pin out table for GH128 PQFP package

VP2612

VIDEO MULTIPLEXER

(Supersedes version in June 1995 Digital Video & DSP IC Handbook, HB3923-2)

FEATURES

- Fully integrated H261 video multiplexer
- Inputs data direct from VP2611 source coder
- Output to X21 line buffers
- Line rates from 64kbits/s up to 2Mbits/s
- 100 Pin Quad Flatpack

ASSOCIATED PRODUCTS

- VP2611 H.261 Encoder
- VP2615 H.261 Decoder
- VP2614 Video Demultiplexer
- VP520S CIF/QCIF Converter
- VP510 Colour Space Converter

The VP2612 Video Multiplexer forms part of the GPS chip-set for video conferencing, video telephony, and multimedia applications. This chip set implements the H261 standard for video compression for line rates of between 64K and 2M bits per second. With a 27MHz clock rate full CIF resolution images can be coded at a frame rate of up to 30Hz.

The device contains all the elements necessary to convert the run length coded data from the VP2611 source coder into an H261 compatible bit stream. It also calculates the differential motion vectors and macroblock addresses from the absolute values received from the VP2611. These values are variable length coded, and bit packed for temporary storage in the transmission buffer. The size of this buffer can be either 256Kbits or 512Kbits. Data from the transmission buffer is output through an X21 compatible serial interface, and consists of frames containing framing bits, data, and the BCH (511,493) forward error correction code.

The system processor interface is used to write data for PTYPE, PSPARE, GSPARE, and to select the source of temporal reference. The interface can also be used to monitor the pointers into the transmission buffer, so that the buffer fullness can be controlled using proprietary software algorithms. In addition to the bus interface, flags are supplied which indicate the start of each macroblock, each FEC stuffed frame, the number of bits per picture is reaching the allowable maximum, and impending buffer overflow.

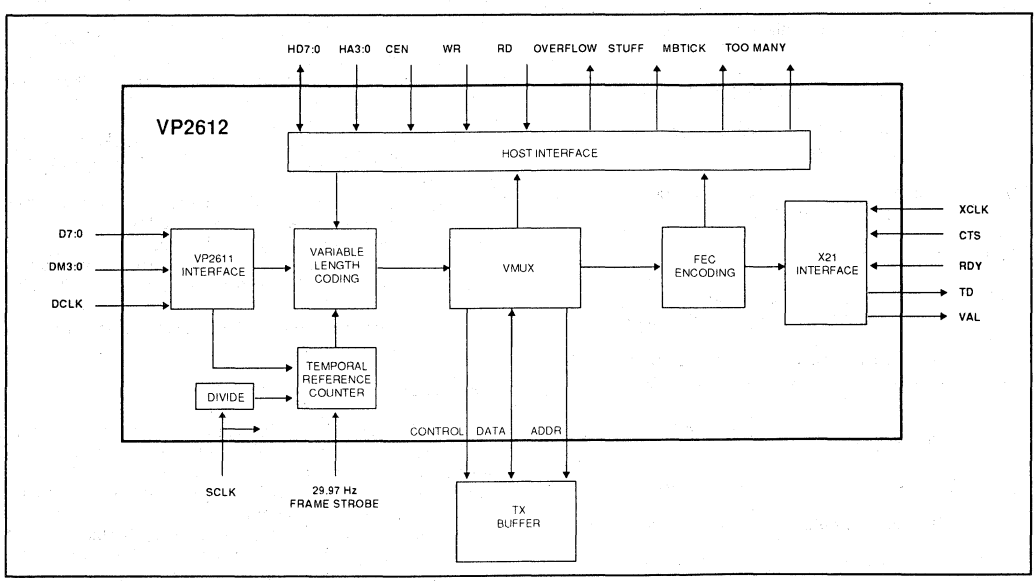


Fig. 1. VP2612 Video Multiplexer

PIN DESCRIPTIONS

DBUS7:0 The input data bus from VP2611. The data type is defined by the value present on DMODE3:0

DMODE3:0 These inputs define the data type present on the data bus D7:0. Polarities are given in Table 1.

DCLK A strobe for DM3:0 and DBUS7:0.The high going edge latches data into the VMUX.

HD7:0 A bidirectional tri-state data bus connecting the VMUX to the system processor.

HA3:0 Four system processor address bits used to address internal registers.

WR An active low write strobe from the system processor.

RD An active low read strobe from the system processor.

CEN An active low chip select input from the system processor.

OVR An active high output which signals impending buffer overflow.

STUFF An active high output that signals that FEC stuffing is occuring.

MTICK An output which pulses high for every macroblock received.

TOOM This active high output indicates that the picture is likely to exceed the allowable number of bits per picture.

VAL This line is taken low to indicate that the VMUX is ready to transmit valid data. The C line in an X21 system.

TD This is the serial data output from the VMUX.

CTS Indicates that the receiver can accept data. The I line in an X21 system.

RDY Indicates that the receiver can accept data. The R line in an X21 system.

XCLK X21 line clock input. 0 to 2.048MHz.

SCLK System clock input. Only the high going edge is used internally, apart from TXWE generation.

FS A 29.97 Hz frame strobe for the temporal reference counter. Must be high for at least 4 SCLK periods.

RES Active low reset signal. Must be low for at least 16 SCLK periods.

TXA14:0 Address output to Transmission buffer.

TXD7:0 Bidirectional data interface to Transmission buffer.

TXE1 Active low chip enable for the Transmission buffer. If a 256kBit buffer is being used this Chip Enable should be used.

TXE2 Active low chip enable for the Transmission buffer. This is used for the optional second memory chip, if a 512kBit buffer is being used.

TXWE Active low write enable for the Transmission buffer.

TXOE Active low O/P enable for the Transmission buffer.

TCK Test clock for JTAG.

TMS Test mode select.

TDI Test data I/P.

TDO Test data O/P.

TRST JTAG reset.

TOE When low ALL O/P pins are high impedance.

NOTE: "Barred" active low signals do not appear with a bar in the main body of the text.

OPERATIONS OF MAJOR BLOCKS

Variable Length Coding

This block is responsible for ordering the data from the VP2611 Encoder into the correct sequence for the H261 bit stream, and for performing the variable length coding. It also uses data supplied by the system controller and the Temporal Reference Counter.

Data for PTYPE, PSPARE, GSPARE is only obtained from the system controller, and only 8 bits of PSPARE and GSPARE information can be transmitted per picture or GOB respectively. The temporal reference can either be obtained from an internal counter, from the VP2611 outputs, or can be written by the system controller. The actual source is determined by bits in a control register as described later. The internal counter is clocked from either a frame clock with a maximum frequency of 29.97Hz, or a 29.97Hz clock derived from the 27MHz system clock, or it simply counts H.261 frames from the encoder.

There is no support provided for macroblock stuffing, however FEC stuffing is implemented, and can be used to provide bit stuffing.

This block is also responsible for converting the absolute values that are output from the V2611 into the relative values that are required in parts of the H261 bitstream. The VMUX has been designed so that it can accept ±15 motion vectors, rather than the +7/-8 motion vectors produced by the VP2611. Thus it will be compatible with any future upgrades to the VP2611 that increase the size of the motion estimator search window.

VMUX Block

The VMUX section performs the bit packing on the data coming from the variable length coder. This data is in the form of a delimiter and a variable number of valid bits. The VMUX section packs these variable length fields into bytes for storage in the transmission buffer.

The transmission buffer is controlled by this block. It thus generates read and write pointers, and performs the arbitration between read and write operations. Buffer level

monitoring is, however, done by the FEC block as described later.

The two address pointers can be read by the system processor, thus allowing the level of the buffer to be monitored. These are provided as 16 bit words with no truncation, and thus require two bytes. The 16 bit value is internally frozen when the most significant byte is requested by the system processor, and for accuracy the write pointer should be read first. There is also a control register bit which selects a buffer size of either 256kbits or 512kbits.

FEC Block

The FEC section performs the framing, and adds the error correction parity bits. If sufficient data for a frame is not available in the transmission buffer, then the frame will be stuffed automatically. There is no absolute threshold at which the FEC will start to stuff, as the buffer level monitor in the FEC only works to a resolution of ±128bits. FEC stuffing can also be forced by setting the "Force FEC stuffing" bit in the VMUX/FEC control register.

If the buffer level reaches a threshold, internally set to 512 short of the buffer being full, the OVERFLOW output is asserted.

DMODE3:0	FUNCTION
0000	GOB Number
0001	MB Number
0010	Control Decisions
0011	Quant Value
0100	Horizontal MV
0101	Vertical MV
0110	Coded Blk Pattern
0111	Sub-Block No.
1000	Zero Run Count
1001	RLC Coefficient
1010	Not Used
1011	Not Used
1100	Not Used
1101	Not Used
1110	Not Used
1111	Wait State

Table 1

This is to warn the system processor that drastic action is needed to avert a buffer overflow, which will result in corruption and loss of data. Since the buffer level monitor only works to resolution of ±128bits, then the overflow detection can only be accurate to ±128bits.

VP2611 Interface

The VMUX has been designed to interface directly to the VP2611 encoder, with no buffering. The interface consists of two buses DBUS7:0 and DMODE3:0, and a strobe signal DCLK. The value on DMODE3:0 identifies the data type on DBUS7:0 during the same period (see Table 1).

The output of the VP2611 is structured such that the data on DBUS7:0 and DMODE3:0 is always valid for at least two cycles, and DCLK is high for minimum of one cycle. The rising DCLK edge occurs one cycle after DBUS7:0 and DMODE3:0 are valid, as shown in Figure 2.

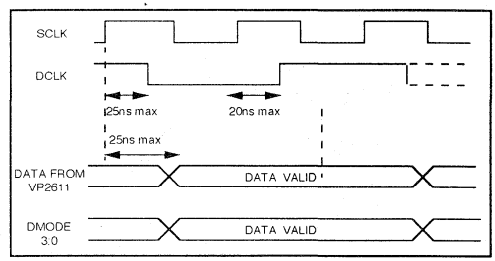


Figure 2. DBUS Timing

The sequence of events, and the duration of each event, is shown in Figure 3. These duration times have been chosen to satisfy the internal requirements of the VP2612, and Wait States are inserted such that the time to transfer a macroblock is always 2064 SCLK periods.

The parameters used by the VP2612 are described in more detail below;

GOB Number : The current GOB Number is provided on DBUS3:0 after the Control Decisions byte. (DBUS3 is MSB).

MB Number : After the GOB Number, the macroblock Number is provided on DBUS5:0 (DBUS5 is MSB).

Control Decisions : This byte shows which control decisions have been taken for the forthcoming macroblock, and is the first in the sequence. DBUS0 will be high if a Fixed Macroblock (FIX MB) was enforced i.e. no new data will be transmitted this macroblock. DBUS1 indicates whether Inter (high) or Intra (low) coding was used for the macroblock. DBUS2 will be high if the macroblock was filtered, and DBUS3 will be high if motion compensation was used. DBUS5 will be high if the current frame is being coded in FAST UPDATE mode. In this mode the complete frame will be intra coded. DBUS6 will be high if the current frame is a SKIP FRAME i.e. not being coded - so no coefficients will be transmitted. DBUS4 and DBUS7 are not used.

Quant Value : The quantisation value used in processing the current macroblock is provided on DBUS4:0 (DBUS4 is MSB). This represents an actual quantisation level between 2 and 62, in steps of 2 and as defined in H.261.

Horizontal MV : If motion compensation was used the horizontal component of the motion vector will be provided on DBUS4:0 (DBUS4 is MSB). (This 5 bit value represents a two's complement number in the range (-15 to +15) (although only vectors in the range +7/-8 are currently possible with the VP2611). If motion compensation was not used this is a don't care value.

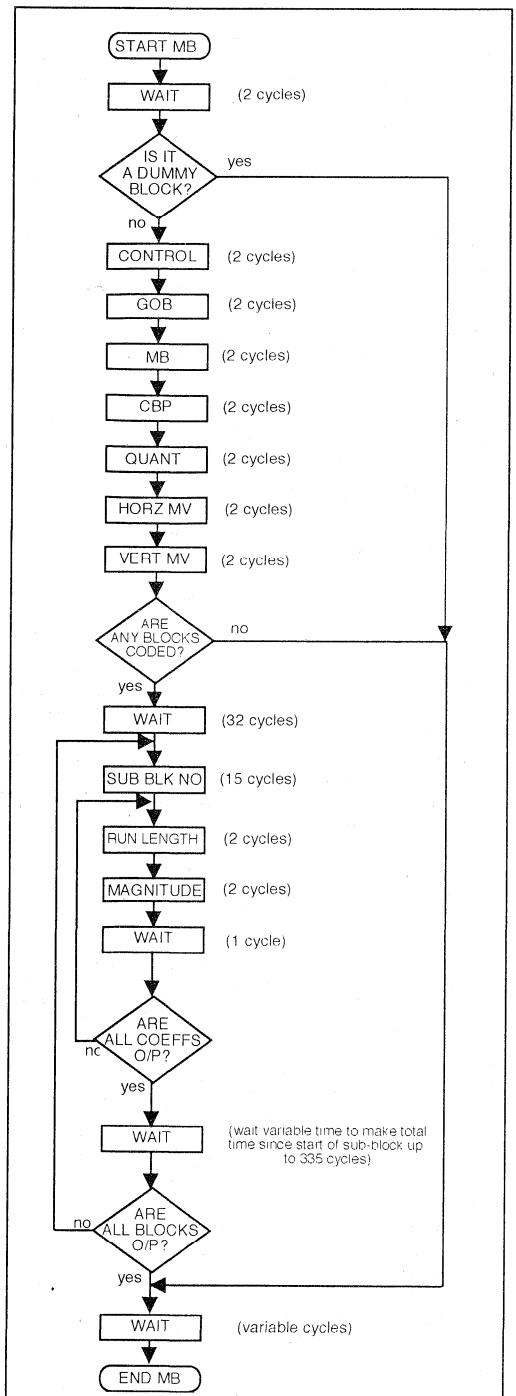


Figure 3. DBUS Port Flow Chart

Vertical MV : If motion compensation was used the vertical component of the motion vector will be provided on DBUS4:0 (DBUS4 is MSB). (This 5 bit value represents a two's complement number in the range ±15 (although only vectors in the range (±7) are currently possible with the VP2611). If motion compensation was not used this is a don't care value.

Coded Block Pattern : This byte contains a 6 bit linear code that indicates which of the sub-blocks actually contain coded data. DBUS6 will be high if sub-block 1 contains coded data, through to DBUS1 being high if sub-block 6 contains coded data. DBUS7 and DBUS0 are not used.

Sub-block Number : An identifier for the run length coded coefficients which are about to be made available. DBUS2:0 contain the coded sub-block number from 1 to 6. All zero sub-blocks will not be produced, and their corresponding numbers will not appear.

Zero Run Count : The number of zero valued coefficents preceding the next non zero coefficient is provided on DBUS5:0 (DBUS5 is MSB). Normally, DBUS7:6 are low, except to signify the end of a Sub-block, when they will both be high. Zero Run Count is always followed by a coefficient, even at the end of a sub-block.

RLC Coefficient : This byte contains the 8 bit coefficient value. It will always be a non-zero value, except when the previous Zero Run Count signalled the end of sub-Block. A zero value is then possible since, as stated above, the run count is always followed by a coefficient byte, which may be zero if the last coefficient is zero.

Wait State : This indicates that no valid data is being output from the DBUS port during this cycle. No DCLK is produced for this state.

SYSTEM PROCESSOR INTERFACE

The system processor interface is a memory mapped microprocessor compatible interface. It has been designed for use with any system processor, and consists of the following buses and signals:

HD7:0	Processor Data Bus
HA3:0	LSBs of address bus
WR	Active Low Write strobe
RD	Active Low Read strobe
CEN	Decoded Active Low chip select

Detailed interface timing is shown in Figure 4. Since there are several internal pipeline registers which are clocked by SCLK, then access times and strobe widths are dependent on the period of SCLK.

Table 2 shows the addresses used for each of the user accessible registers, and the function of each register is described in detail below.

Address	Function	Read / Write
0	PTYPE	W
1	Temporal Reference	W
2	PSPARE	W
3	TR Source	W
4	GSPARE	W
5	Not Used	
6	Not Used	
7	Not Used	
8	TX-buffer Write Address MSB	R
9	TX-buffer Write Address LSB*	R
A	TX-buffer Read Address MSB	R
B	TX-buffer Read Address LSB*	R
C	FEC / VMUX status word	W
D	Bits per Picture Threshold	W
E	Not Used	
F	Not Used	

* N.B. The LSB must be read after the appropriate MSB.

Table 2. Address Locations

PTYPE This is the picture type as defined in H261. The bits are assigned as follows:

Bit 0 Split screen indicator, "0" off, "1" on.
Bit 1 Document camera indicator, "0" off, "1" on.
Bit 2 Freeze picture release, "0" off, "1" on.
Bit 3 Source Format, "0" QCIF, "1" CIF.
Bit 4:5 Both are set to one as presently defined in the H261 specification
[Bit 0 is LSB].

These values can be changed at will by the system processor, and will be transmitted at the start of each picture.

Temporal Reference If the temporal reference is being written from the system processor, then the 5 LSB's in this register are used to define the next temporal reference value to be transmitted.

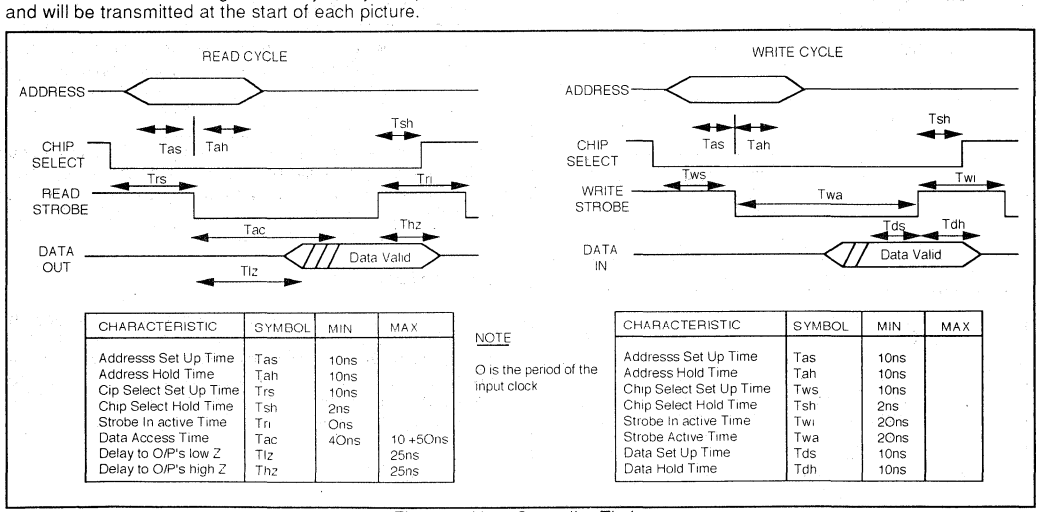
PSPARE This register holds 8 bits of PSPARE information which may be transmitted for each picture. The data in the PSPARE register will be transmitted at the start of the next picture after it has been written. Once an item of data has been transmitted, it will not be re-transmitted until data is written from the system processor. It is the responsibility of the system processor to ensure that it does not rewrite to this register before the previous value has been transmitted. This can be done by utilizing a frame interrupt from the video source in conjunction with the MBTICK output from the VMUX.

TR Source The 3 LSB's in this register define the source for the strobe used by the 5 bit temporal reference counter. When the sytem processor is selected, the counter value is replaced by the contents of the Temporal Reference Register.

VALUE	SOURCE
0XX	System Processor
100	Actual coded frames from the VP2611 are counted
101	SCLK is divided down to provide a 29.97 Hz frame strobe
110	The strobe is provided by the frame strobe input pin (FS)
111	Illegal

GSPARE This register holds 8 bits of GSPARE information which may be transmitted every GOB. Once written the data is transmitted at the start of the next GOB, but will not be re-transmitted until the system processor again writes to this address. The system processor must ensure that data is not overwritten before it is used.

TX Buffer Addresses These allow the system processor to monitor the level of the buffer. The write pointer should be read first to minimize the error between the the two



CHARACTERISTIC	SYMBOL	MIN	MAX
Addresss Set Up Time	Tas	10ns	
Address Hold Time	Tah	10ns	
Cip Select Set Up Time	Trs	10ns	
Chip Select Hold Time	Tsh	2ns	
Strobe In active Time	Tri	Ons	
Data Access Time	Tac	4Ons	10 +5Ons
Delay to O/P's low Z	Tlz		25ns
Delay to O/P's high Z	Thz		25ns

NOTE

O is the period of the input clock

CHARACTERISTIC	SYMBOL	MIN	MAX
Addresss Set Up Time	Tas	10ns	
Address Hold Time	Tah	10ns	
Chip Select Set Up Time	Tws	10ns	
Chip Select Hold Time	Tsh	2ns	
Strobe In active Time	Twi	2Ons	
Strobe Active Time	Twa	2Ons	
Data Set Up Time	Tds	10ns	
Data Hold Time	Tdh	10ns	

Figure 4. Host Controller Timing

values. With a 2Mbits/sec line the error will increase at a rate of 0.25 bytes per microsecond. Reading the most significant bytes will trigger the internal latching of the least significant bytes.

FEC / VMUX Control This register controls the operation of the transmission buffer and the FEC block. Actions taken when bits are set are given below;

BIT	FUNCTION
0	Select 512K buffer. The buffer size must not be changed during normal operation and must be defined within 2.4 ms of reset.
1	Enable FEC framing.The option to disable FEC framing is only provided as a test mode.
2	Force FEC stuffing. If force FEC stuffing is selected it will start at the beginning of the next frame and only stop at the start of subsequent frames. The system processor must ensure that the transmission buffer does not overflow with forced stuffing. In normal operation FEC stuffing only occurs when there is insufficient data in the transmission buffer.

Bits Per Picture Register When the number of bits which have been coded has been subtracted from the maximum possible (as defined by H.261), and the result reaches the value in this register, then the TOO MANY interrupt will be generated. The programmed value thus defines in Kbits the number of bits which may still be generated before reaching the maximum allowed. The default value is 8 Kbits, and the maximum number used internally changes between CIF and QCIF.

INTERRUPT OUTPUTS

The special signals listed below are provided to drive timers and interrupt inputs on the system processor.

OVERFLOW	**(OVR)**
FEC STUFF	**(STUFF)**
MACROBLOCK TICK	**(MTICK)**
TOO MANY	**(TOOM)**

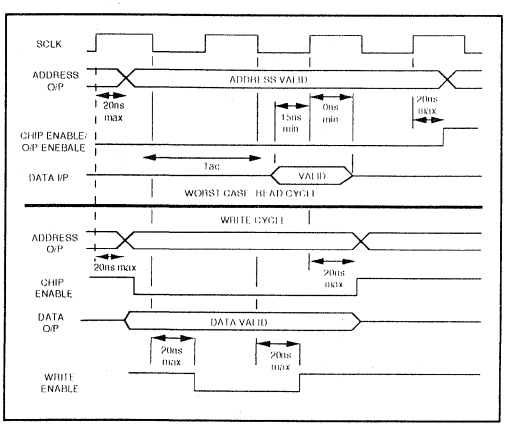


Figure 5. Transmission Buffer Timing

They perform the following functions:

OVR This line signals an impending buffer overflow. When the buffer reaches 512±128 bits from being full this line will be taken high, and will remain high until the buffer level falls below the threshold. It is intended that this line be used as a processor interrupt, to signal that drastic action must be taken.

STUFF This line signals that FEC stuffing is occuring, and can be used to monitor the amount of stuffing being performed. It will pulse high once at the start of each FEC stuffed frame, the length of the pulse being one line clock period. It is intended that this should be used to clock a system processor counter, to keep a running total of the number of FEC stuffed frames.

MTICK This output pulses high once for every Macroblock received from the VP2611. The pulse is 3 clock cycles in duration, and the leading edge will occur 6 SCLK cycles after the Macroblock address was received from the VP2611. It is anticipated that this should be used to clock a counter in the system processor, so that the system processor can keep track of which MB is being processed. In conjunction with the frame pulse this will enable the system processor to write information to the VP2611 at appropriate times.

TOOM This signal indicates that the present picture has reached a threshold relative to the maximum number of bits per picture allowed by H.261 (256k if CIF, 64k if QCIF). It is set when the number of bits remaining before the maximum will be exceeded reaches the value in the Bits Per Picture Register, and stays high until the end of the current picture.

TRANSMISSION BUFFER INTERFACE

The transmission buffer can consist of either one or two 32K x 8 bit static RAMs. Fifteen address outputs are provided for direct connection to the memory devices, and two RAM select pins are provided to define the device in use. If only a single device is being used then CE2 is redundant.
An internal FIFO is provided to average out high speed bursts of transmission buffer cycles. This allows the external SRAM read cycles to occupy at least three SCLK periods. Detailed timing for the buffer is given in Figure 5, and shows that with a 27 MHz clock the RAM must have an access time of less than 39 nanoseconds. Figure 5 illustrates the worst case read access time, which occurs when a second read cycle follows the first without an intermediate write cycle. Chip enable and output enable remain low from the first read cycle.
The write cycle uses two SCLK periods and requires the use of both the falling and rising edges of SCLK. The Write Enable output thus remains active for one SCLK period minus differential rising and falling edge delays. These are limited to two nanoseconds. Note that when consecutive read or write operations take place then Chip Enable will remain active, and not go inactive between cycles.

LINE INTERFACE

A serial interface is provided which facilitates the operation of the encoder and decoder in a back to back configuration. It is similar in operation to an X21 interface but does not support balanced lines. Alternatively the interface can be used in a simple serial manner by tying the control lines to fixed logic levels. It uses the following signals:

XCLK	Line rate clock
VAL	Ready to send
TD	Transmitted Data
CTS	Clear To Send
RDY	Receiver ready

Of these signals XCLK, CTS and RDY are supplied by the receiving device, the latter two indicating that the receiver is ready to accept data. The VAL line is used to signal that the VMUX is ready to start transmitting valid data, and the TD line provides the data. The signaling convention is as follows:

CTS = 1 RDY = 0	Receiving device not ready
CTS = 0 RDY = X	Receiving device ready to accept data
CTS =1 RDY =1	Receiving device ready to accept data

The VAL line is taken high by the reset input, and when the receiving device signals that it is ready to accept data then the VP2612 takes the VAL line low on a falling edge of an XCLK. The data is then clocked out on subsequent falling edges of the XCLK signal, so that it can be sampled by the receiver on the rising edge of the clock.

If a simple serial interface is required, the CTS input should be tied low and the RDY input tied high. It is possible to use a variable rate clock provided the maximum instantaneous bit rate does not exceed 8Mbits/s, and the average clock rate over 32 bits does not exceed 2Mbits/s. Timing delays with respect to the incoming XCLK are shown in Figure 6.

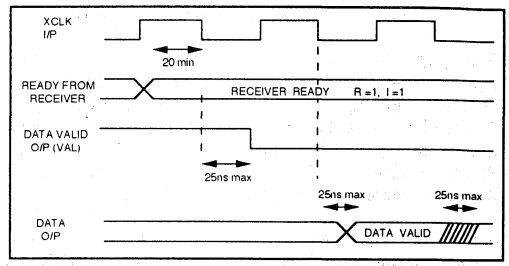


Figure 6. Serial Interface Timing

JTAG Test Interface

The VP2612 includes a test interface consisting of a boundary scan loop of test registers placed between the pads and the core of the chip. The control of this loop is fully JTAG/ IEEE 1149-1 1990 compatible. Please refer to this document for a full description of the standard.

The interface has five dedicated pins: TMS, TDI, TDO, TCK and TRST. The TRST pin is an independent reset for the interface controller and should be pulsed low, soon after power up; if the JTAG interface is not to be used it can be tied low permanently. The TDI pin is the input for shifting in serial instruction and test data; TDO the output for test data. The TCK pin is the independent clock for the test interface and registers, and TMS the mode select signal.

TDI and TMS are clocked in on the rising edge of TCK, and all output transitions on TDO happen on its falling edge.

Instructions are clocked into the 3 bit instruction register (no parity bit) and the following instructions are available.

Instruction Register (MSB first)	**Name**
111	BYPASS
000	EXTEST
010	SAMPLE/PRELOAD

The TAP controller used in this device does not support a separate INTEST instruction but allows EXTEST to drive the internals of the device as well as to drive the output pins. Output enables are thus present in the chain which are not connected to pins but which allow EXTEST to be used to control the impedance of all the outputs. The JTAG signal TXD controls the TXD bus, HD controls the HD bus, and TOPS controls all remaining outputs. The TOE pin, which can separately be used to control the impedance of all the outputs, can be monitored as an input through the scan chain but cannot be used to control the outputs through the TAP controller.

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage VDD	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to VDD + 0.5V
Output voltage V_{OUT}	-0.5V to VDD+ 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HMB)	500V
Storage temperature T_S	-65°C to 150°C
Ambient temperature with power applied T_{AMB}	0°C to 70°C
Junction temperature	100°C
Package power dissipation	1000mW

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.

STATIC ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise stated)
Tamb = 0 C to +70°C VDD = 5.0v ± 5%

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.0		-	V	3.0V for SYSCLK and DCLK
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{DD}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{DD}
Output S/C current	I_{SC}	10		300	mA	

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	N/C	21	GND	41	HD3	61	TXD1	81	TXA1
2	N/C	22	DCLK	42	HD4	62	TXD0	82	TXA0
3	N/C	23	XCLK	43	HD5	63	TXA14	83	TXWE
4	TOE	24	RDY	44	HD6	64	TXA13	84	TXOE
5	OVR	25	CTS	45	HD7	65	TXA12	85	GND
6	DMODE0	26	TD	46	VDD	66	TXA11	86	VDD
7	DMODE1	27	VAL	47	GND	67	TXA10	87	TXE2
8	DMODE2	28	N/C	48	WR	68	TXA9	88	TXE1
9	DMODE3	29	N/C	49	RD	69	TXA8	89	TDI
10	GND	30	N/C	50	CEN	70	TXA7	90	TMS
11	VDD	31	HA0	51	N/C	71	VDD	91	TRST
12	DBUS0	32	HA1	52	N/C	72	GND	92	TCK
13	DBUS1	33	HA2	53	TXD7	73	TXA6	93	TDO
14	DBUS2	34	HA3	54	TXD6	74	TXA5	94	VDD
15	DBUS3	35	SCLK	55	TXD5	75	TXA4	95	GND
16	DBUS4	36	GND	56	TXD4	76	TXA3	96	RES
17	DBUS5	37	VDD	57	TXD3	77	TXA2	97	MTICK
18	DBUS6	38	HD0	58	TXD2	78	N/C	98	STUFF
19	DBUS7	39	HD1	59	GND	79	N/C	99	TOOM
20	VDD	40	HD2	60	VDD	80	N/C	100	FS

Pin Out Diagram

PAD	TYPE	REG No.	PAD	TYPE	REG No.
TXE1	O/P	88	HD5	(input)	44
TXE2	O/P	87	HD4	(output)	43
TX0E	O/P	86	HD4	(input)	42
TXWE	O/P	85	HD3	(output)	41
TXA0	O/P	84	HD3	(input)	40
TXA1	O/P	83	HD2	(output)	39
TXA2	O/P	82	HD2	(input)	38
TXA3	O/P	81	HD1	(output)	37
TXA4	O/P	80	HD1	(input)	36
TXA5	O/P	79	HD0	(output)	35
TXA6	O/P	78	HD0	(input)	34
TXA7	O/P	77	HD	I/P	33
TXA8	O/P	76	SCLK	I/P	32
TXA9	O/P	75	HA3	I/P	31
TXA10	O/P	74	HA2	I/P	30
TXA11	O/P	73	HA1	I/P	29
TXA12	O/P	72	HA0	I/P	28
TXA13	O/P	71	VAL	O/P	27
TXA14	O/P	70	TD	O/P	26
TXD	I/P	69	CTS	I/P	25
TXD0	(input)	68	RDY	I/P	24
TXD0	(output)	67	XCLK	I/P	23
TXD1	(input)	66	DCLK	I/P	22
TXD1	(output)	65	DBUS7	I/P	21
TXD2	(input)	64	DBUS6	I/P	20
TXD2	(output)	63	DBUS5	I/P	19
TXD3	(input)	62	DBUS4	I/P	18
TXD3	(output)	61	DBUS3	I/P	17
TXD4	(input)	60	DBUS2	I/P	16
TXD4	(output)	59	DBUS1	I/P	15
TXD5	(input)	58	DBUS0	I/P	14
TXD5	(output)	57	DMODE3	I/P	13
TXD6	(input)	56	DMODE2	I/P	12
TXD6	(output)	55	DMODE1	I/P	11
TXD7	(input)	54	DMODE0	I/P	10
TXD7	(output)	53	OVR	O/P	9
CEN	I/P	52	TOE	I/P	8
RD	I/P	51	TOPS	I/P	7
WR	I/P	50	TSE	I/P	6
HD7	(output)	49	DEN	I/P	5
HD7	(input)	48	FS	I/P	4
HD6	(output)	47	TOOM	O/P	3
HD6	(input)	46	STUFF	O/P	2
HD5	(output)	45	MTICK	O/P	1
			RES	I/P	0

JTAG Register Allocation

ORDERING INFORMATION

VP2612 CG GPFR (Commercial - Plastic QFP package)

DS3735 - 3.2

VP2614

H.261 VIDEO DE-MULTIPLEXER

(Supersedes version in June 1995 Digital Video & DSP IC Handbook, HB3923-2)

FEATURES

- Fully integrated H.261 video de-multiplexer
- Inputs an H.261 bitstream. Outputs error corrected run length coded coefficients.
- Interfaces directly to the VP2615 H.261 decoder
- Extracts side information and status for transfer to a System Controller
- User definable system level options for proprietary applications
- Average input rates between 40 Kbit /sec and 2Mbit / sec. Maximum peak input rates of 4 Mbit / sec.
- 100 pin quad flatpack

ASSOCIATED PRODUCTS

- VP2611 H.261 Encoder
- VP2612 H.261 Video Multiplexer
- VP2615 H.261 Decoder
- VP520S CIF / QCIF Converter
- VP510 Colour Space Converter

DESCRIPTION

The VP2614 Video De-Multiplexer forms part of the GPS chip set for video conferencing, video telephony, and multimedia applications. It extracts video parameters and run length coded DCT coefficients from an H.261 bitstream. Elements of the data which have been variable length coded according to the specification are decoded within the device. It produces tagged data, aligned to a macroblock timing structure, in the format needed by the VP2615 Decoder. Side information and status bits are separately made available for the system controller.

The VP2614 will accept data up to a peak rate of 4 Mbits per second, but with an average rate up to 2 Mbits per second. The bursty nature of the input, together with the fact that each coded picture does not use the same number of bits, requires the provision of a received data buffer. Since the VP2615 Decoder accepts macroblock data as it becomes available, it is not necessary to provide storage for a complete coded picture. Worst case analysis has shown that a buffer size of 256K bits is adequate in practice for bit rates up to 2Mb/sec.

The incoming sequence is coded with a strict syntax, and the VP2614 must identify and align with this sequence before correct decoding is possible. Storage for this alignment is contained within the external buffer. The device monitors that lock is always valid, and reports to the system controller. Error correction bits are ignored.

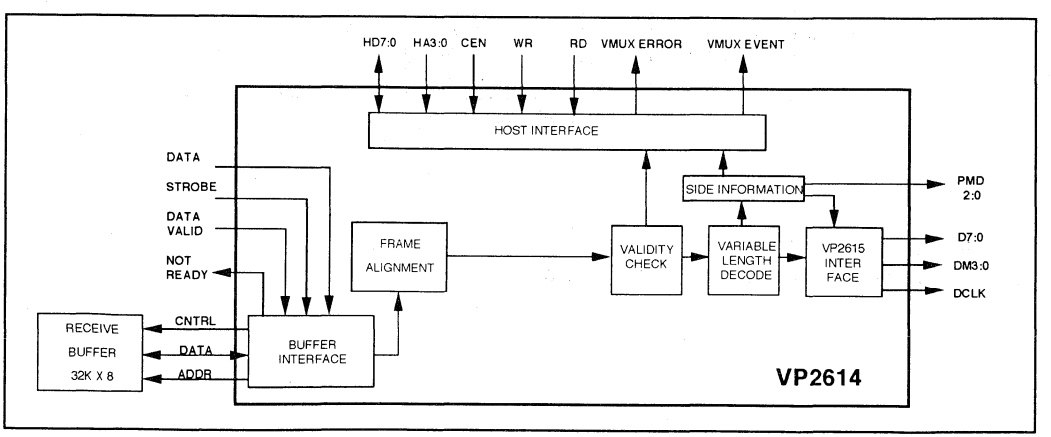


Fig 1 : Simplified Block Diagram

PIN DESCRIPTION

SIG	TYPE	FUNCTION
LD	I	Line input data
LEN	I	When low, the line input data is valid.
LCLK	I	Line input strobe
LRED	O	When low, line data cannot be accepted.
DBUS7:0	O	Data and control bus to the VP2615.
DMODE3:0	O	These outputs identify the data on DBUS7:0.
PM2:0	O	Identifiers for the additional information on DBUS7:0 .Not used by the VP2615.
DCLK	O	Continuous O/P strobe for the DBUS7:0 bus which is derived from SCLK.
SCLK	I	System clock. Must be 27 MHz for 30 Hz frame rates.
HD7:0	I/O	Bi-directional data bus.
HA3:0	I	Four system controller address bits.
WR	I	An active low write strobe from the system controller.
RD	I	An active low read strobe from the system controller.
CEN	I	An active low chip select from the system controller.
ERR	O	An active low output which Indicates framing and decoding errors.
EVT	O	An active low output which Indicates that new picture status data is available.
B7:0	I/O	Bi-directional data bus to the receive buffer.
A14:0	O	Address bus to the receive buffer.
WS	O	An active low write strobe for the receive buffer.
BCS	O	An active low select for the receive buffer.
BEN	O	An active low output enable for the buffer.
TCK	I	JTAG test clock
TMS	I	JTAG mode select
TDI	I	JTAG I/P data
TDO	O	JTAG O/P data
TRST	I	JTAG reset
TOE	I	When low all outputs are high impedance
RES	I	An active low power on reset

NOTE:
"Barred" active low signals do not appear with a bar in the main body of the text.

OPERATION OF THE MAJOR BLOCKS

FRAME ALIGNMENT

The H.261 continuous bitstream is split into frames of 512 bits the first bit in each frame being part of an 8 bit frame alignment pattern. Only the sequence in the pattern is important and detection can start from any bit. To avoid false detection within the actual data, this pattern must be repeated at least three times before " frame lock " can be considered to have been achieved.

The detection of frame lock thus requires data from 24 consecutive 512 bit frames, and a section of the Received Data Buffer is reserved for this purpose. This external RAM is supported by a small internal buffer which allows eight consecutive bits (obtained from reading a byte) to be simultaneously checked for alignment with the corresponding bits in seven other bytes spaced apart by complete frames. The search for alignment over 512 bits takes less than 250 microseconds with a 27 MHz clock, this being less than the time taken to receive 512 bits at the maximum rate of 2Mb/second. Thus the buffer area for frame lock does not overflow.

Once frame lock has been achieved it is continually monitored using the appropriate bit in each frame. If a mismatch occurs then the next four frame alignment bits will be checked for errors. If any one of these four bits is also in error then loss of frame alignment is declared by setting a Status Register Bit, and a search for a new alignment position will commence. If none are in error then a random bit error is assumed and no further action is taken.

The check done on loss of alignment is a compromise between falsely believing that alignment has been lost and not detecting that frame alignment has been lost. The probability of two random bit errors in the five frames used in the check is dependent on the bit rate and also the error rate. With a high error rate of 1:100000, and a bit rate of 2Mb/sec, false detection is possible once per week. The probability of detecting a change in the frame alignment (caused by switching in a new bitstream) is 46.9% in the first five frames, but this rises to 97.4% after 12 frames have been processed.

Control Bits allow H261 framing to be either identified or ignored. In the latter case Frame Lock will always be indicated and data is still buffered and processed. The datastream is then expected to contain pure data and a search will be made to find picture start codes. When framing is enabled the 18 parity bits are extracted from the data, but single bits in error can still go un-detected in some circumstances.

VIDEO LOCK

Once the VP2614 has locked to the H261 frames it will begin searching for the 20 bit unique Picture Start Code. Once this has been identified the "Video Lock" status bit will be set, and the bitstream will be translated on a code by code basis. Video lock will be lost and translation process interrupted under the following conditions:

1) A Picture Start Code or Group of Blocks (GOB) Start Code is not present when expected.

2) The codeword is not valid for its context, causing no match to be obtained. Each variable length code in the bitstream is analysed by the VP2614, and invalid patterns will force Video Lock to be lost.

3) Too many coefficients are transferred for the current macroblock because the End of Block code was missing.

4) GOB number is not in the correct range for the operating mode.

5) A GOB number not in sequence will cause lock to be lost and then regained.

Note that only the most frequently occurring coefficients are variable length coded, the others being represented by an escape sequence followed by a fixed length code. The Intra DC coefficient is also a fixed length code. These fixed length codes have bit patterns which are forbidden in the H.261 specification, but they could appear due to bit errors. These invalid codes are trapped by the VP2614, but do not cause Video Lock to be lost. Instead the run length coefficient is replaced by a default value of magnitude 1. When video lock has been lost the DMODE 3:0 outputs indicate a WAIT state. When lock is regained any missing macroblocks are replaced with Fixed Macroblocks.

A count is maintained of up 256 occurrences of faults 1 - 3, and a status bit is set when lock is lost (the Video Lock Achieved bit is also cleared). An output signal is also provided which can, if required, be used to interrupt the system controller. This indicates any of the above errors which cause Video Lock to be lost and also frame alignment errors; alternatively it can be used to just indicate framing errors.

When Video Lock has been achieved, the detection of a Picture or GOB start code when it is not expected will not cause lock to be lost. Instead the VP2614 will resynchronize to the new start code, and dummy macroblocks will be generated for the missing GOB's. These dummy blocks will be Fixed Macroblocks, and will cause the VP2615 Decoder to use data from the previously decoded picture. Note that Video Lock is actually lost and re-gained under these conditions. The status bit will momentarily be set and then reset, and the Video Lock Lost Counter will be incremented.

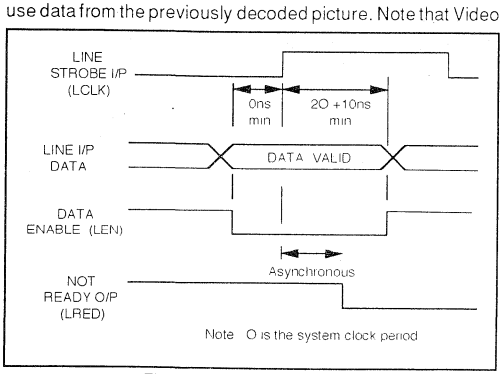


Fig 2 : Line Interface Timing

Similarly any errors in the actual GOB number will not cause lock to be lost and then gained again. Since sequential GOB numbers are always produced by the encoder, then the Decoder generates its own GOB numbers and ignores those in the bitstream.

A Control Bit allows the system controller to take one of two actions when Video Lock is lost. Either the VP2614 can be forced to re-initialize to the next Picture Start Code, or it can abandon the decoding operation until the next GOB Start Code is detected. When lock has been lost, and a new start code has been found, the VP2614 assumes its number to be initially correct and starts its own sequence from that number. If, however, the next number in the bitstream is not in sequence then this new number is used to start a new sequence. This process continues until two sequential numbers are obtained, and then no further checks on the GOB numbers are made until Video Lock is again lost. The VP2614 will generate "Fixed Macroblocks " for the missing GOB numbers since Video Lock was lost, and will output these to the VP2615 decoder. This then uses data from the previous decoded picture for those macroblocks.

A Video Hold bit is provided in one of the System Control Registers which forces Video Lock to be lost immediately. No further data is passed to the VP2615 whilst this bit is set, but the Received Data Buffer is not allowed to fill unnecessarily. Incoming data will be flushed out and lost. When the hold bit is cleared a Picture Start Code must be detected to re-gain Video Lock. The VP2615 will then be provided with any missing GOB's as described above, before GOB's in the new picture are processed.

A Freeze Frame Control Bit is also provided. This has a similar action to the Video Hold Bit, except that it is only actioned when PTYPE has been decoded in the picture layer, and it also sets a Freeze Frame status bit. If Video Lock is lost before the start of a new frame then Freeze Frame will become active and a search will commence for a picture start code. Even though Freeze Frame causes Video Lock to be lost, the VP2614 will still search for picture start codes and will extract PTYPE and Temporal Reference values.

If clear, a Release Mode Control Register Bit will allow the freeze condition to be released when the Freeze Bit is cleared, but is only actioned when the next Picture Header is decoded. If the Release Mode Bit is set, then the freeze condition is only released when the PTYPE bit in the H.261 stream specifies that this is to occur. Even when automatic release has been selected the system controller can still monitor the length of time that the freeze has been in effect. It can then force a release after a time out period by setting the Release Mode Bit and clearing the Freeze Bit.

DE-MUX CORE

Once Video Lock has been achieved, the core of the VP2615 will convert the H.261 bitstream into video parameters and run length coded coefficients. A state machine, which is a hardware manifestation of the H.261 coding structure, maintains the current position in the bitstream. When necessary variable length de-coding is performed, and side information such as temporal reference and Picture Type Information is stored in registers.

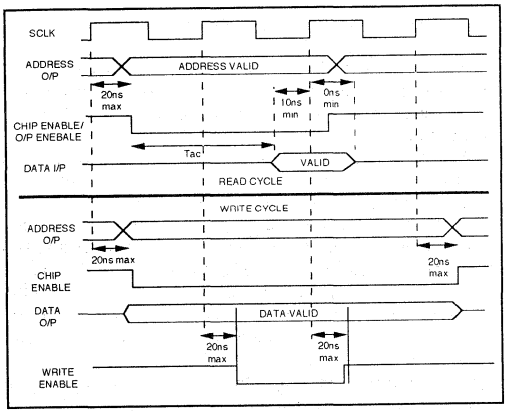


Fig 3 : External Buffer Timing

Not all this side information is used by the VP2615 Decoder, but is still made available on the data output bus DBUS7:0. This is described in the section on Additional Information. In addition the side information can be examined by the system controller.

Requirements for the complete decoder system are such that it is desirable for the VP2614 /15 pair to free run, and to ignore the Temporal References embedded in the video bitstream. The pair then always process the bitstream, whenever code bits are available, using the processing rate needed for the full 30 Hz frame rate. Operating in this manner allows the de-mux core to be closely coupled to the VP2615 Interface circuitry, and no additional buffering is necessary. The demultiplexing process is then locked to the macroblock timing structure needed by the VP2615.

LINE INTERFACE

Bitstream inputs to the device are controlled by an asynchronous line input strobe, which when data is valid is enabled by a Data Valid signal. Detailed timing information is given in Figure 2.

Maximum input frequency is 4 MHz and the rising edge of the strobe is used to internally latch the data. The VP2614 generates a Ready signal which goes invalid when data cannot be accepted. This, for example, occurs during system reset or if the Received Data Buffer overflows.

EXTERNAL BUFFER REQUIREMENTS

The external buffer must be a 32K x 8 bit static RAM, and must comply with the timing requirements given in Figure 3. Under normal operating conditions the buffer will not overflow, however it is conceivable that under some unforseen condition the buffer may fill and then overflow. For this reason a Buffer Full Flag is provided in one of the Status Registers. This is asserted when the buffer is 90% full, and is not itself an error condition. If the buffer continues to fill and eventually overflows, then the Ready Signal to the line interface goes invalid. The effect of overflow is to also clear the buffer and the Buffer Empty Flag will be raised. There is no status bit to indicate overflow, but an extended period of Buffer Full followed by Buffer Empty can be used to infer the condition.

DMODE3:0	FUNCTION
0000	GOB Number
0001	MB Number
0010	Control Decisions
0011	Quant Value
0100	Horizontal MV
0101	Vertical MV
0110	Coded Blk Pattern
0111	Sub-Block No
1000	Zero Run Count
1001	RLC Coefficient
1010	Not used
1011	Not used
1100	Not used
1101	Not used
1110	Not used
1111	Wait State

Table 1. Output Codes

VP2615 INTERFACE

The VP2614 provides a glueless interface to the VP2615 Decoder. Run length coded coefficients and control information are transmitted over the DBUS7:0 bus, and are identified by the code on the DMODE3:0 bus given in Table 1. The VP2614 produces a continuous DCLK which is used to strobe data into the VP2615. This is derived by dividing the system clock by two, and when no data is actually available the DMODE3:0 bus will indicate a wait state. Timing is shown in Figure 4.

The VP2615 expects a macroblock and its control information to be transferred over a minimum period, nominally equivalent to 2048 system clock cycles but with allowance for the asynchronous DCLK. Wait states are thus inserted as necessary by the VP2614 in order to enforce this macroblock period. Under normal circumstances the VP2614 will not take longer than 2048 clock periods to produce a macroblock, but some 10% extra time is available for each macroblock before the 30 Hz frame rate becomes impossible to maintain.

The start of a macroblock transfer is identified by the presence of the Control Decisions Byte (DMODE3:0 = 0010). Each macroblock slot must at least consist of this Control Decisions Byte, followed by the GOB number and then the Macroblock number. No further bytes are mandatory.

When high, Bit 0 in the Control Decisions Byte indicates a Fixed Macroblock, and a high on Bit 1 indicates Inter Mode coding. A high on Bit 2 indicates that the macroblock was filtered, and a high on Bit 3 indicates that Motion Compensa-

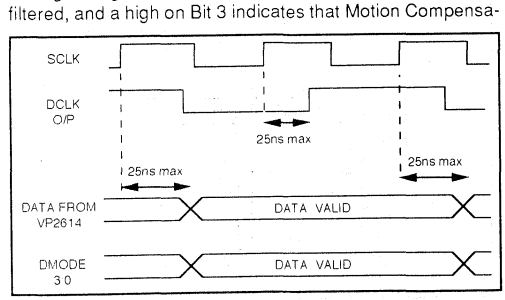


Fig 4 : Output Timing

tion was used. When Bit 7 is high this indicates that CIF resolution is in use, but the VP2615 does not use this information. Instead the host controller must supply this information.

The VP2615 is essentially a Macroblock Processor which produces decoded data for the position on the screen defined by the GOB and Macroblock number. Since the H.261 specification allows macroblocks to be skipped, then the VP2614 generates dummy Fixed Macroblocks if necessary (see below) which are still separated by 2048 clock cycles. Similarly after Video lock has been re-gained the VP2614 will generate Fixed Macroblocks for those missing in the sequence, even if this wraps around into the next picture.

These steps ensure that a complete picture, containing dummy data when necessary, is always supplied by the VP2614. The Fixed Macroblock bit in the Control Decisions Byte is set when dummy data is needed, and Intra Mode decoding is specified. This causes the VP2615 to output macroblock data from the previously decoded picture, which was already in the frame store.

ADDITIONAL INFORMATION

Picture Type, PSPARE and GSPARE information is not used by the VP2615 decoder. In future or proprietary uses of H.261 this information could become considerable and be useful to other devices in the system. This can conveniently be supplied by using the DBUS7:0 bus when the DMODE3:0 bus indicates that a wait state is present and there is no useful information for the VP2615. An additional control bus PM2:0 defines the additional information that is present, with the coding given below:

PM2:0	ADDITIONAL PARAMETER
000	Temporal Reference
001	GSPARE transfer
010	PSPARE transfer
011	PTYPE transfer
100	Quantizer step value
111	Data present is that defined by DMODE3:0

SYSTEM CONTROLLER INTERFACE

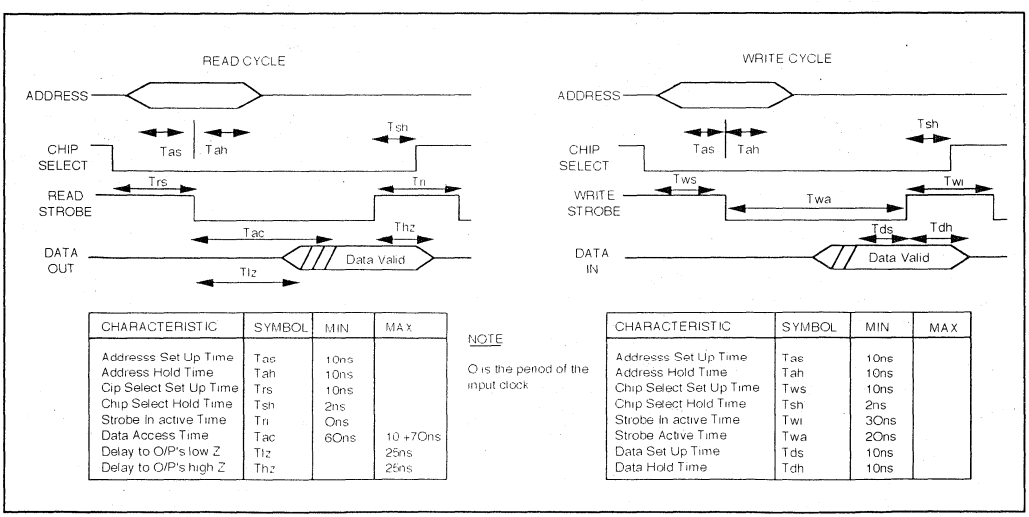
A conventional microprocessor interface is used consisting of a byte wide bi-directional data bus, four address bits, a chip enable and separate read and write strobes. Detailed timing is given in Figure 5.

In addition two outputs are available which can be used as interrupts if necessary. These can be disabled by control bits. When the Error Interrupt Source Bit is set, the ERROR signal indicates that an error has occurred in the FEC frame alignment module. The Frame Lock Lost Status Bit is also set. The output signal is cleared by reading the status register and will be set again when frame alignment is again achieved. If the host has forced a loss of alignment then ERROR does not go active when lock is lost, but it will still go active when lock is regained.

When the Error Interrupt Source Bit is cleared, then the ERR output also goes active when Video Lock is lost. Reading the Status Register will detemine the actual cause of the ERR interrupt.

The EVT signal allows the controller to synchronize with picture related parameters extracted from the bitstream. It goes active when new picture status data is available, as does the Picture Ready bit in Status Register A. This bit and the output signal are cleared when any Status Register is read. The pipeline delay of two macroblock periods through the VP2615 decoder will give the controller time to react to changes in PTYPE affecting the final output of the picture in question. When PTYPE specifies a change between CIF and QCIF, the controller has an amount of time equivalent to that needed to decode the first GOB before it needs inform the VP2615 of the change in operation.

The addresses and functions of the various control and status registers are given below. Setting a Control Bit always performs the function specified, and a high in a Status Register indicates the state is true. All error counters saturate at their maximum values, and are prevented from changing whilst being read.



CHARACTERISTIC	SYMBOL	MIN	MAX
Addresss Set Up Time	Tas	10ns	
Address Hold Time	Tah	10ns	
Cip Select Set Up Time	Trs	10ns	
Chip Select Hold Time	Tsh	2ns	
Strobe In active Time	Tri	Ons	
Data Access Time	Tac	6Ons	10 +7Ons
Delay to O/P's low Z	Tlz		25ns
Delay to O/P's high Z	Thz		25ns

NOTE

O is the period of the input clock

CHARACTERISTIC	SYMBOL	MIN	MAX
Addresss Set Up Time	Tas	10ns	
Address Hold Time	Tah	10ns	
Chip Select Set Up Time	Tws	10ns	
Chip Select Hold Time	Tsh	2ns	
Strobe In active Time	Twi	3Ons	
Strobe Active Time	Twa	2Ons	
Data Set Up Time	Tds	10ns	
Data Hold Time	Tdh	10ns	

Fig 5 : Host Controller Timing

SUPPLEMENTARY NOTE:
To avoid problems with register loading, the VP2614 requires two write operations with no read strobe in between. The absence of chip enable with the read strobe does not prevent this problem. Thus if I/Os are memory mapped it will be necessary to externally gate the read strobe with chip enable for the VP2614 and to do two writes for every load operation.

STATUS REGISTER A (ADDRESS 0)

BIT	FUNCTION
0	GSPARE Byte Available (FIFO not Empty)
1	Freeze Frame
2	Buffer Full
3	Buffer Empty
4	Picture Information Ready
5-7	Unassigned

STATUS REGISTER B (ADDRESS 1)

BIT	FUNCTION
0	Frame Lock Lost
1	Frame Lock Achieved
2	Video Lock Lost
3	Video Lock Achieved
4 -7	Unassigned

CONTROL REGISTER A (ADDRESS 2)

BIT	FUNCTION (when the bit is set)
0	Freeze Frame released by bit stream
1	Force Freeze Frame
2	Error interrupt only from Frame Lock
3	Enable EVT Interrupt
4	Enable ERR Interrupt
5	Video Hold
6	Clear Buffer
7	System Re-start

CONTROL REGISTER B (ADDRESS 3)

BIT		FUNCTION (when the bit is set)
0		Re-lock to Picture Start Code
1-2		Unassigned
4	000	FEC Framing Off
5:3	101	FEC Framing On
6		Clear Video Lock Lost Counter
7		Clear other Counters apart from above

Note: Control Register B must be loaded with the required values before Register A is programmed.

USER READABLE COUNTERS

ADDRESS	FUNCTION
4	FEC Frame Count
5	Filled Frames Count
9	Video Lock Lost Count

PICTURE STATUS REGISTERS

10	Temporal Reference Register
11	Picture Information (see below)
12	First PSPARE Byte
13	Second PSPARE Byte
14	Top of GSPARE Stack

PICTURE INFORMATION REGISTER (ADDRESS 11)

BIT	FUNCTION
7	PSPARE Byte 2 Valid (cleared by reading byte)
6	PSPARE Byte 1 Valid (cleared by reading byte)
5	Split screen
4	Document camera
3	Freeze frame
2	CIF/QCIF
1:0	Set to one

[Bit 0 is LSB]

A master - slave arrangement is used for the Picture Status Registers, and the slave is not updated for the duration of the host read operation plus 32 system clock cycles.

Reading any of the counter values (address 4-9) or any Picture Status Register (address 10-13) causes all values in the respective blocks to be frozen for 32 clocks, thus allowing a complete snapshot to be taken of the respective values.

Two bytes of PSPARE data are stored and further bytes will be lost. Note that the VP2612 Video Multiplexer presently only provides one byte of PSPARE information. A FIFO is provided to provide storage for 12 GSPARE bytes, and a status bit is provided to indicate that this FIFO is not empty, and that the byte at the top of the stack should be read.

RESET OPERATION

In addition to the hardware reset there are several software reset options which are selective in their action. The hardware reset input will initialize all the internal circuit blocks, and will clear all status registers, error counters, and address pointers. The bits in Control Registers A and B are cleared except that the Video Hold Bit in Register A is set, and Bits 0,4, and 5 are set in Register B. The device will thus re-lock to a Picture Start Code, will correct 2 bit errors, and FEC Framing will be on. The circuit which interfaces to the VP2615 Decoder is reset to the end of picture condition (Macroblock 33 in GOB 12).

The System Re-start bit (Bit 7 in Control Register A) will clear all status bits and will initialize the bitstream decoder, the forward error corrector, and the buffer alignment modules. It should be used if there has been an interruption in the bitstream, and does not affect the circuit producing GOB's and macroblocks for the VP2615 Decoder. Thus, after the re-start, Video Lock can be obtained on a GOB boundary, and Fixed macroblocks can be generated for missing macroblocks within the same picture.

The Clear Buffer bit (Bit 6 in Control Register A) will reset the read and write address pointers for the external buffer. A full software restart requires both Bit 7 and Bit 6 to be set.

Two bits are also provided in Control Register B for reset operations. One will clear the Video Lock Lost counter, the other clears the FEC frame counter, the Filled Frames counter, and the three error counters in the error detection circuit.

JTAG Test Interface

The VP2614 includes a test interface consisting of a boundary scan loop of test registers placed between the pads and the core of the chip. The control of this loop is fully JTAG/ IEEE 1149-1 1990 compatible. Please refer to this document for a full description of the standard.

The interface has five dedicated pins: TMS, TDI, TDO, TCK and TRST. The TRST pin is an independent reset for the interface controller and should be pulsed low, soon after power up; if the JTAG interface is not to be used it can be tied low permanently. The TDI pin is the input for shifting in serial instruction and test data; TDO the output for test data. The TCK pin is the independent clock for the test interface and registers, and TMS the mode select signal.

TDI and TMS are clocked in on the rising edge of TCK, and all output transitions on TDO happen on its falling edge.

Instructions are clocked into the 8 bit instruction register (no parity bit) and the following instructions are available.

Instruction Register (MSB first)	Name
11111111	BYPASS
00000000	EXTEST (No inversion)
10XXXXXX	INTEST (Product test only)
01XXXXXX	SAMPLE/PRELOAD

The positions of the test registers in the boundary loop, and their corresponding functional names, are detailed in Table 3.

INTEST is non-standard and is used for production testing and also to invoke the overall output enable function (TOE) via the scan chain.

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	N/C	21	GND	41	HD3	61	B1	81	A1
2	N/C	22	DCLK	42	HD4	62	B0	82	A0
3	N/C	23	LD	43	HD5	63	A14	83	BEN
4	TOE	24	PM0	44	HD6	64	A13	84	BCS
5	N/C	25	PM1	45	HD7	65	A12	85	GND
6	DMODE0	26	PM2	46	VDD	66	A11	86	VDD
7	DMODE1	27	N/C	47	GND	67	A10	87	WS
8	DMODE2	28	N/C	48	WR	68	A9	88	LRED
9	DMODE3	29	N/C	49	RD	69	A8	89	TDI
10	GND	30	N/C	50	CEN	70	A7	90	TMS
11	VDD	31	HA0	51	N/C	71	VDD	91	TRST
12	DBUS0	32	HA1	52	N/C	72	GND	92	TCK
13	DBUS1	33	HA2	53	B7	73	A6	93	TDO
14	DBUS2	34	HA3	54	B6	74	A5	94	VDD
15	DBUS3	35	SCLK	55	B5	75	A4	95	GND
16	DBUS4	36	GND	56	B4	76	A3	96	RES
17	DBUS5	37	VDD	57	B3	77	A2	97	LEN
18	DBUS6	38	HD0	58	B2	78	N/C	98	LCLK
19	DBUS7	39	HD1	59	GND	79	N/C	99	ERR
20	VDD	40	HD2	60	VDD	80	N/C	100	EVT

Table 2. Pinout

SIGNAL	DIRECTION	JTAG Bit Number	SIGNAL	DIRECTION	JTAG Bit Number
TOE	IN	84	CEN	IN	41
testoeout	OUT	83	B0	IN	40
DMODE0	OUT	82	B1	IN	39
DMODE1	OUT	81	B2	IN	38
DMODE2	OUT	80	B3	IN	37
DMODE3	OUT	79	B4	IN	36
DBUS0	OUT	78	B5	IN	35
DBUS1	OUT	77	B6	IN	34
DBUS2	OUT	76	B7	IN	33
DBUS3	OUT	75	B0	OUT	32
DBUS4	OUT	74	B1	OUT	31
DBUS5	OUT	73	B2	OUT	30
DBUS6	OUT	72	B3	OUT	29
DBUS7	OUT	71	B4	OUT	28
DCLK	OUT	70	B5	OUT	27
LD	IN	69	B6	OUT	26
PM0	OUT	68	B7	OUT	25
PM1	OUT	67	nroeout	OUT	24
PM2	OUT	66	LRED	OUT	23
HA0	IN	65	WS	OUT	22
HA1	IN	64	BCS	OUT	21
HA2	IN	63	BEN	OUT	20
HA3	IN	62	A0	OUT	19
SCLK	IN	61	A1	OUT	18
HD0	IN	60	A2	OUT	17
HD1	IN	59	A3	OUT	16
HD2	IN	58	A4	OUT	15
HD3	IN	57	A5	OUT	14
HD4	IN	56	A6	OUT	13
HD5	IN	55	A7	OUT	12
HD6	IN	54	A8	OUT	11
HD7	IN	53	A9	OUT	10
HD0	OUT	52	A10	OUT	9
HD1	OUT	51	A11	OUT	8
HD2	OUT	50	A12	OUT	7
HD3	OUT	49	A13	OUT	6
HD4	OUT	48	A14	OUT	5
HD5	OUT	47	RES	IN	4
HD6	OUT	46	LEN	IN	3
HD7	OUT	45	LCLK	IN	2
oeout	OUT	44	ERR	OUT	1
WR	IN	43	EVT	OUT	0
RD	IN	42			

Table 3. Boundary scan allocations

Those signals labelled testoeout, oeout, and nroeout, are not connected to ASIC output pins, but are provided on the JTAG boundary scan to enhance the device testability.

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage VDD	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to VDD + 0.5V
Output voltage V_{OUT}	-0.5V to VDD+ 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HMB)	500V
Storage temperature T_S	-65°C to 150°C
Ambient temperature with power applied T_{AMB}	0°C to 70°C
Junction temperature	100°C
Package power dissipation	1000mW

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.

STATIC ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise stated)
Tamb = 0 C to +70°C VDD = 5.0v ± 5%

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.0		-	V	3.0V for SYSCLK and LCLK
Input low voltage	V_{IL}	-		0.8	V	0.6V for SYSCLK and LCLK
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{DD}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{DD}
Output S/C current	I_{SC}	10		300	mA	

ORDERING INFORMATION

VP2614 CG GPFR (Commercial - plastic QFP package)

VP2615

H.261 DECODER

(Supersedes January 1996 Edition, DS3479-3.0)

FEATURES

- Inputs run length coded transform data
- Outputs 8 bit pixels in YUV block format
- Up to full CIF resolution and 30 Hz frame rates
- Supports motion compensation with up to 15 pixel movement
- On chip frame store controller
- 100 pin QFP package

ASSOCIATED PRODUCTS

- VP510 Colour Space Converter
- VP520S Three Channel Video Filter
- VP2611 Integrated H261 Encoder
- VP2612 Video Multiplexer
- VP2614 Video Demultiplexer

DESCRIPTION

The VP2615 decoder forms part of a chip set for use in video conferencing and video telephony applications. It conforms to the CCITT H261 standard, and will decode data coded with full or quarter CIF resolution at frame rates up to 30 Hz.

It accepts run length coded coefficients which have already been error corrected and Huffman decoded, and produces multiplexed YUV data in macro block format after a pipeline delay of two MacroBlocks. As shown in Figure 1, other devices in the chip set then convert this data into full resolution, component or composite, video.

The incoming run length coded data is converted to individual coefficient values in the correct order. Data reconstruction is then performed on a block by block basis by multiplying the quantized coefficients with the original quantization value, and then applying the inverse cosine transform. In the inter frame mode this data is then added to the motion compensated block from the previous frame. This block can be passed through a low pass filter when required. A frame store controller produces addresses which allow the best fit block to be read from the frame store, and which also allow the store to be updated with reconstructed data. Refresh cycles are generated when necessary.

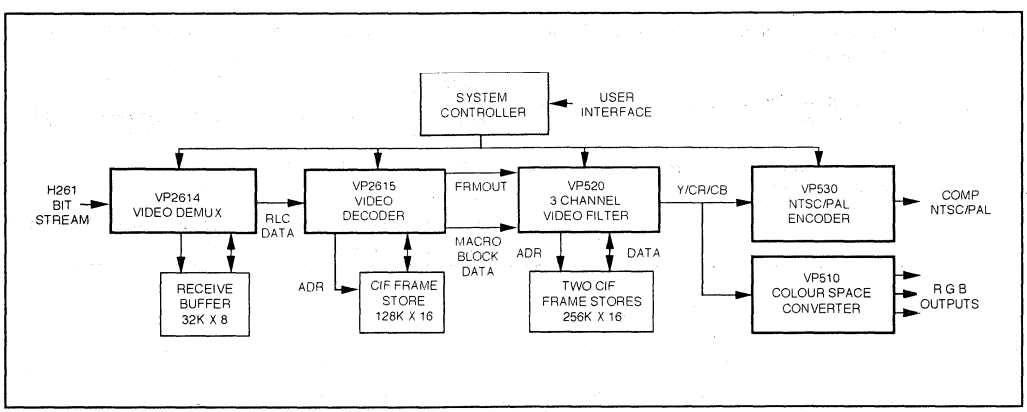


Fig 1 : Typical Video Conferencing Receiver

PIN DESCRIPTIONS

DIN7:0	This port is used to input quantised transform data and control information. Its function is determined by DMODE3:0. Data is clocked in on the rising edge of DCLK.
DMODE3:0	This input controls the function of DIN7:0. Data is clocked in on the rising edge of DCLK.
DCLK	This signal is used to strobe in data at the DIN and DMODE inputs. DCLK can effectively be disabled by inputting a WAIT STATE on DMODE. DCLK must be derived by dividing SYSCLK with an integer greater than one.
YUV7:0	This bus outputs pixel data in YUV block format at quarter SYSCLK frequency.
VPIX	This synchronous output pulses high for two SYSCLK periods when valid pixel data appears at the YUV port. It remains low when inactive.
MBOUT	This synchronous output goes high on the first cycle of a new MacroBlock and stays high until the final pixel of that MacroBlock has been output. At the end of the MacroBlock MBOUT goes low until a new MacroBlock begins.
FRMOUT	This synchronous output goes high to indicate a new Frame is about to begin at the YUV port. It remains high till the last pixel is output. Then, FRMOUT goes low until a new Frame starts.
FS15:0	Data bus for reading and writing to the external DRAM frame store.
ADR7:0	Address bus controlling the external DRAM frame store.
RAS	Row Address Strobe controlling the external DRAM frame store.
CAS	Column address strobe controlling the external DRAM frame store.
RW1	Read/Write control for the external DRAM 1.
RW2	Read/Write control for the external DRAM 2.
OE1	Output Enable control for external DRAM 1 or ADR8 if 256K DRAM's in use.
OE2	Output Enable control for external DRAM 2 N/C if 256k DRAMs in use.
CBUS7:0	Bi-directional data bus for use by a microprocessor. Data and instructions are clocked on and off the chip on the rising edge of CSTR.
CSTR	This input strobes the data in and out of the CBUS port.
CEN	When this pin is low the CBUS port can be used to input or output data.
CADR	When high this signal defines CBUS as data, and when low as an instruction.
SYSCLK	System clock, run at 27MHz maximum. SYSCLK must remain high for 35% to 65% of each cycle. All internal clocks are derived from this clock.
RESET	Active low reset. Must be held low for at least 2048 cycles on power up. If RESET is used during operation, all previous frame data will be lost.
TCK	Test clock for JTAG
TMS	Test mode select for JTAG (Internally pulled high).
TRST	JTAG reset pin (Internally pulled high).
TDI	Input JTAG test data (Internally pulled high).
TDO	Output JTAG test data.

NOTE:
"Barred" active low signals do not appear with a bar in the main body of the text.

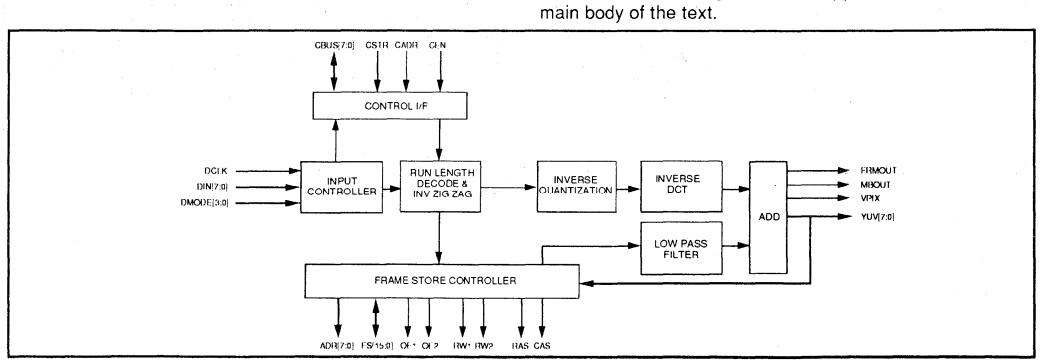


Fig 2 : Simplified Block Diagram

OPERATION OF MAJOR BLOCKS

Run Length Decode

This block converts the run length coded data into 64 individual coefficient values, inserting zero value coefficients where required. It then re-orders these 8 bit quantized DCT coefficients from the zig zag arrangement into normal 8 x 8 format.

Inverse Quantise

This circuit reconstructs the 12 bit DCT coefficients from the 8 bit quantized coefficients using the 5 bit Quantization Value. This is performed using the following formulae.

If QUANT is odd :
REC = QUANT*(2*LEVEL+1) : LEVEL > 0
REC = QUANT*(2*LEVEL-1) : LEVEL < 0

If QUANT is even :
REC = QUANT*(2*LEVEL+1)-1 : LEVEL > 0
REC = QUANT*(2*LEVEL-1)+1 : LEVEL < 0

For Intra coded DC coefficients :
REC = 8*LEVEL
except if LEVEL=255 when REC=1024

If LEVEL=0 then REC=0 in all cases.

The reconstructed values (REC) are passed through a clipping circuit in case of arithmetic overflow.

Inverse DCT

This circuit performs an Inverse Discrete Cosine Transform on an 8x8 block of 12 bit coefficients outputting 9 bit signed pixel data. This IDCT fully meets the CCITT specification.

Frame Store Interface

The whole of the previous picture is stored in either two external 64K x 16 DRAMs, or in a single 256 k x 16 DRAM, or in four 256K x 4 DRAM's. A bit in the user defined Input Set Up Data determines whether 64K or 256K DRAM's are to be used. In the latter case, use OE1 as ADR8, RW1 as R/W and do not connect RW2 and OE2. Table 1 specifies the worst case maximum and minimum times which must be achieved by the DRAM for correct operation with the VP2615. Times in the DRAM specification must be less than or equal to the times stated.

The Frame Store Interface manages all read and write operations to these DRAM's. During the course of each MacroBlock, the "Best Fit" MacroBlock is read from the DRAMs and the fully processed MacroBlock is written back. In this way, the previous frame is continually updated. The DRAM controller also takes care of refresh for the DRAMs.

Figure 3 illustrates the effects of the pipeline delays through the device; whilst macro block 3 is being input the previous macroblock (2) is being decoded and needs the equivalent macroblock from the previous frame to be read from the frame store. At the same time macroblock 1, which has already been decoded, is being written to the frame store

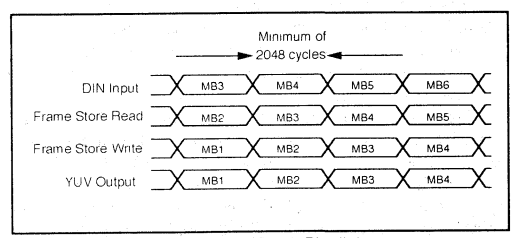


Fig 3 : MacroBlock Pipelining

SYMBOL	PARAMETER	MINIMUM	MAXIMUM
t RAC	Access time from RAS	-	105ns or under
t CAC	Access time from CAS	-	25ns or under
t RP	RAS precharge time	50ns or under	-
t CP	CAS precharge time	15ns or under	-
t RAS	RAS pulse width	90ns or under	-
t CAS	CAS pulse width	50ns or under	-
t REF	Time to refresh 256 rows	-	0.25ms or over

N.B. All times are quoted assuming 27MHz operation. For lower clock frequencies increase the above values proportionately.

Table 1. External DRAM Timing Requirements

for use in the next frame and is also available on the output pins.

Loop Filter

The best matched block from the search window in the previous frame can be passed through a low pass filter to reduce block boundary effects. The filter uses a simple [1 2 1] characteristic in both horizontal and vertical dimensions as laid down in the H261 Specification, on the macroblock boundaries [010] is used. An instruction input at the DIN port defines whether the filter should be used or not.

Reconstruction Adder

In Inter Mode, the IDCT data is added to the best fit block from the previous frame store. In Intra Mode, the IDCT data is added to zero. After the adder, the sign bit is removed from the result to give 8 bit pixels. Clipping circuits ensure that any pixels with values exceeding 255 are clipped to 255 and any with negative values are clipped to zero (such values are possible due to quantization effects).

OPERATION OF INTERFACES

DIN Input Port

The DIN port provides a glueless interface to the VP2614 Video Demultiplexer, from which it will accept run length coded transform data and control information. The general purpose nature of the interface will, however, allow other sources of macroblock data to be used.

Data on the input bus is defined by means of the signals DMODE3:0, and is strobed in with the DCLK signal which is provided by the VP2614 and derived from SYSCLK. Set up and hold times with respect to the rising edge of DCLK are given in Figure 4. If DCLK is a continuous strobe, then the WAIT state defined by DMODE 3:0 should be used to disable any clocking actions. If preferred DCLK can alternatively be

DMODE3:0	FUNCTION
0000	GOB Number
0001	MB Number
0010	Control Decisions
0011	Quant Value
0100	Horizontal MV
0101	Vertical MV
0110	Coded Blk Pattern
0111	Sub-Block No
1000	Zero Run Count
1001	RLC Coefficient
1010	Not used
1011	Not used
1100	Not used
1101	Not used
1110	Not used
1111	Wait State

Table 2 . DIN Mode Functions

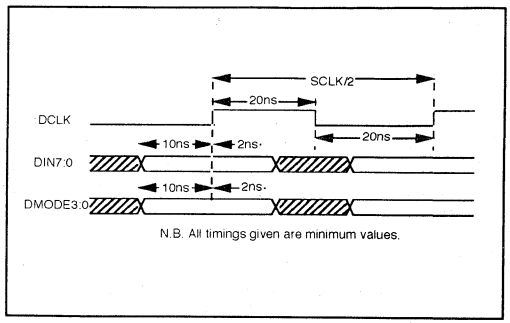


Fig 4 . DIN Port Timing

used as a strobe which is only present when data is valid and action is needed. In this case WAIT states are not strictly necessary.

The VP2615 always expects to receive a complete video frame of data, even if error conditions have occurred in the de-multiplexer. Skip Picture or Fixed Macroblocks should be supplied if necessary once a frame has started. With the latter, decoded data from the previously stored frame will be produced by the VP2615.

The asynchronous interface will allow the use of other video de-multiplexers, as long as the protocol defined by DMODE3:0 is observed. This protocol is defined below, and summerized in Table 2.

Control Decisions : This byte must always be the first in the sequence since it resets the internal control logic. It defines which control decisions were taken when coding the forthcoming MacroBlock. A high on DIN 0 indicates a Fixed Macro Block (ie no change since the previous frame), and a high on DIN1 indicates that Inter coding was used. Similarly a high on DIN2 indicates that the MacroBlock was filtered, a high on DIN3 indicates that Motion Compensation was used. and a high on DIN6 indicates that SKIP PICTURE is in effect. In the latter case the VP2615 will cease processing until SKIP PICTURE is reversed by writing a new Control Decisions byte. Whilst SKIP PICTURE is active, no further data will be output from the YUV port. SKIP PICTURE effectively resets the VP2615, and the next MacroBlock input should be the first of a new frame. Since the frame store will not be updated then the system should ensure that an Intra coded picture is sent as soon as possible.

GOB Number: The correct GOB number is required for every macro block in that group. (DIN3 is MSB).

MB Number: Each macroblock in a group requires an identification number. (DIN5 is MSB).

Coded Blk Pattern: This byte is defined in the H.261 Specification and is used to indicate which sub blocks contain non zero coefficients. It is produced by the encoder but is not used by the VP2615, and if provided will be ignored. The sub block numbering sequence is actually used to indicate blocks with zero coefficients.

Quant Value: This input represents the quantization value

(between 2 and 62 with DIN4 as MSB), which has been used for this macroblock. If no new value is provided for a macroblock then the old value is re-used.

Horizontal MV: This input (on DIN4:0) represents the horizontal component of the motion vector. It must always be provided when motion compensated Inter coding is in use.

Vertical MV: This input (On DIN4:0) represents the vertical component of the the motion vector. It must always be provided when motion compensated Inter coding is in use.

Sub Blk No: Each macroBlock contains 6 Sub-blocks, numbered 1 through 6. The corresponding binary value should be provided on DIN2:0, before the RLC coefficients of that Sub-Block appear. If a Sub-Block contains no coefficients, then its number need not be provided at all, or it can be immediately followed by the next sub block number without any intermediate coefficient values. Even though zero valued sub blocks can simply be ignored in this way, a 2048 clock delay between new macroblocks must still be maintained by the video de-multiplexer.

Zero Run Count: The number of zero valued coefficients preceding the (non-zero) RLC coefficient is defined by this input. DIN 6 and 7 are not used, with the value between 0 and 63 defined by DIN5:0.

RLC Coefficient: This input defines the value of the run length coded coefficient. It will always be a non-zero value

Wait State: This mode should be used on any cycle where no data is being input at the DIN port. Wait States can be

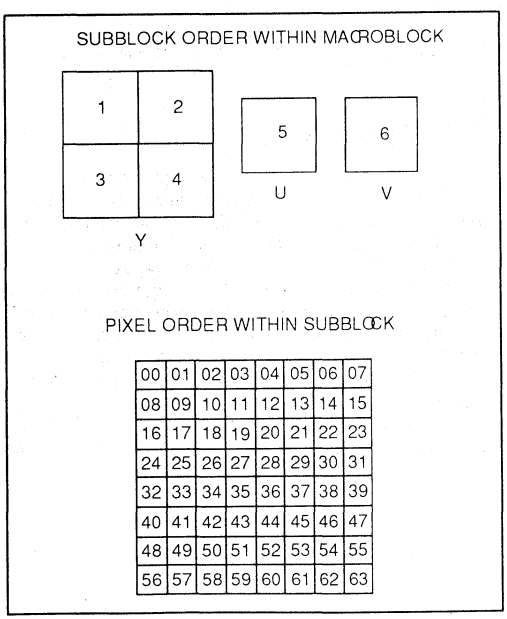


Fig 5 : Ordering of Pixels within MacroBlock

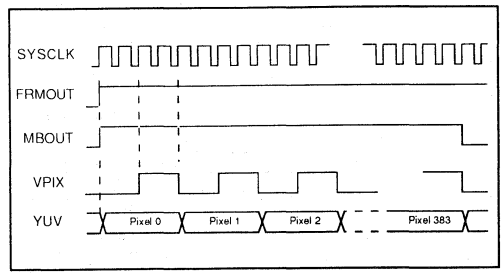


Fig 6 : YUV Port Timing

inserted between any other instructions as required.

Any undefined bits in the above descriptions may be made high or low as desired.

The first information supplied for a macroblock should be that contained within the Control Decisions byte. Receipt of this instruction resets the internal cycle counter for that MacroBlock. Although some Macro Blocks may contain no data, the VP2615 requires that at least the Control Decisions, GOB Number and Macro Block Number be supplied by the de-multiplexer (in that order). All other side information, which is to be provided for a non zero block, must then be supplied before any sub block data can be accepted. GOB's and Macroblocks must be supplied in the correct sequence, but sub blocks within a macroblock can be in any order. The VP2615 does not need to be explicitly informed that the last coefficient has been received within a sub-block. It will wait for a new sub-block number, or a new Macroblock Control Decision Byte, before processing the previous sub-block since it then knows that the sub block is complete.

At least 2048 SYSCLK cycles must separate the start of one Macro Block (identified by receipt of the Control Decisions byte) from the start of the following Macro Block. There are, however, no specific restrictions on the timing of Sub-Blocks within the MacroBlock. The minimum gap between incoming macroblocks is needed for internal processing and also for the time to output 384 decoded values at one quarter the SYSCLK frequency.

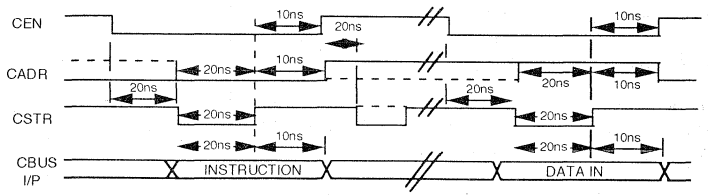
The VP2615 contains two complete macro block buffers in its input circuitry, which swap on the completion of the processing and outputting of the results. Whilst one is used internally the other can be loaded with a new macroblock. It essentially is a macroblock processor and produces the decoded outputs for a macroblock after two macroblock pipeline delays. When it is no longer supplied with macroblock inputs then the pipeline stalls and does not flush out. Thus two macroblocks from a new picture are needed to produce the decoded outputs from the last two macroblocks in a previous picture.

YUV Output Port

Decoded pixel data is presented at the YUV port in standard macroblock format at quarter SYSCLK frequency (6.75MHz max), and in the macroblock order presented at the input. Since the VP2615 always expects a complete picture's worth of GOB's and macroblocks (unless Skip Picture is sent by the video de-mux), then it will always produce a complete

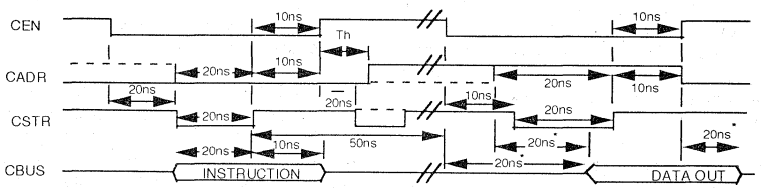
WRITING DATA ONTO THE CBUS:
WRITING DATA FROM THE CBUS:

This diagram shows a typical instruction and associated data field being written to the device.



READING INFORMATION ON CBUS :

This diagram shows a typical instruction and associated data field being read from the device.



If Th is less than 5 ns then CBUS may be driven by the VP2615until CEN going high eventually turns off the drivers. It will not prevent correct data being read when CEN again goes active

N.B. All timings shown are minimum values except those marked * which are maximums.

Fig 7 : CBUS Timing

coded picture. As explained in the previous section, however, it requires to be supplied with two macroblocks from the next picture before a complete frame is fully decoded. The standard macroblock internal configuration is shown in Figure 5.

Output timing is shown in Figure 6. VPIX is toggled high each time a valid pixel is available at the output pins, and remains low when no pixel data is output. MBOUT is used to define the boundaries between MacroBlocks, but is not used when the device is directly connected to the VP520. The Frame Ready Output nominally goes high on the same SYSCLK edge as the first MBOUT goes high, and returns low when the last MBOUT goes low. This will actually be after two macroblocks from the next frame have been supplied as inputs, but this gap will not effect the operation of the VP520 which converts macro block data to full resolution line data. The first VPIX strobe produced after MBOUT goes high, will go high after two SYSCLK periods, with the data being valid for two SYSCLK periods either side of this edge. These delays are subject to internal differential delays and will not be precise clock period delays.

CBUS Control Port

The CBUS control port is used to input control and setup information and also to output status information. In order to save on pin count, a microprocessor driving this port is required to execute two I/O instructions in order to transfer a single byte of information to or from the device. The first transfer is always a write operation, with a low level on the single address line which is used by the interface. Data on the bus then defines the instructions listed in Table 3. The second transfer can be a read or write operation as necessary, but the address line must then be high with the set up time given in Figure 7.

In addition to the single addresss line (CADR), data transfers use a control strobe (CSTR) which is only effective

CBUS3:0	INSTRUCTION
0000	Unassigned
0001	Unassigned
0010	Unassigned
0011	Unassigned
0100	Input Setup Data
0101	Unassigned
0110	Reserved
0111	Reserved
1000	Output GOB Number
1001	Output MB Number
1010	Unassigned
1011	Output Control Decisions
1100	Output Setup Data
1101	Unassigned
1110	Unassigned
1111	Overide internal clock doubler

Table 3: CBUS Instructions

when a chip enable is present (CEN). Detailed timing information is given in Figure 7, and when writing data or instructions to the VP2615 the set up and hold times which are referenced to the rising edge of CSTR must be maintained.

When a write instruction has been defined CADR should be pulled high, valid data presented to CBUS7:0 and then strobed in using CSTR. Other system I/O transfers can occur between defining a write operation and supplying the data to be written, assuming CEN is not active during those other transfers. If CSTR does not go active because of I/O transfers to other devices, then CEN can remain active low between the instruction and data.

When a read instruction has been specified the requested data will then be output on CBUS7:0 after the access time specified from CEN going low, assuming that CADR was already high. Otherwise the data will become valid after the access time specified from CADR going high after CEN was low. Note that in the data read phase CADR must always go high before CSTR goes high, with the set up time specified. When CEN goes high, or CADR goes low, the CBUS will go high impedance after the delay specified.

Note that the access times under the conditions given above are only true when the gap between CSTR going high in the instruction phase, and CEN going low in the data phase, is greater than the minimum specified in figure 7.

Only CBUS3:0 are used to define an instruction. The remaining bits, CBUS7:4, should be pulled low. The instructions are listed in Table 3 but are described below in greater detail;

Input Setup Data: This instruction performs several functions, the details being specified in the data field following this instruction. If CBUS0 is high, the device will operate in QCIF mode, otherwise in full CIF mode. If CBUS6 is high, then the device will be configured to use 256K word DRAM's, otherwise it will assume two 64K word DRAM's. All CBUS inputs not defined above must be pulled low during the set up definition phase and the D/R7:0 bus must not be active. On reset the defaults are 64k DRAMs and full CIF mode. Note that if macroblocks have been received, and a CIF/QCIF mode change is made, then a reset is needed. At the the system level the EVT signal from the de-mux can be used to instigate the controller into reading PTYPE, thus detecting a CIF/QCIF change and forcing a software reset.

Output GOB number: This instruction will make the VP2615 output the GOB Number associated with the data currently being output at the YUV port. The number will appear on CBUS3:0. CBUS7:4 are not used (always low).

Output MB Number: This instruction will make the VP2615 output the Macroblock Number associated with the data currently being output at the YUV port. The number will appear on CBUS5:0. If CBUS6 is low, this indicates that the MacroBlock number has just changed or is about to change, and is thus not reliable.

Output Control Decisions : This instruction will make the VP2615 output control information received through the DIN port. CBUS0 shows whether the MacroBlock currently being output was Inter or Intra coded (0=Intra). CBUS1 shows whether Motion Compensation was used (1=MC used). CBUS3 will be high if the MacroBlock was passed through the Loop Filter. If CBUS6 is high, this indicates that SKIP PICTURE is currently active.

JTAG Test Interface

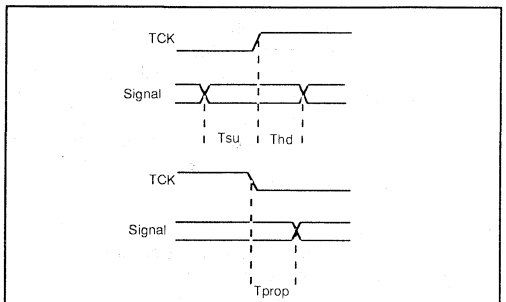
The VP2615 includes a test interface consisting of a boundary scan loop of test registers placed between the pads and the core of the chip. The control of this loop is fully JTAG/IEEE 1149-1 1990 compatible. Please refer to this document for a full description of the standard.

The interface has five dedicated pins: TMS, TDI, TDO, TCK and TRST. The TRST pin is an independent reset for the interface controller and should be pulsed low, soon after power up; if the JTAG interface is not to be used it can be tied low permanently. The TDI pin is the input for shifting in serial instruction and test data; TDO the output for test data. The TCK pin is the independent clock for the test interface and registers, and TMS the mode select signal.

TDI and TMS are clocked in on the rising edge of TCK, and all output transitions on TDO happen on its falling edge.

Instructions are clocked into the 8 bit instruction register (no parity bit) and the following instructions are available.

Instruction Register (MSB first)	Name
11111111	BYPASS
00000000	EXTEST (No inversion)
01000000	INTEST
XX001011	SAMPLE/PRELOAD



	Tsu	Thd	Tprop
TMS toTCK timing	15	5	
TDI to TCK timing	15	5	
Chip i/p to TCK timing	15	5	
TCK to TDO timing			20

Fig 8. Typical JTAG Interface timing

Timing details (minimums) for the JTAG control signals are shown in Figure 8. The maximum TCK frequency is 5 MHz.

The positions of the test registers in the boundary loop, and their corresponding functional names, are detailed in Table 4. Note that any internal signals controlling the impedance of a bus also have associated registers, even though they are not normally available to the user. These are listed as TRI in Table 4.This register order will determine the serial data stream for JTAG testing. The signal DHZ will, if loaded with a logic '1', force all the outputs to a high impedance state.

All bus output enables are invoked through the INTEST instruction.

PAD	TYPE	REG NO	PAD	TYPE	REG NO
DHZ	TRI	93	FS10	IN	46
CADR	IN	92	FS10	OUT	45
CEN	IN	91	FS9	IN	44
CSTR	IN	90	FS9	OUT	43
CBUS0	OP	89	FS8	IN	42
CBUS	TRI	88	FS8	OUT	41
CBUS0	IP	87	FS7	IN	40
CBUS1	OUT	86	FS7	OUT	39
CBUS1	IN	85	FS6	IN	38
CBUS2	OUT	84	FS6	OUT	37
CBUS2	IN	83	FS5	IN	36
CBUS3	OUT	82	FS5	OUT	35
CBUS3	IN	81	FS4	IN	34
SYSCLK	IN	80	FS4	OUT	33
CBUS4	OUT	79	FS3	IN	32
CBUS4	IN	78	FS3	OUT	31
CBUS5	OUT	77	FS2	IN	30
CBUS5	IN	76	FS2	OUT	29
CBUS6	OUT	75	FS1	IN	28
CBUS6	IN	74	FS1	OUT	27
CBUS7	OUT	73	FS0	IN	26
CBUS7	IN	72	FS0	OUT	25
DMODE0	IN	71	ADR7	OUT	24
DMODE1	IN	70	ADR6	OUT	23
RESET	IN	69	ADR5	OUT	22
DCLK	IN	68	ADR4	OUT	21
DMODE2	IN	67	ADR3	OUT	20
DMODE3	IN	66	ADR2	OUT	19
DIN0	IN	65	ADR1	OUT	18
DIN1	IN	64	ADR0	OUT	17
DIN2	IN	63	RW1	OUT	16
DIN3	IN	62	RW2	OUT	15
DIN4	IN	61	DE1	OUT	14
DIN5	IN	60	DE2	OUT	13
DIN6	IN	59	RAS	OUT	12
DIN7	IN	58	CAS	OUT	11
FS15	IN	57	MBOUT	OUT	10
FS	TRI	56	FRMOUT	OUT	9
FS15	OUT	55	VPIX	OUT	8
FS14	IN	54	YUV0	OUT	7
FS14	OUT	53	YUV1	OUT	6
FS13	IN	52	YUV2	OUT	5
FS13	OUT	51	YUV3	OUT	4
FS12	IN	50	YUV4	OUT	3
FS12	OUT	49	YUV5	OUT	2
FS11	IN	48	YUV6	OUT	1
FS11	OUT	47	YUV7	OUT	0

Table 4. Pin and JTAG Test Registers

1	GND	21	DIN7	41	CBUS6	61	TRST	81	RAS
2	N/C	22	DIN6	42	CBUS5	62	TD0	82	OE2
3	FS3	23	DIN5	43	CBUS4	63	YUV7	83	OE1
4	FS4	24	DIN4	44	VDD	64	YUV6	84	GND
5	GND	25	VDD	45	SYSCLK	65	VDD	85	RW2
6	FS5	26	DIN3	46	GND	66	YUV5	86	VDD
7	FS6	27	DIN2	47	CBUS3	67	GND	87	RW1
8	VDD	28	DIN1	48	CBUS2	68	YUV4	88	ADR0
9	FS7	29	N/C	49	CBUS1	69	YUV3	89	ADR1
10	FS8	30	GND	50	CBUS0	70	YUV2	90	ADR2
11	FS9	31	DIN0	51	GND	71	YUV1	91	ADR3
12	GND	32	DMODE3	52	N/C	72	YUV0	92	ADR4
13	FS10	33	DMODE2	53	CSTR	73	VDD	93	ADR5
14	VDD	34	VDD	54	VDD	74	VPIX	94	GND
15	FS11	35	DCLK	55	CEN	75	FRMOUT	95	ADR6
16	FS12	36	GND	56	CADR	76	GND	96	VDD
17	FS13	37	RESET	57	GND	77	MBOUT	97	ADR7
18	FS14	38	DMODE1	58	TD1	78	CAS	98	FS0
19	FS15	39	DMODE0	59	TMS	79	N/C	99	FS1
20	GND	40	CBUS7	60	TCLK	80	GND	100	FS2

Table 5. 100 Pin QFP Pin Assignment

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage VDD	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to VDD + 0.5V
Output voltage V_{OUT}	-0.5V to VDD + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HBM)	500V
Storage temperature T_S	-55°C to 150°C
Ambient temperature with power applied T_{AMB}	0°C to 70°C
Junction temperature	125°C
Package power dissipation	1000mW

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation for 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.

STATIC ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise stated)
Tamb = 0°C to +70°C VDD = 5.0v ± 5%

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.0		-	V	V_{DD} -1V for SYSCLK, DCLK
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{DD}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{DD}
Output S/C current	I_{SC}	10		300	mA	V_{DD} = Max

ORDERING INFORMATION

VP2615 CG GH1R (Commercial - Plastic QFP power package)

VP520S

PAL/NTSC TO CIF/QCIF CONVERTER

(Supersedes version in June 1995 Digital Video & DSP IC Handbook, HB3923-2)

FEATURES

- Lower Power, pin compatible replacement for VP520
- Converts CCIR601 luminance and chrominance to CIF or QCIF resolution, and vice versa, using a 27MHz system clock.
- Luminance and chrominance channels have their own sets of horizontal and vertical filters with on chip line stores
- Each filter set may be configured to either decimate or interpolate.
- NTSC line insertion or removal mode
- Produces / expects CIF/QCIF data in macroblock format.
- 120 Pin QFP Package

ASSOCIATED PRODUCTS

- VP510 Colour Space Converter
- VP2611 H261 Encoder
- VP2615 H261 Decoder
- VP2612 Video Multiplexer
- VP2614 Video Demultiplexer

DESCRIPTION

The VP520S is designed to convert 16 bit multiplexed luminance and chrominance data between CCIR601 and CIF/QCIF resolutions. Vertical and horizontal FIR filters are provided, with the vertical filters supported by on chip line stores. The coefficients used by the filters are user definable, and are down loaded from an independent host data bus. An internal address generator supports an external DRAM frame store, and also provides line to macroblock conversion.

When producing CIF or QCIF video the horizontal filters precede the vertical filters, and are provided with between 8 and 16 taps. The vertical filters are provided with four CIF line delays which allow a 5 tap filter to be implemented. When producing QCIF the available RAM is used to provide six line delays, which thus allows 7 tap filters to be used.

When the device is producing CCIR601 video, the incoming data must be in macroblock format, and the vertical filters precede the horizontal filters The inputs are firstly written to a external CIF sized frame store, and are read out in line format. The VP520S will support two complete frame stores, and allows the CIF/QCIF data to be read out twice in order to produce two interlaced fields of video.

The VP520S supports the conversion between CIF/QCIF and NTSC video. An extra line is produced for every five lines when producing CIF data, and one line in six is removed when producing NTSC video. Poly phase filters are used to provide the correct decimation and interpolation ratios.

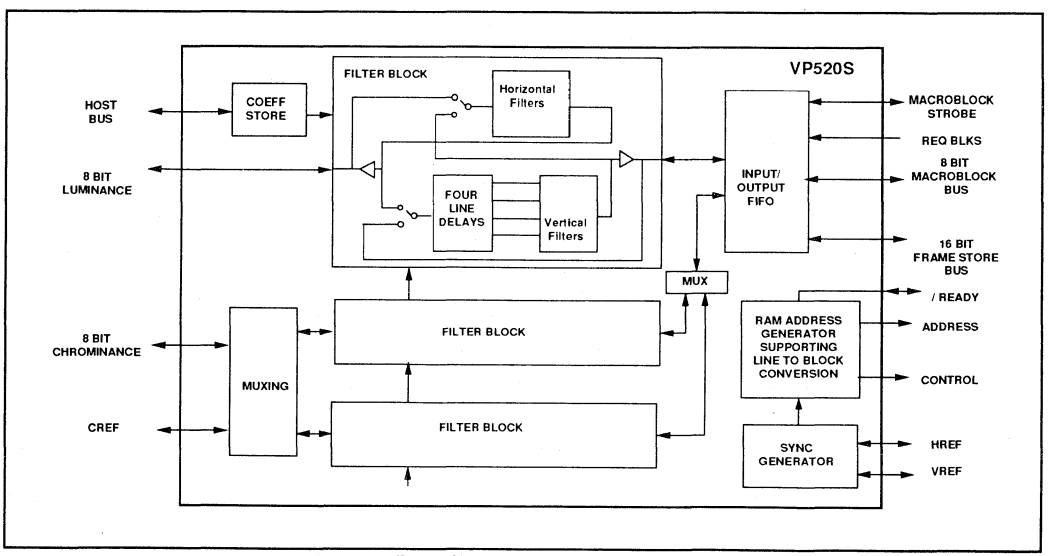


Fig 1 : Simplified Block Diagram

PIN DESCRIPTION

NAME	TYPE	FUNCTION
Y7:0	I/O	Luminance input or output bus
C7:0	I/O	Chrominance input or output bus
M7:0	I/O	Macroblock input or output bus
D15:0	I/O	16 bit data bus for DRAM frame store
A7:0	O	Multiplexed address bus to the DRAM
A8	O	Most sig address bit or second CAS
RAS	O	Row strobe for the DRAM's
CAS	O	Column strobe for the DRAM's
R/W	O	Read/ write signal to the DRAM's
HREF	I/O	Horiz. reference in or horiz. sync out
VREF	I/O	Vertical reference in or vertical sync out
CREF	I/O	CREF in or CREF out
FREF	I/O	Field Indicator in or out
HBLNK	O	Horizontal Blanking output
CSYNC	O	Composite sync output in free run mode
CLMP	O	Defines a black level clamping period for A/D converters
VRST		Frame start identifier. If FRST is low then a low going edge will reset the internal sync generator.
FRST		Field identifier
REQYUV	I	Request macroblocks from encoder
MCLK	I/O	Macroblock I/O strobe
FSIG	I/O	Frame start/ ready signal
SCLK	I	System Clock. 27MHz in PAL/NTSC systems
HD7:0	I/O	Host data bus
HA3:0	I	Host controller address bits
RD	I	An active low host read strobe
WR	I	An active low host write strobe
CEN	I	An active low enable for the strobes
RST	I	Power on reset
TDI	I	JTAG I/P data
TDO	O	JTAG O/P data
TMS	I	Test mode select
TCK	I	JTAG clock
TRST	I	JTAG reset
TOE	I	When high all O/P's are high impedance

NOTE:
"Barred" active low signals do not appear with a bar in the main body of the text.

VIDEO COMPRESS MODE (DECIMATE)

This mode is used when CCIR601 video is to be converted to CIF or QCIF spatial resolution prior to compression. Incoming luminance and chrominance data does not need any prior buffering, but must meet the timing requirements given in Figure 2. A bit in Control register 1 allows the Cb component to precede the Cr component if necessary. This data is passed through vertical and horizontal decimating filters before it is stored in an external frame store. When a complete field has been decimated it is read out in macroblock format and transferred to the next system component.

In this mode HREF, VREF, and FREF are normally inputs which are used to reference active video with respect to video synchronization pulses. The active going edges are used internally, and these must meet the set up time with respect to the system clock as given in Figure 2. Stable inputs are needed with no jitter due to asynchronous pixel clocks, but when this is not possible an external FIFO can be used plus two extra signals as described later. The reference inputs need only stay active for one system clock period. Note that the active going edges for HREF and VREF can individually be defined to be high going or low going, through two bits in Control Register 0. Also note that CREF is always an input and is used as a qualifier for SCLK. The actual edges of CREF are not used.

The internal sync generator can still be used in this mode, if there is a need to supply sync to the video source. The HREF and VREF pins are then used to output HSYNC and VSYNC. Composite sync is supplied on the CSYNC pin.

In addition the CLMP pin provides a pulse [13 SCLK's wide] which can be used to DC restore the black level in an A/D converter. It is active high during the back porch.

The horizontal blanking output (HBLANK) defines when the device expects the first pixel in a line to be supplied, and is derived from the user supplied HREF input. The delay between HREF and HBLANK is user definable in multiples of CREF periods. If the defined value is zero then the HREF input must be horizontal blanking with the minimum set time specified. The HBLANK output is then not defined.

All data changes are referenced to the system clock. The edge actually used is indicated by the CREF input signal, which has a period of double the clock period. The VP520S will strobe in data on the rising edge of the system clock which occurs whilst CREF is high.

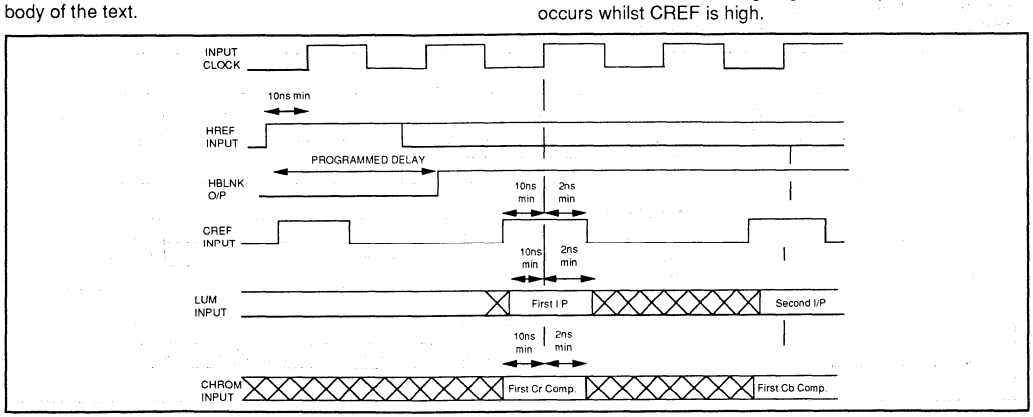


Fig 2 : Luminance and chrominance inputs in the decimate mode.

The first video line to be filtered and stored will be derived from the vertical reference input (VREF). The user can choose the number of transitions of the HREF input which must occur, after VREF has gone active, before starting the filter operation. Data is then not written to the DRAM until after the pipeline delay through the filters.

The VP520S only expects to use one field of CCIR601 video, which can be selected by the FREF input or internal logic. A bit in Control Register 1 (Internal / External Field Detect) determines which option is to be used. An additional Field Select Bit determines whether the field selected should correspond to FREF being high or low. When the Field Select Bit and the input are at the same logical level then that field is used. Note that FREF transitions must be coincident with active going VREF transitions.

Internal logic is provided which determines the field (Field 1) in which VREF goes active in less than half a line period after the HREF input last went active.The half line period is determined by VREF going active between 1 and 432 CREF qualified SCLK edges after HREF went active (1-429 in NTSC mode). Note that coincident VREF and HREF edges will indicate this field on the first CREF qualified SCLK edge.

This logic is used, rather than the FREF input, when the Internal / External Field Detect Bit is low. Field 1 is selected when the Field Select in Control register 1 is low, and Field 2 is used when the bit is high.

In the Split Screen mode this logic is overridden, and both fields are actually used. External logic is assumed to switch between two sources of video, one for each field. The internal DRAM address generator is modified such that half area pictures from the centre of each source are actually stored as CIF/QCIF data. The first line used in each field will be 72 line delays in addition to the number which has been defined by the user. The split screen option is not supported in the QCIF mode of operation, and a reset is needed after a mode change in CIF.

The VP520S will insert zero's into the line delays during vertical blanking. This ensures that all the filter accumulators are cleared and the edges of the picture are correctly processed. The horizontal filters always give the required results since four decimated values are ignored at either side of the picture.

Incoming luminance data could have a black level of 16, which will be shifted if the filter coefficients are not chosen to exactly give a gain of unity. A Control Bit is thus provided, which when set causes 16 to be subtracted from incoming luminance. A black level of zero will then stay as zero throughout the filter operation. At the output of the filters 16 is always added to the results, regardless of the state of the Control Bit. Saturation logic ensures that these addition / subtraction operations do not produce negative results or values greater than 254.

A Control Bit is also provided which selects between colour difference inputs and true Cr Cb chrominance values. Cr Cb values are 8 bit positive only numbers, with black levels of 128. These must be converted to two's complement signed numbers by subtracting 128, thus giving a black level of zero through the filters. The outputs of the filters are always converted to positive only Cr Cb values by adding 128 to the results, regardless of the state of the Control Bit.

COPING WITH SYNC JITTER

When input syncs to the VP520S have jitter, due to the use of a composite video decoder which does not produce a line locked clock, it is necessary to use an external FIFO line buffer. For this reason the VP520S supports a system in which external line buffer writes are controlled by the video source and line reads are controlled by the VP520S. The VP520S in the decode loop is assumed to be supplying sync to the VP520S in the encode loop, but the sync generator must be reset at the start of a frame to be in step with the video source. Two pins have been supplied to support this situation, namely: VRST - pin 34, and FRST - pin 36. The falling edge of VRST (frame start identifier) when FRST (field identifier) is low identifies the start of the frame. These two inputs can typically be supplied by the Brooktree Bt812 Composite Video Decoder. Note that Host Address 3 must be programmed with the value 02 Hex to enable the reset operation.

CIF/QCIF MACROBLOCK OUTPUTS

When producing decimated CIF/QCIF data in macroblock format, the device raises a flag when a frame of data is ready for reading from the frame store (FSIG). The FSIG pin is automatically configured as an output in the decimate mode, but will only stay active (high) for the time given in Figure 3. If a Request Macroblock response (REQYUV) is not obtained during this period, then FSIG will be taken low and the frame of data presently available will be ignored. It will go high again when a new frame of data is available.

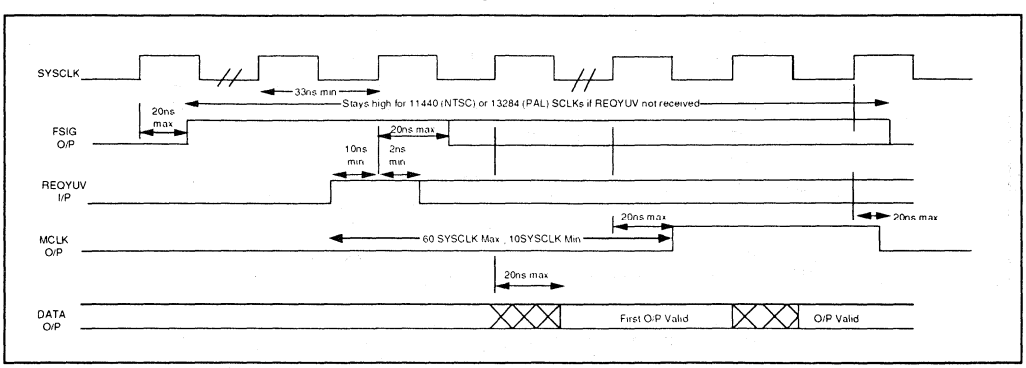


Fig 3 : Macroblock Output Timing

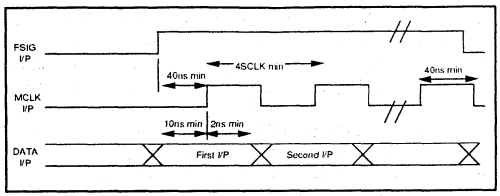


Fig 4 : Macroblock Input Timing

When it receives a REQYUV response from the next system component, it starts to output a macroblock by using an output strobe derived by dividing down the clock input. Detailed timing is given in Figure 3. This strobe only occurs when data is available at the output pins and at a rate of SYSCLK/4. The 'Request Macroblock' flag must go inactive and then active again before a further macroblock is made available.

The Frame Ready flag is only available on the output pin if the Frame Enable Bit is set in Control Register 1. Through this control bit a host controller is able to determine whether a new frame is to be compressed and transmitted. In an alternative arrangement the control bit can be permanently set, and the Frame Ready Flag is then used as an interrupt to the host controller. It then generates a signal which is used as the Frame Ready signal for the next device.

The following sections describe this interface as it applies to the VP2611 H261 Video Encoder.

TRANSFERING MACROBLOCKS TO THE VP2611

When the VP520S has stored a complete field of decimated video in the DRAM, it raises a Frame Ready Flag (FSIG). If the bit in Control Register 1 does not inhibit the output, this flag becomes the FRMIN input on the VP2611. This responds to the FRMIN input by generating a Request for Macroblock Data (REQYUV). The VP2611 MUST then receive a complete macroblock (384 bytes) within 1870 cycles of the system clock. When the VP520S is producing decimated CIF/QCIF data, writing line data to the DRAM has priority, and only four macroblock read operations are possible in every 32 clock cycles i.e. one read takes eight cycles. These, however, are 16 bit word operations and it thus requires 384 x 8/2 = 1536 cycles to output the data. In addition there is a maximum delay of 60 clock periods from receiving REQYUV to producing the first output strobe (MCLK). This is still well within the time available.

The four 16 bit words are stored in the VP520S and transmitted to the VP2611 as eight bytes using a strobe (MCLK) derived from the system clock. This is only present when valid data is available, and it drives the PCLK input on the VP2611.

It takes the VP2611 almost exactly all the available time at 30 Hz frame rates to process all the macroblocks. After a field time (half an interlaced frame) the VP520S will start to write new data to the DRAM, and data could be overwritten during the last macroblocks. Since there is available space in the DRAM, a small address offset is used between video fields to avoid this problem.

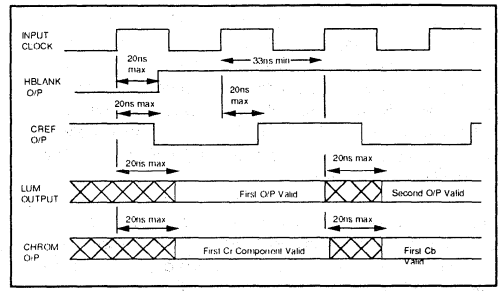


Fig 5 : Luminance and Chrominance Output Timing

INTERPOLATE MODE

In this mode the VP520S expects to receive CIF/QCIF data in macroblock format, which it then writes to an external frame store. This is then read back in line format and passed through vertical and horizontal interpolating filters to produce two fields of CCIR601 video. Detailed input timing is given in Figure 4.

FSIG automatically becomes an input which is used to identify the start of a frame and to reset the internal address counter. FSIG must stay high until a complete CIF/QCIF frame has been received (internal logic counts macroblocks). If FSIG goes low early then the complete frame will be ignored, and the previously received frame will continue to be displayed.

An input strobe, derived by dividing the system clock by four, must also be provided in order to input data. This must only be present when valid data is available on the input pins. Incoming macroblocks are byte wide, and these are internally buffered to allow four 16 bit words to be written to the DRAM every 32 system clock cycles. This is equivalent to a byte input rate of SCLK/4 which must not be exceeded.

The CIF frame store is double buffered such that a new frame can be received whilst the previous one is being displayed. In fact the use of 256K x 16 DRAM's gives sufficient capacity for more than three complete CIF frames, and the internal address generator will simply roll around to make full use of the available space.

Once a complete CIF/QCIF frame has been received, it will normally be used to generate two interlaced PAL or NTSC fields. These fields continue to be re-generated until a complete new CIF frame has been received. The rate of receiving frames depends on the transmission bandwidth, but the maximum rate is 30 Hz. The changeover to the newly received frame will occur when the VP520S has finished generating any one of the pair of interlaced fields for display, it does not

SYMBOL	PARAMETER	MINIMUM	MAXIMUM
t RAC	Access time from RAS	-	105ns or under
t CAC	Access time from CAS		25ns or under
t RP	RAS precharge time	50ns or under	-
t CP	CAS precharge time	12ns or under	-
t RAS	RAS pulse width	80ns or under	-
t CAS	CAS pulse width	50ns or under	-
t REF	Time between complete refreshes	-	4 ms or over (8 ms with 256k x n)

N.B. All times are quoted assuming 27MHz operation. For lower clock frequencies increase the above values proportionately.

Table 1. External DRAM Timing Requirements

necessarily have to have generated two interlaced fields from the received frame. If the VP520S is receiving frames at the full CIF 30 Hz frame rate but only displaying PAL frames at 25 Hz, then periodically one of the PAL frames (comprising two interlaced fields at 50 Hz) will be generated from two received CIF/QCIF frames. An incoming CIF/QCIF frame will always be used since the interlaced field rate is always greater than 30 Hz in either PAL or NTSC.

The data is read from the frame store such that interpolated data becomes available after programmed delays referenced to the VREF and HREF signals. Six bits are available to define the line delay, and ten are provided to define the delay from HREF in CREF periods. The actual delays are greater than the programmed values because of the internal pipeline delays, which are also mode dependent.

HREF and VREF can either be user supplied inputs, or are generated internally from a PAL/NTSC timing generator. A bit in Control Register 0 determines this option, and when the internal generator is specified the HREF pin becomes an output which supplies horizontal sync and the VREF pin supplies vertical sync. A composite sync output is also provided for system level use. In this mode the VREF and HREF signals used internally are effectively vertical and horizontal sync, and the programmed delays should be chosen to reflect this condition.

The signals provided from the internal timing generator allow the VP520S to drive the VP510 Colour Space Converter and an RGB monitor. Detailed output timing is given in Figure 5. Note that the chrominance order can be changed. Alternatively they can be used to drive off the shelf composite video encoders.

External chrominance data can have a zero colour difference value of either 0 or 128. This is defined using the Chrominance Control Bit. Where 128 is the zero colour difference value, 128 will be subtracted from incoming chrominance data and 128 will be added to output chrominace data. Output values will be limited to lie in the range 16 to 240.

External luminace data can have a black luminace level of either 0 or 16. This is defined using the Luminace Control Bit. Where 16 is the black value, 16 will be subtracted from incoming luminace data and 16 will be added to output luminace data. Output values will be limited to lie in the range 16 to 235.

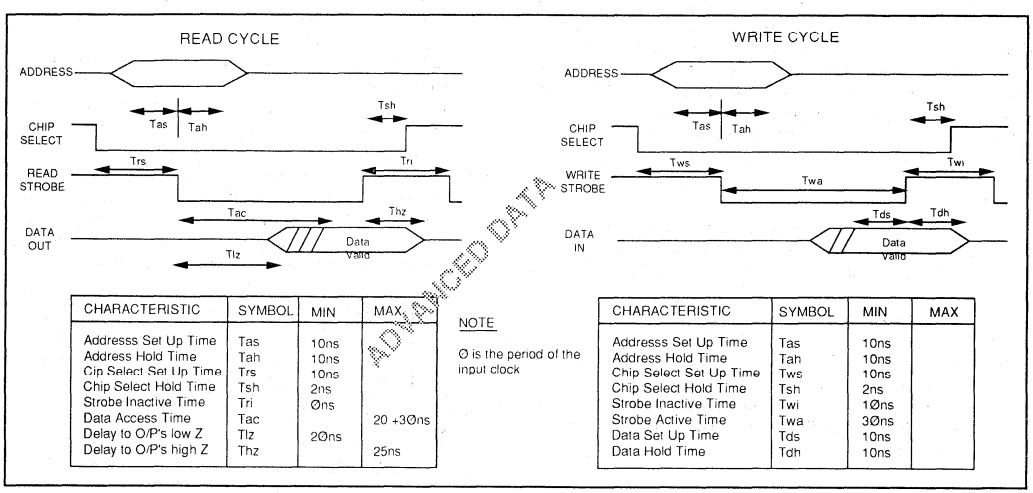
The data stored in the CIF frame store will not contain the black levels normally present during horizontal and vertical flyback. This is inserted by the VP520S at the appropriate times in order to ensure that the correct filter operation occurs at the edges of the picture. In addition to these black levels during flyback, a bit in Control Register 1 allows all active video to be replaced by a fixed colour. This colour is user definable through YUV values in three registers.

FRAME STORE INTERFACE

All read and write operations to the external DRAM frame stores are based on the use of fast page mode with 13.5 MHz CAS cycles. Internally a 54 MHz clock is produced from the 27MHz System clock, and this determines the minimum time interval which can be used in the generation of pulses and defining precharge times. Any DRAM used must meet the timing constraints given in Table 1.

Reading and writing rates dictate the need for a 16 bit data interface, and line data is re-organized to allow a 16 bit word to consist of either two luminance values or two chrominance values. This gives compatibility with the macroblock requirements since a sub block is either all chrominance or all luminance data. Reading or writing macroblock data requires jumps between pages, but four words can always be read or written using fast page mode.

Read and write operations must be timeshared to meet the requirements of the system. This time-sharing is based on the use of 16 cycles of the 13.5 MHz clock. When reading or writing line data to the store, 10 cycles are used for eight words, and six cycles are left free for four exchanges with the encoder or decoder. The additional cycles are needed when



CHARACTERISTIC	SYMBOL	MIN	MAX
Addresss Set Up Time	Tas	10ns	
Address Hold Time	Tah	10ns	
Cip Select Set Up Time	Trs	10ns	
Chip Select Hold Time	Tsh	2ns	
Strobe Inactive Time	Tri	Øns	
Data Access Time	Tac		20 +3Øns
Delay to O/P's low Z	Tlz	2Øns	
Delay to O/P's high Z	Thz		25ns

NOTE

Ø is the period of the input clock

CHARACTERISTIC	SYMBOL	MIN	MAX
Addresss Set Up Time	Tas	10ns	
Address Hold Time	Tah	10ns	
Chip Select Set Up Time	Tws	10ns	
Chip Select Hold Time	Tsh	2ns	
Strobe Inactive Time	Twi	1Øns	
Strobe Active Time	Twa	3Øns	
Data Set Up Time	Tds	10ns	
Data Hold Time	Tdh	10ns	

Fig 6 : Host Interface Timing

using fast page mode in order to guarantee RAS precharge times and RAS to CAS delays.

The above time partitioning gives a line rate of 6.75 MHz, which meets real time CIF requirements. The exchange rate with the encoder or decoder is only half of this, but is adequate for CIF data at 30 Hz frame rates. In the decode mode the VP520S produces two fields at 60 Hz rates from every 30 Hz received frame, thus writing need only be half the rate of reading. In the decimate mode the VP520S produces a CIF frame using line rates which could have supported two 60Hz fields, but only one is used. Thus reading rates need only be half writing rates since the spare field time is available.

In the interpolate mode two complete CIF frame stores are required, which dictates the use of 256K word DRAM's. The A8 pin then provides the ninth address bit needed for such devices. In the decimate mode only one CIF frame store is required, and a Control Register Bit allows the user to select either 256K word DRAM's, or 64K x 16 devices. In the latter case two such devices are needed, and the A8 pin now supplies a second CAS strobe to enable the second device. Refresh cycles generate CAS before RAS sequences.

HOST INTERFACE

The VP520S employs a conventional memory mapped host interface using a data bus and an address bus. To minimize on pin count the VP520S only uses four address lines, and all internal RAM is addressed through counters. All data is validated with a read or write strobe, and an active low enabling signal. These strobes can be asynchronous to the 27 MHz clock, but the latter must be present to move the data through several pipeline delays. Strobes must thus be valid for several clock periods. Timing is shown in Figure 5.

In the worst case mode (QCIF to NTSC video), the device must store 40 horizontal coefficients and 210 vertical coefficients. Internal storage must thus be provided for a total of 250 eight bit coefficients, and this is split into four blocks. These consist of storage for 24 horizontal luminance coefficients; storage for 16 horizontal chrominance coefficients; storage for 70 vertical luminance coefficients; and finally 140 vertical chrominance coefficients. Each block of RAM has its own internal address counter, and all counters are simultaneously reset with a write to address F hex. Each RAM area has an associated address as listed below, and a read or write using that address will increment the relevant counter. Attempts to use more addresses than are applicable to a particular area will cause undefined behaviour.

Address allocations are given below;

Addr	Function
0	Reserved
1	R/W horizontal luminance coefficients. Max 24
2	R/W horizontal chrominance coefficients. Max 16.
3	Normally 00 Hex. When 02 Hex the sync generator can be reset with the FRST and VRST pins.
4	Reserved for internal use
5	R/W vertical luminance coefficients. Max 70.
6	R/W vertical chrominance coefficients. Max 140.
7	Set to the normal operating value of 01 Hex by RESET. When loaded with 21 Hex an encoding plus a decoding VP520S can be connected 'back to back' for test purposes or coefficient investigations. No other values must be used.
8	Control Register 0. See below.
9	Control Register 1. See below
A	Line delay from VREF to first active line. 6MSBs only
A/B	Pixel delay from HREF to first active pixel 2 Bits from A plus 8 from B to give a 10 Bit value. Bit A1 is the MSB
C	Blanked screen Y value
D	Blanked screen U value
E	Blanked screen V value
F	Clear all address counters

The bits in control registers 0 and 1 are used individually, and are defined below. Where necessary the action caused when changing a control bit is delayed until the start of a new field.

REGISTER 0 (Address 8)

BIT	FUNCTION
0	Interpolate if high, decimate if low
1	PAL if low, NTSC if high
2	QCIF if high, CIF if low
3	If low subtract 16 from Y, add 16 back after filtering
4	If low subtract 128 from chrominance I/Ps, add 128 to O/Ps
5	If low generate sync, if high lock to HREF and VREF
6	If low then active edge of VREF is low going.
7	If low then active edge of HREF is low going.

REGISTER 1 (Address 9)

BIT	FUNCTION
0	If low then U inputs precede V inputs and outputs
1	If low use the internal field detect logic
2	Field Select. See text.
3	If low use 64Kx16 DRAM (encoder only)
4	When high specifies Split Screen mode (encoder only)
5	When low the Frame Ready Flag is enabled
6	When high the screen is blanked (colour defined in addresses C, D, E)
7	When high DRAM writes are disabled

USE OF ADDRESS 7

By loading Hex 21 into host address 7 it is possible to connect the encoding and decoding filters into a back to back configuration. This is useful for test purposes or for evaluating the filter coefficient values, and it avoids the need for a 'Frame Start' signal into the filter in the decode path. In normal operation address 7 should contain 01 which is the default after a reset operation.

LOADING COEFFICIENTS

The following tables show the coefficient storage locations for different modes. The filter sections below describe the use of coefficient sets. Within a set, coefficients are stored in ascending order, ie. C0, C1, C2 etc. Note that some locations are shown as not used. However, since each store is loaded sequentially, the data stream used to load the coefficient stores must contain padding values corresponding to the unused addresses. Note also that only the address range shown in the tables have to be loaded with data.

A: Horizontal Luminance Store

This is a 24 byte RAM and coefficients will be stored as follows. The full sequence is obtained by writing to Address 1, twenty four times and supplying the required data.

Mode	Addresses	Coefficient Set
CCIR -> CIF	0-7	1
CCIR -> QCIF	0-15	1
CIF -> CCIR	0-5	1
	6-11	2
QCIF -> CCIR	0-5	1
	6-11	2
	12-17	3
	18-23	4

B: Horizontal Chrominance Store

This is a 16 byte RAM and coefficients will be stored as follows, by writing to Address 2 the required number of times.

Mode	Addresses	Coefficient Set
CCIR -> CIF	0-7	1
CCIR -> QCIF	0-15	1
CIF -> CCIR	0-3	1
	4-7	2
QCIF -> CCIR	0-3	1
	4-7	2
	8-11	3
	12-15	4

C: Vertical Luminance Store

This is a 70 byte RAM and coefficients will be stored by writing to Address 5 the required number of times.

Mode	Addresses	Coefficient Set
625 line -> CIF	0-4	1
525 line -> CIF	0-4	1
	5-9	2
	10-14	3
	15-19	4
	20-24	5
	25-29	6
625 -> QCIF	0-6	1
525 -> QCIF	0-6	1
	7-13	2
	14-20	3
	21-27	4
	28-34	5
	35-41	6
CIF -> 625 line	0-4	1, even field
	5-9	1, odd field
CIF -> 525 line	0-4	1, even field
	5-9	2, even field
	10-14	3, even field
	15-19	4, even field
	20-24	5, even field
	25-29	not used
	30-34	1, odd field
	35-39	not used
	40-44	2, odd field
	45-49	3, odd field
	50-54	4, odd field
	55-59	5, odd field
QCIF -> 625 line	0-6	1, even field
	7-13	2, even field
	14-20	1, odd field
	21-27	2, odd field
OCIF -> 525 line	0-6	1, even field
	7-13	2, even field
	14-20	3, even field
	21-27	4, even field
	28-34	5, even field
	35-41	1, odd field
	42-48	2, odd field
	49-55	3, odd field
	56-62	4, odd field
	63-69	5, odd field

D: Vertical Chrominance Store

This is a 140 byte RAM and coefficients will be stored by writing to Address 6 the required number of times.

Mode	Addresses	Coefficient Set
625 line -> CIF	0-4	1
525 line -> CIF	0-4	1
	5-9	2
	10-14	3
625 line -> QCIF	0-6	1
525 line -> QCIF	0-6	1
	7-13	2
	14-20	3
CIF -> 625 line	0-4	1, even field
	5-9	2, even field
	10-14	1, odd field
	15-19	2, odd field
CIF -> 525 line	0-4	1, even field
	5-9	2, even field
	10-14	3, even field
	15-19	4, even field
	20-24	5, even field
	25-29	not used
	30-34	1, odd used
	35-39	not used
	40-44	2, odd field
	45-49	3, odd field
	50-54	4, odd field
	55-59	5, odd field
QCIF -> 525 line	0-6	1, even field
	7-13	2, even field
	14-20	3, even field
	21-27	4, even field
	28-34	5, even field
	35-41	6, even field
	42-48	7, even field
	49-55	8, even field
	56-62	9, even field
	63-69	10, even field
	70-76	1, odd field
	77-83	2, odd field
	84-90	3, odd field
	91-97	4, odd field
	98-104	5, odd field
	105-111	6, odd field

	112-118	7, odd field
	119-125	8, odd field
	126-132	9, odd field
	133-139	10, odd field
QCIF -> 625 line	0-6	1, even field
	7-13	2, even field
	14-20	3, even field
	21-27	4, even field
	28-34	1, odd field
	35-41	2, odd field
	42-48	3, odd field
	49-55	4, odd field

HORIZONTAL FILTERS

Chrominance data is assumed to have already been decimated down to half the horizontal sampling rate of the luminance data, before it is applied to the VP520S. When producing CIF data both luminance and chrominance are then both decimated by two, when producing QCIF data they are both decimated by four.

Simulations with actual video have shown that 8 tap CIF filters and 16 tap QCIF filters give more than adequate performance in the decimation mode. In the interpolation mode these same simulations have shown the need for longer filters in the luminance channel. The hardware thus supports a 12 tap filter when interpolating luminance from CIF inputs, but only 8 taps are provided for each chrominance channel. Even longer filters are needed when QCIF data must be interpolated, and the luminance channel is provided with 24 taps, and each chrominance channel with 16 taps.

Note that when interpolating by two the output rate is double the input rate, but every other input will be conceptually zero. Similarly when interpolating by four there are three zero's between every data point, even though the output rate is four times the input rate. Thus during any clock period only one half or one quarter of the coefficients are actually in use, and the computational burden is no greater than when doing the equivalent decimation.

Since all the coefficients are not in use during any clock cycle, it is convenient to refer to two smaller sets of coefficients. Thus the 12 tap CIF luminance filter, for example, can be considered to have two sets of 6 coefficients, and the 24 tap QCIF luminance filter to have four sets of 6 coefficients. The addressing in the coefficient RAMs uses this concept of sets.

VERTICAL FILTERS

The vertical filters are designed to produce CIF with the spatial relationship shown in Figure 7, and QCIF with the spatial relationship shown in Figure 8. Original PAL or NTSC video contains lines of coincident luminance and chrominance, but the CIF specification requires that the decimated chrominance information is shifted such that it lies mid way between two luminance lines. This is achieved by choosing the centre outputs from the filter which best fit the requirements. The filter outputs actually used by the device are shown by the arrows in Figures 7 and 8, and are optimal when the even field provides the original video.

It is assumed that one of the interlaced fields has been discarded prior to the VP520S, and thus no further decimation occurs when producing CIF luminance from PAL (NTSC in

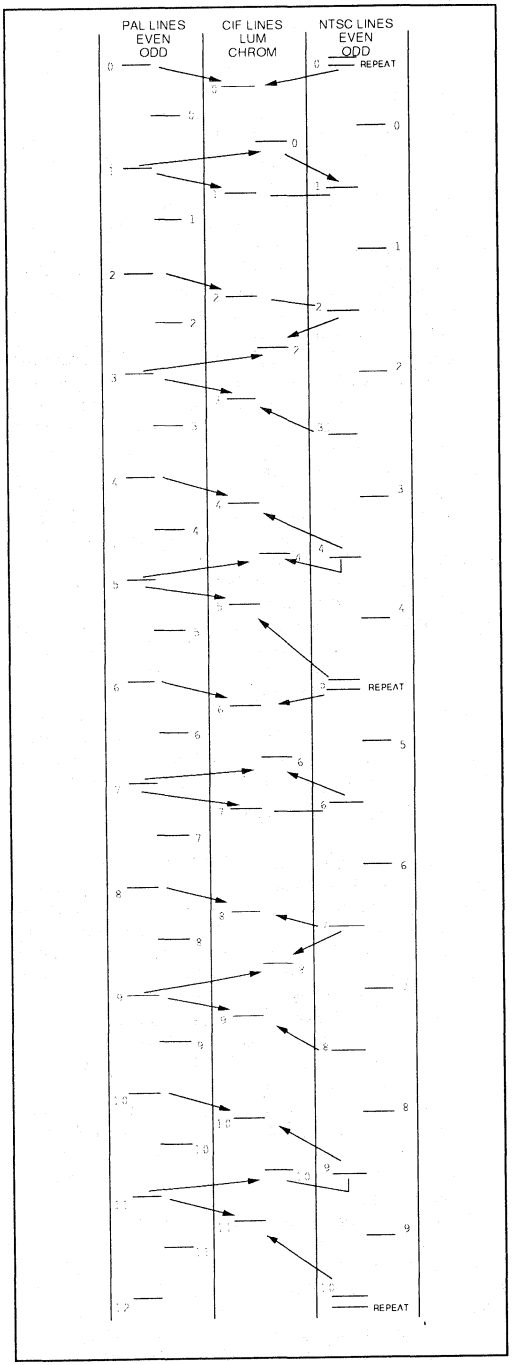


Fig 7 : CIF Spatial Relationships

fact needs some interpolation - see the relevant section). Chrominance, however, is decimated by two. When producing QCIF data the luminance channel is decimated by two, and the chrominance by four.

When the VP520S is used to derive interlaced CCIR601 video, the internal address generator will read the CIF/QCIF frame store twice in order to produce the two fields. Each field has its own set of coefficients.

Internal RAM is provided which will support four CIF line delays for both chrominance and luminance. Five tap filters are thus possible for CIF conversions. With a QCIF system the internal RAM could theoretically be used to provide eight QCIF line delays. In practice, however, little benefit is obtained by using vertical filters with more than seven taps, and thus only six line delays are used.

Polyphase filters are used to support the spatial conversions. PAL conversion is relatively simple and only requires a set of coefficients for each mode. NTSC conversion requires several sets of coefficients since the 240 lines in a field must be converted to 288 lines of CIF. One line is repeated in every five to produce six lines which are then filtered with their own coefficients.

The generation of interpolated outputs requires CIF / QCIF data to be repeatedly read from the frame store at various line intervals. This is all handled by the internal address generator, and is transparent to the user. The device then produces coincident luminance and chrominance data which has been interpolated from data in the frame store. The first line will be produced to match the delay from the VREF input which has been pre-defined. This delay must be greater than the internal pipeline delay, which itself is mode dependent (delay yet to be determined).

The device introduces black lines at the top and bottom of the fields. Thus the first and last lines in the interpolated field will be filtered with varying amounts of black information.

PAL VERTICAL FILTERING

When producing CIF data the five tap filters provide outputs for every line at the 6.75 MHz decimated line rate. Every filtered luminance line is used but every other filtered chrominance line will be discarded. Filter outputs corresponding to odd numbered PAL chrominance lines in any field being at the centre are used to provide the CIF chrominance lines. This is shown by the arrows in Figure 7.

When decimating down to QCIF seven tap filters are used, which provide outputs for every line at the 3.375 MHz line rate. Only every other filtered luminance line, and every fourth chrominance line are actually stored in the frame store. Different PAL lines are used to produce the offset luminance and chrominance lines as indicated by the arrows in Figure 7.

When interpolating from CIF the luminance channel conceptually uses a 10 tap filter, with every other input line containing only zero's. Thus only five coefficients are actually used when producing interpolated lines for the even field, and five different coefficients are used when producing the odd field. The device thus stores two sets of five coefficients; one set for each field produced by reading the CIF frame store twice.

The chrominance filter is conceptually a 20 tap filter with three lines of zero's for every actual input. Thus each chrominance channel needs four sets of five coefficients; two sets are needed to produce one field, and two sets are needed for the other field. The same chrominance data is read twice for a given pair of luminance lines, in order to provide inputs for the filter. Thus the internal line delays contain the same set of chrominance data on two consecutive lines supplying data to the filters.

When interpolating from QCIF, seven coefficients can be

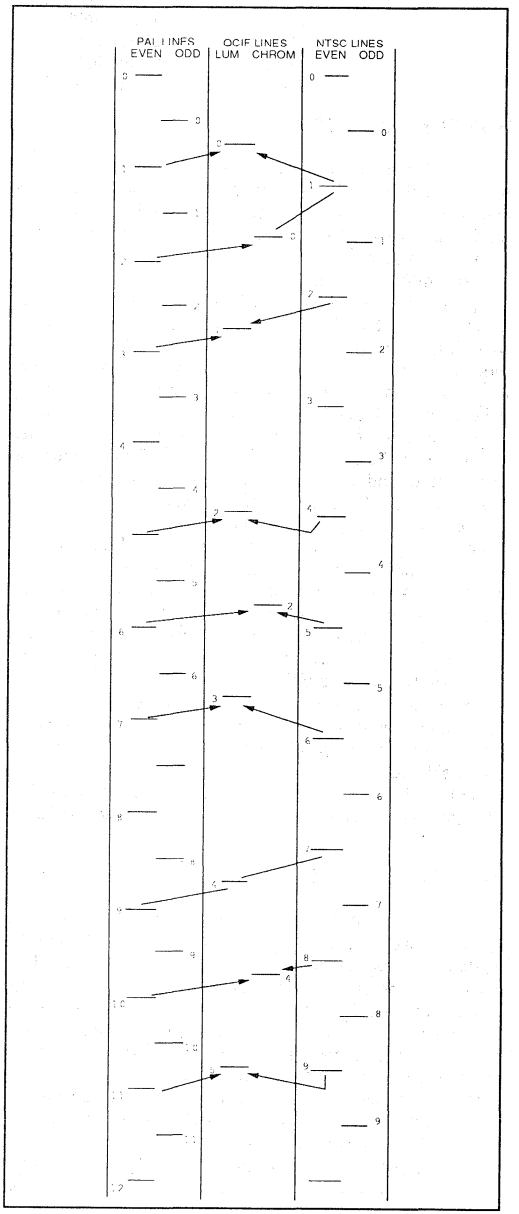


Fig 8 : QCIF Spatial Relationships

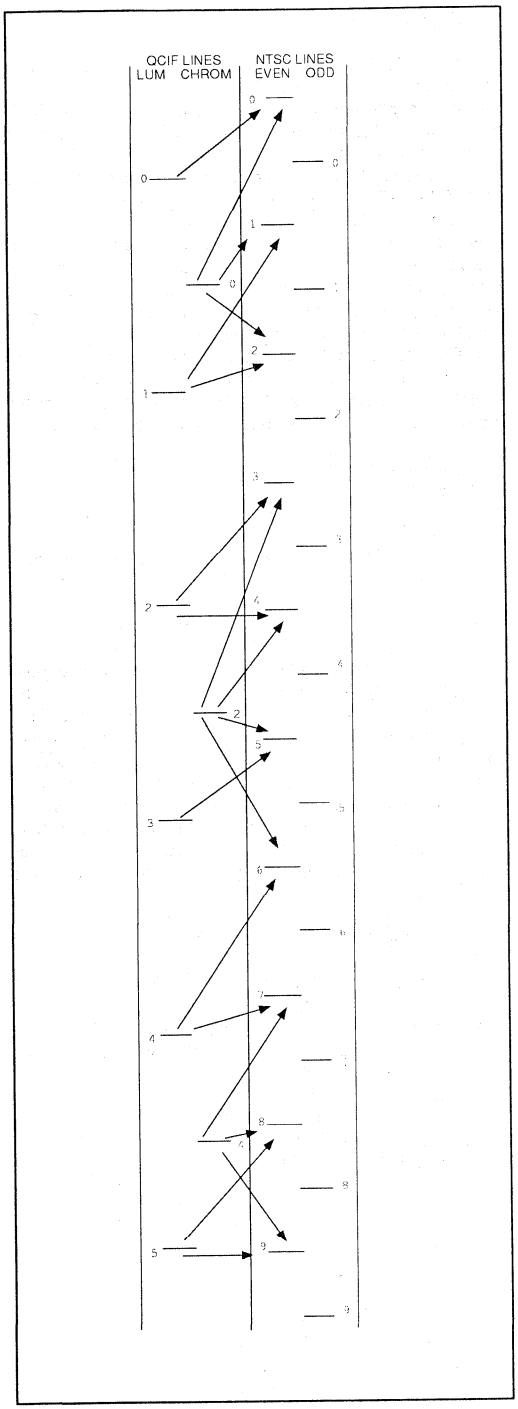


Fig 9 : Interpolating from QCIF to NTSC

used in each set since six line delays are provided. The luminance filter conceptually contains 28 taps (four sets of seven coefficients with two sets used to produce each field). Similarly the chrominance filter consists of 56 taps arranged as eight sets of seven coefficients with four sets needed for each field. In order to provide data for the filters each luminance line is read twice, and each chrominance line is read four times to produce each field.

NTSC VERTICAL FILTERING

One field of NTSC video consists of 240 chrominance and luminance lines, which must be converted to 288 lines of CIF luminance and 144 lines of CIF chrominance. The luminance increase is mechanized by repeating the first line in every five to produce six lines, which are then applied to the vertical filters. A different set of coefficients is used for each line, requiring a total of 30 to be stored within the device. The line repeat causes one set of line data to be used twice, but each time different coefficients are used by the filter. This technique is equivalent to interpolating the data by six, and then decimating by five. The required coefficients for each of the six sets can be derived by conceptually using this approach.

The line repeat requires an additional FIFO line delay before the four delays used by the filters. By reducing the horizontal blanking time it is possible to read six lines (one is repeated) from the FIFO in the time taken to acquire five lines of video with blanking.

Chrominance data also passes through the input FIFO and one line in every five is repeated. This is done in order to avoid differential delays with the luminance data. Three chrominance lines are only needed, however, for every five original lines. They are produced by using three sets of five coefficients and discarding two filtered lines in every five. The three selected filter outputs are chosen such that the centre line of the filter is closest to the CIF line number needed. The centre lines which are actually used are shown in Figure 8, and result in a sequence of two chosen outputs then a gap followed by one output then a gap. Simply using every other output would not give the best fit.

A simplified approach is used when decimating down to QCIF resolution, and the input FIFO is not used. Six luminance lines are derived from ten NTSC lines by choosing the six outputs produced when the centre line in the filter is closest to the QCIF line that is needed. Overall this results in a luminance sequence consisting of two outputs then a gap, followed by one output then a gap and is shown in Figure 8.

Three chrominance lines are derived from the same inputs by using three sets of seven coefficients. The chrominance sequence is also shown in Figure 7, and consists of an output then three gaps, followed by an output and two gaps.

When interpolating from CIF up to NTSC resolutions, it is necessary to read lines of data from the CIF frame store with reduced blanking periods. The timing is calculated such that six lines are read in the time that five lines would have been read if they had the correct blanking period. These fast lines are continuously filtered using all the available information, and the results are written to an output FIFO. This FIFO is then read with the correct blanking period inserted in order to provide NTSC data at the output pins. Thus five lines are read out in the time taken to load six lines (one of which need not actually be written since it is never used)

Five sets of coefficients are used to produce the five lines which are actually stored, but the coefficients are different for the even and odd field generation. Thus a total of ten sets of five coefficients are internally stored. In effect we have interpolated by five and then decimated by three in order to produce the complete NTSC frame.

Each CIF chrominance line is used to produce two filtered NTSC chrominance lines, and one filtered line in every six is then ignored. This is mechanized by reading each CIF chrominance line twice for every pair of luminance lines. The same filtering and discard technique as used in the luminance channel is then applied, using five sets of coefficients for each field. Ten sets are thus needed to produce two NTSC fields. We have effectively interpolated by ten and then decimated by three to produce 480 chrominance lines for the complete frame.

When interpolating from QCIF to NTSC the additional output buffering is not used. Instead a sequence is used which will generate 10 NTSC lines in any field from six QCIF luminance lines and three chrominance lines. Figure 9 illustrates how the first and fourth lines are used once and the second, third, fifth, and sixth used twice to produce QCIF luminance. Since this 1 - 2 - 2 sequence is used twice in every ten lines, only five rather than ten sets of coefficients are actually needed for each field (ten sets in total).

The first and third chrominance lines are used three times, and the second line is used four times. Thus ten sets of coefficients are needed for each field (twenty sets in total). Each luminance and chrominance set consists of seven coefficients, since six line delays are provided for the filters.

JTAG Test Interface

The VP520S includes a test interface consisting of a boundary scan loop of test registers placed between the pads and the core of the chip. The control of this loop is fully JTAG/ IEEE 1149-1 1990 compatible. Please refer to this document for a full description of the standard.

The interface has five dedicated pins: TMS, TDI, TDO, TCK and TRST. The TRST pin is an independent reset for the interface controller and should be pulsed low, soon after power up; if the JTAG interface is not to be used it can be tied low permanently. The TDI pin is the input for shifting in serial instruction and test data; TDO the output for test data. The TCK pin is the independent clock for the test interface and registers, and TMS the mode select signal.

TDI and TMS are clocked in on the rising edge of TCK, and all output transitions on TDO happen on its falling edge.

Instructions are clocked into the 3 bit instruction register (no parity bit) and the following instructions are available.

Instruction Register (MSB first)	Name
111	BYPASS
000	EXTEST (Inversion except for VREF, HREF, CSYNC and CLMP)
010	SAMPLE/PRELOAD

The TAP controller used in this device does not support a separate INTEST instruction but allows EXTEST to drive the internals of the device as well as to drive the output pins. Output enables are thus present in the chain which are not connected to pins but which allow EXTEST to be used to control the impedance of all the outputs. The TOE pin, which can separately be used to control the impedance of all the outputs, can be monitored as an input through the scan chain but cannot be used to control the outputs through the TAP controller. The signals controlled by the various enables are listed below:

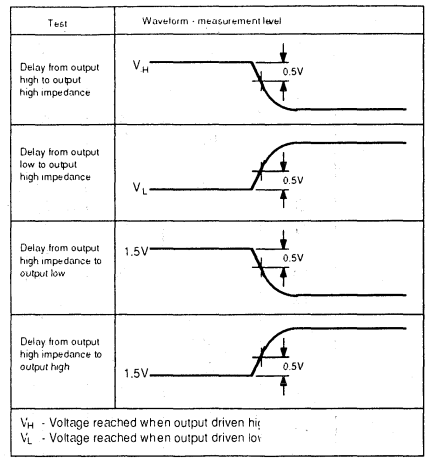
PAD NAME	SIGNALS CONTROLLED
dram_oeb	A8:0, RAS, CAS, R/W
refs_oeb	FREF, VREF, HREF
csync_oeb	CLMP, CSYNC, HBLNK
cgtout_oeb	Test function only
d_oeb	D15:0
m_oeb	M7:0, MCLK, FSIG
c_dec_b	CREF
yuv_oeb	Y7:0, C7:0
cdata_oeb	HD7:0

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage V_{DD}	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to V_{DD} + 0.5V
Output voltage V_{OUT}	-0.5V to V_{DD} + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HMB)	500V
Storage temperature T_S	-65°C to 150°C
Ambient temperature with power applied T_{AMB}	0°C to 70°C
Junction temperature	150°C
Package power dissipation	5000mW

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.



STATIC ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise stated)
Tamb = 0 C to +70°C V_{DD} = 5.0v ± 5%

Characteristic	Symbol	Value Min.	Typ.	Max.	Units	Conditions
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.0		-	V	V_{DD} - 1V for SYSCLK and MCLK
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{DD}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{DD}
Output S/C current	I_{SC}	10		300	mA	

ORDERING INFORMATION

VP520S/CG/GH1R (Commercial - Plastic QFP package)

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	GND	25	M3	49	CREF	73	VDD	97	D14
2	A8	26	M2	50	GND	74	SCLK	98	D13
3	A7	27	M1	51	CSYNC	75	GND	99	D12
4	A6	28	M0	52	Y0	76	VDD	100	GND
5	A5	29	MCLK	53	Y1	77	HA0	101	VDD
6	VDD	30	VDD	54	Y2	78	HA1	102	D11
7	GND	31	GND	55	Y3	79	HA2	103	D10
8	A4	32	REQYUV	56	Y4	80	HA3	104	D9
9	A3	33	GND	57	Y5	81	WR	105	D8
10	A2	34	VRST	58	Y6	82	RD	106	GND
11	A1	35	FSIG	59	Y7	83	CEN	107	VDD
12	A0	36	FRST	60	VDD	84	HD0	108	D0
13	VDD	37	VDD	61	GND	85	HD1	109	D1
14	GND	38	RST	62	HBLNK	86	HD2	110	D2
15	RW	39	TCK	63	C0	87	HD3	111	D3
16	VDD	40	TMS	64	C1	88	HD4	112	GND
17	GND	41	TRST	65	C2	89	HD5	113	VDD
18	RAS	42	TDI	66	C3	90	VDD	114	D4
19	VDD	43	TDO	67	C4	91	GND	115	D5
20	GND	44	TOE	68	C5	92	HD6	116	D6
21	M7	45	VDD	69	C6	93	HD7	117	D7
22	M6	46	VREF	70	C7	94	CLMP	118	CAS
23	M5	47	FREF	71	N/C	95	VDD	119	GND
24	M4	48	HREF	72	GND	96	D15	120	VDD

Table 2: 120 Pin QFP Pin Assignment

Signal	Direction	JTAG Bit Number	Signal	Direction	JTAG Bit Number	Signal	Direction	JTAG Bit Number
A8	OUT	145	Y2	OUT	93	HD5	OUT	43
A7	OUT	144	Y2	IN	92	HD5	IN	42
A6	OUT	143	Y3	OUT	91	HD6	OUT	41
A5	OUT	142	Y3	IN	90	HD6	IN	40
A4	OUT	141	Y4	OUT	89	HD7	OUT	39
A3	OUT	140	Y4	IN	88	HD7	IN	38
A2	OUT	139	Y5	OUT	87	cdata_oeb*	OUT	37
A1	OUT	138	Y5	IN	86	CLMP	OUT	36
A0	OUT	137	Y6	OUT	85	D15	OUT	35
RW	OUT	136	Y6	IN	84	D15	IN	34
RAS	OUT	135	Y7	OUT	83	D14	OUT	33
dram_oeb	OUT	134	Y7	IN	82	D14	IN	32
M7	OUT	133	HBLNK	OUT	81	D13	OUT	31
M7	IN	132	C0	OUT	80	D13	IN	30
M6	OUT	131	C0	IN	79	D12	OUT	29
M6	IN	130	C1	OUT	78	D12	IN	28
M5	OUT	129	C1	IN	77	D11	OUT	27
M5	IN	128	C2	OUT	76	D11	IN	26
M4	OUT	127	C2	IN	75	D10	OUT	25
M4	IN	126	C3	OUT	74	D10	IN	24
M3	OUT	125	C3	IN	73	D9	OUT	23
M3	IN	124	C4	OUT	72	D9	IN	22
M2	OUT	123	C4	IN	71	D8	OUT	21
M2	IN	122	C5	OUT	70	D8	IN	20
M1	OUT	121	C5	IN	69	D0	OUT	19
M1	IN	120	C6	OUT	68	D0	IN	18
M0	OUT	119	C6	IN	67	D1	OUT	17
M0	IN	118	C7	OUT	66	D1	IN	16
MCLK	OUT	117	C7	IN	65	D2	OUT	15
MCLK	IN	116	yuv_oeb	OUT	64	D2	IN	14
m_oeb	OUT	115	CGTOUT (N/C)	OUT	63	D3	OUT	13
REQYUV	IN	114	cgtout_oeb	OUT	62	D3	IN	12
FSIG	OUT	113	SCLK	IN	61	D4	OUT	11
FSIG	IN	112	HA0	IN	60	D4	IN	10
RST	IN	111	HA1	IN	59	D5	OUT	9
TOE	IN	110	HA2	IN	58	D5	IN	8
VREF	OUT	109	HA3	IN	57	D6	OUT	7
VREF	IN	108	WR	IN	56	D6	IN	6
FREF	OUT	107	RD	IN	55	D7	OUT	5
FREF	IN	106	CEN	IN	54	D7	IN	4
HREF	OUT	105	HD0	OUT	53	d-oeb*	OUT	3
HREF	IN	104	HD0	IN	52	CAS	OUT	2
CREF	OUT	103	HD1	OUT	51	VRST	IN	1
CREF	IN	102	HD1	IN	50	FRST	IN	0
refs_oeb	OUT	101	HD2	OUT	49			
c_dec_b		100	HD2	IN	48			
CSYNC	OUT	99	HD3	OUT	47			
csync_oeb	OUT	98	HD3	IN	46			
Y0	OUT	97	HD4	OUT	45			
Y0	IN	96	HD4	IN	44			
Y1	OUT	95						
Y1	IN	94						

Table 3: JTAG Register Allocation

CGTOUT (N/C) This pin is only used for GPS test purposes and should not be used for system purposes.

Section 5

H.261 Evaluation Board

VPB261

H.261 EVALUATION BOARD

FEATURES

- Complete evaluation and prototyping system for GEC Plessey Semiconductors H.261 Video Compression/Decompression chipset.
- Fully software configurable IBM PC/XT/AT compatible expansion card
- RGB input and output at Rec. 601 resolution
- Optional gamma correction of input RGB data (VP510)
- Supports coding/decoding of CIF and QCIF images at data rates up to 2Mbits/s and frame rates up to 30Hz
- Three 8 bit video ADCs (GPS VP8708) provide 24 bit colour accuracy
- Triple 8 bit video DAC (GPS VP101) for RGB display
- All RAM requirements fully localised (DRAM & SRAM)
- Tristateable busses allow incremental CODEC evaluation

EVALUATION BOARD OVERVIEW

RGB format video is input to the board from a source which can be gen-locked to the composite sync signal provided by the VP520 video filter in the decode path (figure 1).

RGB data is sampled at the system clock frequency (27MHz) using an individual VP8708 for each of the RED, GREEN and BLUE channels. The data is colour space converted, filtered and coded to H.261 specification and passed to the transmission channel. The transmission channel is normally a simple link to the decoder section of the board, however this can be intercepted and output to another evaluation board, a network/ISDN Terminal Adaptor or a different H.261 decoder if desired. It is also possible to input H.261 data from another system and decode and display using the VPB261.

There is also the option of alternative video I/O formats via two headers on the PCB.

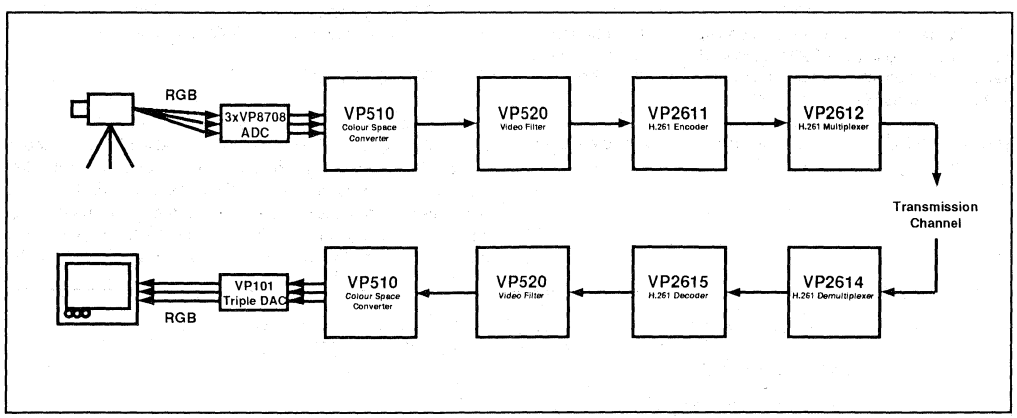


Fig.1 Block Diagram of The Evaluation Board

SOFTWARE

The software provided with the board allows the user to set up each device in all modes to allow for maximum board flexibility. The coefficients and setups in the VP510s and VP520s are fully programmable via the software, as are the setups in the VP2611, VP2612, VP2614 and VP2615.

The software runs under Microsoft Windows 3.1 and allows the user to access the internal registers of each chip.

PC BUS INTERFACE

The board interfaces to the PC over a standard IBM XT 8 bit interface. There is an individual address register on the board, which is written to whenever any of the devices are to be addressed. This register should contain the address internal to the device that is being written to / read from. The actual data is then transferred to/from the device on the board by addressing that device in the PC I/O map. This means that whenever data is to be passed to / from a device on the board it requires two PC operations, the first always being a write. (Except in the cases of the VP2611 and VP2615 where four PC operations will be completed due to the individual addressing strategy of these devices, see the datasheets for each of these devices for more information.)

An example of some code showing this is given in Fig.2.

Here, two aliases for the addresses in I/O space of the address register (311 hex) and the VP520 in the decoder side (31E hex) have been set up. In the code section, two registers internal to the VP520 have been programmed: the register in location C, the blanked screen Y value, and the register in location D, the blanked screen U value have been programmed with 64 and 20 hex respectively. (See VP520 data sheet for more information on these registers.)

The third part of the code section shows a read function from status register B in the VP2614. (First of all the address in the device is loaded into the address register, and then the value of the register is read from the device.)

The board is also supplied with some simple source code examples.

TRISTATE CONTROL

The board allows back to back coding/decoding in each successive stage of the system. This allows incremental evaluation of the coding process (see figure 3).

The tri-stating on the board is controlled by writing to another register, the board control register. This register provides the control for the tristate buffers and also controls the bit rate of the transmission channel. The first three bits of the lower nibble of this register are used for the tristate control, and one of the following values MUST be written to the nibble:

0 = 510 - 510
1 = 510 - 520 - 520 - 510
3 = 510 - 520 - 2611 - 2615 - 520 - 510
7 = Full H.261 encode / decode
{anything else = undefined operation}

SERIAL BIT RATE CONTROL

The serial bit rate is controlled by writing to the upper nibble of the board control register. The clock generated by the on board oscillator is on the encode side of the board. That is, if the user wishes to inject H.261 data from an external source via connector P2, the appropriate control lines should be asserted and jumpers JP2 to JP6 removed. (It is possible, however, to crudely run the decoder by providing a clock and H.261 data only, leaving the line controls connected to the on-board encoder.)

The table below shows the bit rate for each value written to the upper nibble of the board control register. Note this nibble MUST be programmed with one of the following values:

2 = 2.048 Mbits/s	3 = 1.024 Mbits/s
4 = 512 kbits/s	5 = 256 kbits/s
6 = 128 kbits/s	7 = 64 kbits/s

{anything else = undefined operation}

BUFFER CONTROL

When the buffer control option is selected, the buffer read and write pointers of the VP2612 are monitored to obtain a fullness value. This value is used to determine the quantisation of the encoder. If the buffer fullness reaches a certain threshold level the next frame is skipped. There is a linear relationship linking the fullness and bitrate parameters to quantiser and threshold levels - the threshold may also be adjusted via the software controls.

```
/* alias section */
addr_reg  = $311;     /* These are the addresses of the    */
VP2614    = $31C;     /* devices in the PC I/O memory map */
VP520_dec = $31E;

/* code section */
     port[addr_reg]  := $C;
     port[VP520_dec] := $64;

     port[addr_reg]  := $D;
     port[VP520_dec] := $20;

     port[addr_reg]  := $1;
     status_1        := port[VP2614];
```

Fig.2 Example of code

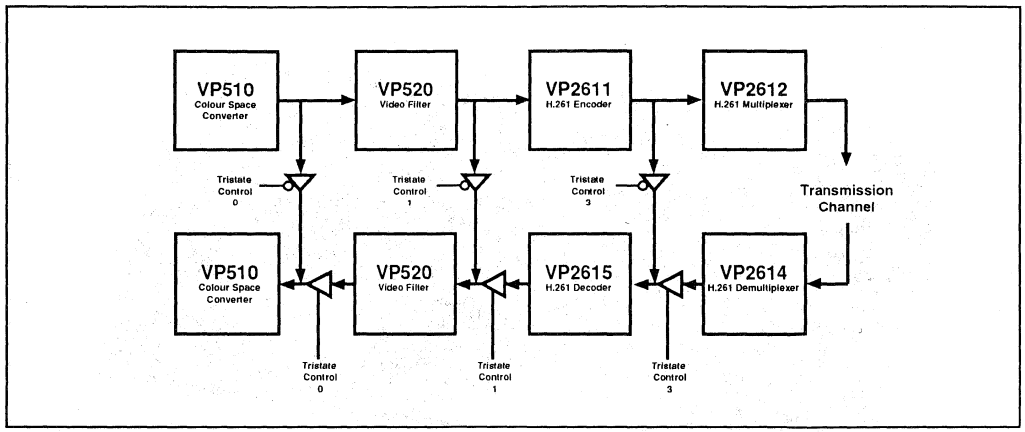


Fig.3 Tristate Connecting for incremental evaluation

COMPONENT SUMMARY

VP8708 Video ADC (Note 1)
A 30MHz analog video interface which includes a video amplifier with clamp and gain control and an internal voltage reference. The output of the video amplifier is externally connected to an anti-aliasing filter (3dB point approx. 6.75MHz) and then re-input to the device for final analog to eight bit digital conversion.

VP101 Triple 8 Bit CMOS Video DAC (Note 1)
A 30MHz or 50MHz device which uses video control inputs (BLANK, SYNC and REF WHITE) to provide appropriate levels required for standard video signals.

VP510 Bidirectional Colour Space Converter
The VP510 converts three channels of RGB data into two channels of decimated luminance and chrominance data. Each channel has its own lookup table, loaded via the software and used for gamma correction and/or ranging. There are two of these devices on board: one to convert RGB to Y-UV (in the encode path) and one to convert Y-UV to RGB (in the decode path). The direction of data flow in the device is set in the control word.

VP520 PAL/NTSC to CIF/QCIF Converter (Note 2)
The VP520 converts between CCIR601 resolution raster scan Y-UV data and H.261 format CIF/QCIF macroblocks. The VP520 supports both PAL and NTSC formats. All on board vertical and horizontal FIR filter coefficients are fully programmable (via software).

VP2611 H.261 Encoder
This device performs DCT, quantisation and run length coding of the input macroblocks. Optional quantisation weighting tables may also be programmed via the software interface. With a 27 MHz clock the device will accept data produced to full CIF resolution up to 30Hz frame rate. The VP2611 also implements motion estimation within a search window of +/- 7 pixels.

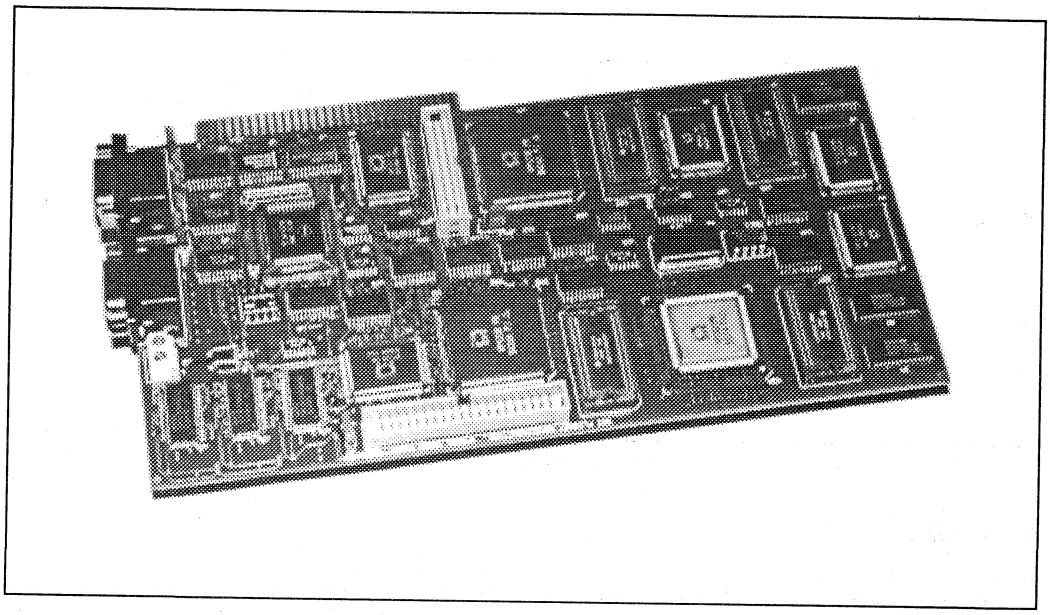
VP2612 Video Multiplexer
The VP2612 will convert run length coded data from the VP2611 encoder into an H.261 compatible bitstream. The serial port outputs the bitstream in frames containing header information and a BCH(511,493) cyclic redundancy code for error detection/correction.

VP2614 Video Demultiplexer
The device will extract error corrected parameters and run length coded DCT coefficients from an H.261 bitstream. It outputs data in the format required by the VP2615.

VP2615 H.261 Decoder
The VP2615 will take run length coded coefficients which have been error corrected and Huffman decoded, and output Y-UV data in macroblock format at CIF/QCIF resolutions.

Note 1 These devices are being withdrawn from sale and are not recommended for new designs. However it is anticipated that most target applications will use composite video decoder/encoder devices to interface video directly to the VP520 (e.g. described in Application Note, AN205).

Note 2 The VP520 is being superseded by the lower power VP520S.



ORDERING INFORMATION

VPB261/--/APPL H.261 Evaluation Board

Note Owing to the pending obsolescence of certain devices the supply of this evaluation board may be discontinued during the life of this handbook. Please confirm availablity with your GPS Customer Service Centre.

Section 6
Digital Video

GEC PLESSEY
SEMICONDUCTORS

VP510

BI DIRECTIONAL COLOUR SPACE CONVERTER

FEATURES

- User definable colour space conversion
- Sampling rates up to 27 MHz
- On chip decimating or interpolating FIR filters
- Conversion from 24 bit inputs to 16 bit outputs or vice versa
- RAM based look up tables for gamma correction
- 100 pin Quad Flat Pack

ASSOCIATED PRODUCTS

- VP2611 Integrated H.261 Video Encoder
- VP2615 H.261 Video Decoder
- VP520S Two dimensional Video Filter

ORDERING INFORMATION

VP510 CG GPFR

(Commercial Temperature - PLCC Package).

DESCRIPTION

The VP510 converts three channels of RGB data into two channels of decimated chrominance and luminance data. Alternatively it converts two channels of luminance and chrominance data into three channels of interpolated RGB data. Each channel has its own RAM based look up table, which can be loaded from a host system and then used for gamma correction and/or ranging.

The direction of the data flow is controlled by a bit in a Control Register, and causes previous outputs to become inputs and vice versa. The filters change from the decimating to the interpolating mode, and correspondingly follow or precede the colour space conversion.

The 3 x 3 conversion matrix is provided with user definable 12 bit coefficients which have a range from -4.0 to +4.0. The luminance channel is provided with a 23 tap low pass filter which can decimate or interpolate by two. The chrominance channels each have two 11 tap filters in series which can decimate or interpolate by four. This arrangement allows the device to accept or produce RGB data which has been 2x oversampled, thus avoiding the need for external analog anti-aliasing filters. If necessary the device will still accept or produce video data which has not been oversampled.

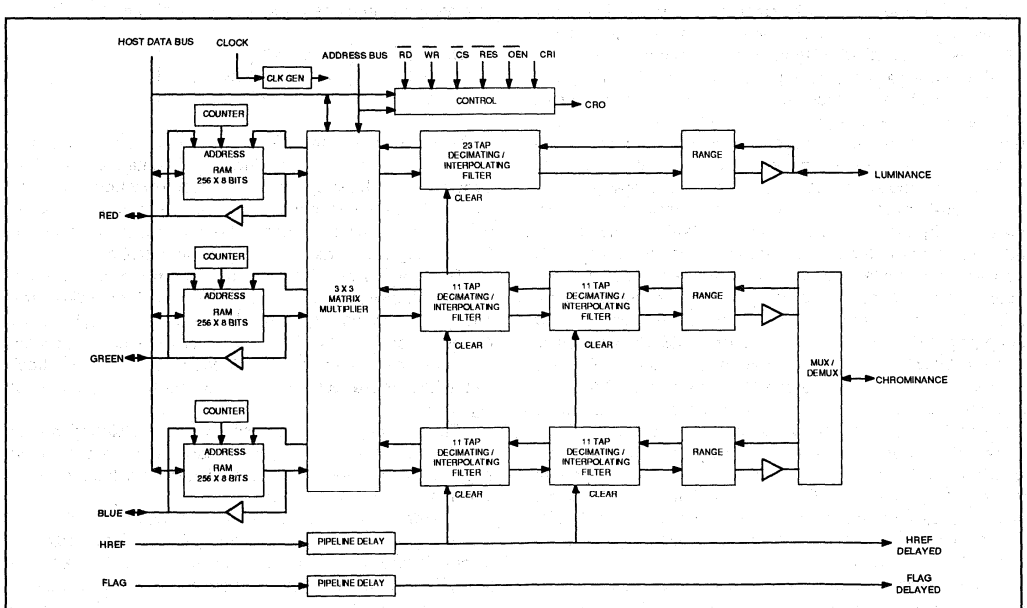


Figure 1. Simplified Block Diagram

PIN DESCRIPTION

PIN	TYPE	DESCRIPTION
R7:0	I/O	Unsigned Red data. Range may be changed by the RAM look up table
G7:0	I/O	Unsigned Green data. Range may be changed by the RAM look up table
B7:0	I/O	Unsigned Blue data. Range may be changed by the RAM look up table
Y7:0	I/O	Unsigned Luminance data in or out. Range is user definable
C7:0	I/O	Two's complement or offset binary multiplexed chrominance data. Range is user definable
D7:0	I/O	Host data bus used for reading or writing
A4:0	I	Host Address Bus. Matrix coefficients and the control register are directly addressable
CLK	I	External line locked clock. All inputs and outputs are referenced to the rising edge
HREF	I	Horizontal or Composite reference used as a start of line indicator and to clear the FIR filters
HDLY	O	HREF input delayed by the 39 clock delay to a correctly filtered output
FI	I	Input Flag as defined by the user. No internal operation.
FO	O	FI delayed by the 39 clock delay to a correctly filtered output
CRI	I	An input which indicates that valid luminance and chrominance data is present
$\overline{\text{CRO}}$	O	An output which indicates that valid luminance and chrominance data is on the output pins
$\overline{\text{OEN}}$	I	Active low output enable for the tristate bus. Used in conjunction with a Control Register bit
$\overline{\text{CS}}$	I	Active low Chip Select from the host system
$\overline{\text{RD}}$	I	Active low request from the host to read the matrix coefficients and RAM contents
$\overline{\text{WR}}$	I	Active low request from the host to write to the device
$\overline{\text{RES}}$	I	Asynchronous low reset used to initialise the device. Must be present for at least 1024 clock periods

LOOK UP TABLES

When the device is configured to produce chrominance and luminance outputs from RGB inputs, each of the three look up tables is addressed by its appropriate colour bus. Any changes to the data thus occur before the colour space conversion. Typically the look up tables are used to provide gamma correction to linear RGB inputs, and / or to limit the range of the inputs. The coefficients in the conversion matrix are usually defined to expect either a range of 1 - 254 or 16 - 235, when converting to Cr and Cb chrominance values.

When the device is configured to produce RGB outputs, the look up tables are positioned just before the output buses. If linear outputs are required the tables can then be used to remove the gamma correction which is produced by the coefficients in the conversion matrix. They can also be used to expand the range produced by the conversion matrix.

The RAM's are not dual ported and use by the host system takes priority over pixel accessing. The RAM's are not directly addressable from the host since the device only uses a 5 bit address bus. Instead each RAM has an internal address counter which must be cleared by writing to address decimal 27. Data is then sequentially written to the Red RAM by supplying 256 bytes of data and address 28. Similarly using address 29 will cause write operations to the green RAM, and address 30 will cause write operations to the blue RAM. The counters do not wrap around and must be reset by using address 27 before further write or read operations are required. Read operations are mechanized in a similar manner to write operations, except that a read strobe must be supplied instead of a write strobe. Since each RAM has its own address counter the red, green, and blue operations can be intermingled on a byte by byte basis, rather than completing one colour before starting the next.

Although host operations are asynchronous to the device clock, this clock must be present to internally effect a read or write operation. The read and write strobes are internally synchronized to the clock, and the read strobe must be active for at least five clock periods, and the write strobe for two clock periods.

CONVERSION MATRIX

The 3 x 3 matrix multiplier performs the following basic operation on three channels with identical sampling rates;

$$\begin{vmatrix} O/PA \\ O/PB \\ O/PC \end{vmatrix} = \begin{vmatrix} c1 & c2 & c3 \\ c4 & c5 & c6 \\ c7 & c8 & c9 \end{vmatrix} X \begin{vmatrix} I/PA \\ I/PB \\ I/PC \end{vmatrix}$$

When converting from RGB to colour difference information, any decimation of the chrominance channels must be done after the above operation. Conversely when producing RGB data the chrominance channels must be interpolated before the matrix operation. The configuration bit in the Control Register takes care of this reorganization.

The coefficients C9:1 are loaded from the host system, and are directly addressable using the 5 bits provided (see Table 1). Each coefficient must be loaded as two bytes since it uses a total of 12 bits. The upper 4 bits in the most significant byte are don't care values. If the loaded values are read back by the host, these four bits will always be zero's, and are not sign bits.

The 12 coefficient bits are comprised of 3 signed integer and 9 fractional bits. This gives a decimal range of -4.00 to approximately +3.998, with the fractional bits actually giving a decimal resolution of 0.001953.

Pixel data going into the matrix multiplier uses a total of 13 bits; 10 signed integer bits plus 3 fractional bits. This additional pixel accuracy is only obtained from the output of the interpolating filters, where 10 integer bits are necessary to accommodate signed data with undershoot and overshoot beyond the nominal gain.

In the RGB to chrominance and luminance mode, when pre interpolation does not occur, only 8 unsigned integer bits are available from the look up table. Thus, within the 13 bit total, the top 2 bits plus the bottom 3 bits will be made into zero's.

Intermediate precision within the matrix multiplier grows to 15 signed integer bits plus 6 fractional bits. The least significant 9 or 10 of the integer bits are selected at the output, and the fractional bits are rounded to 3 bits. Ten integer bits are used when the matrix is producing RGB from interpolated chrominance and luminance. This allows for undershoot and overshoot beyond the nominal 8 bit unsigned value.

Only 9 integer bits are necessary when the matrix is producing chrominance, and the three fractional bits provide additional precision into the decimating filter. In fact, if the matrix is producing normalized chrominance, the coefficients will have been chosen to produce an output in the range ±127. This range only requires 8 integer bits, and the ninth bit will be a repeated sign bit. Note that ±127 is actually representing ±0.5 in this context. When the NORM bit in the Control Register is reset, the chrominance outputs lie in the range ±1, or ±256 in our internal representation. The full 9 integer bits are then needed.

LUMINANCE FILTER

The luminance channel contains a 23 tap low pass filter with internally defined 10 bit signed coefficients. When the MODE bit in the Control Register is reset the filter will decimate the sampling rate by two. When the MODE bit is set the filter will interpolate the incoming data to produce outputs at twice the incoming sampling rate. The filter coefficients remain the same in both cases, but the gain is adjusted to preserve the energy content..

When the filter is producing decimated luminance it accepts data from the matrix converter with 9 signed integer bits plus 3 fractional bits (9.3). Since luminance is always positive, however, the most significant bit will be zero. Words within the filter calculation are allowed to grow to 15 integer bits plus 6 fractional bits. This is then rounded to 15 bits plus 3 fractional bits, and finally the 10 least significant integer bits are chosen to give a 10.3 result. The 10 bit integer component allows for any undershoot or overshoot in the nominal 0 to 255 luminance range. The three fractional bits are used to round the integer component to a 10 bit value. This is then clipped to a value between 0 and 255. Negative values become zero, and positive values greater then 255 will saturate at 255. Outputs will not saturate under normal operating conditions, and the circuit is only necessary to prevent overflow when the input swings between the maximum and minimum values. Figure 2 illustrates the bit significance at various points in the data path.

When the filter is used to interpolate incoming luminance data, the 8 bit input is padded to the 9.3 format used previously. The 13 bit output from the filter is applied to the matrix converter without further rounding.

The response given by the filter is shown in Figure 3. Stop band attenuation is approximately 45 dB, and the maximum pass band ripple is 0.07 dB. These figures were obtained with 10 bit quantized coefficients and unquantized data. The effects of the various quantization steps within the filter, plus the reduction to 10 bits, is superimposed upon Figure 3. Also shown is the CCIR601 specification for a luminance or RGB

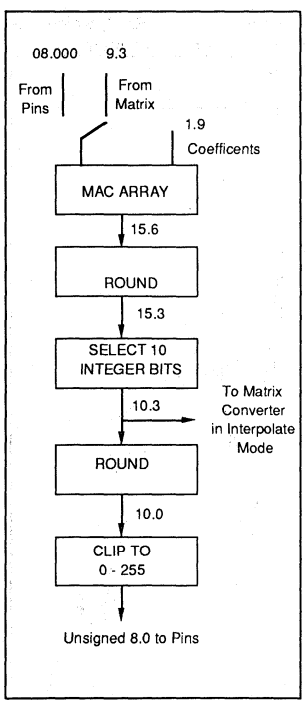


Fig 2. Bit significance in the Y Filter

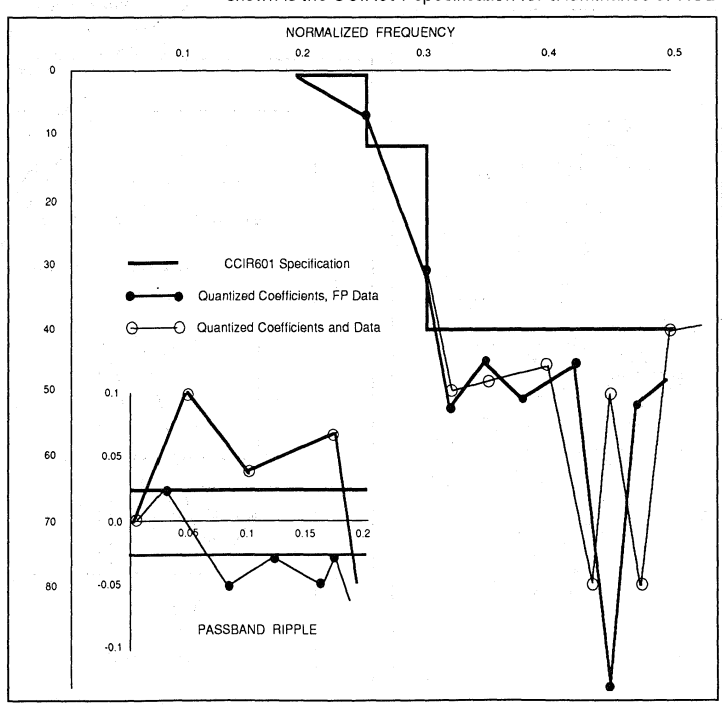


Figure 3. Response of the Luminance Filter

filter with 13.5 MHz output sampling.

CHROMINANCE FILTERS

Each chrominance channel has two 11 tap filters in series and each pair can decimate or interpolate by four. The MODE bit defines whether the filters interpolate or decimate. The coefficients are 10 bit internally defined values, and are the same in both modes. Figure 4 illustrates the bit significance at various points in the calculation.

When the filters are used to decimate chrominance produced by the matrix converter, the inputs are represents by either 8 or 9 signed integer bits plus 3 fractional bits. When the matrix coefficients have been chosen to produce normalized chrominance, the range can be represented by 8 integer bits. Otherwise 9 integer bits are needed. When the inputs are chrominance from the pins, the 3 fractional bits are set to zero, and the ninth bit is sign extended. Words within the filter calculation are allowed to grow to 15 integer bits plus 6 fractional bits. This is then rounded to 15 bits plus 3 fractional bits.

When the filter is used to supply interpolated data to the matrix converter, the least significant 10 integer bits are selected out of the 15 outputs. Only 9 integer bits are actually needed to represent the filtered chrominance with undershoot and overshoot, but the hardware multiplier expects a 10 bit number.

When the filter is producing decimated chrominance, the NORM bit in the Control Register is used to select which 12 integer and fractional bits will be used by the rounding and clipping circuit. For a full description of this operation see the section on Chrominance Outputs.

The response of the filters is given in Figure 5. These results were obtained with 10 bit quantized coefficients and unquantized data. The effects of the various quantization steps within the filter, and then finally rounding down to a 9 bit value are superimposed onto Figure 5. Also shown is the CCIR601 specification for sample rate conversion down to 4:2:2 resolution.

RGB INPUTS

The 24 bit RGB data must meet the set up and hold requirements, with respect to the rising edge of the clock, which are specified in Figure 6. The first edge after HREF has gone inactive (i.e. high) must strobe in the first samples if the delay to the first correctly filtered output is to match the fixed pipline delay of 39 clock to the HDLY and FO outputs. The maximum range is 0 to 255 for each component. If the coefficients in the matrix converter are defined for a restricted input range then this must be guaranteed by the user. Alternatively the look up tables can be used to limit the range. When HREF goes active low the outputs will go low after 39 clocks.

The VP510 has been designed to accept two times oversampled RGB data from an A/D converter. This avoids the need for analog anti aliasing filters before the A/D converters. For this reason the clock used by the VP510 is expected to be twice the sampling clock needed to produce a given number of RGB pixels per line. If the RGB inputs have not been oversampled this double rate clock should still be used. Each incoming sample will then be internally used twice, but the decimating filters will still produce the correct luminance and chrominance values.

Each input directly addresses its own RAM, which has been pre-loaded to meet the system requirements. Linear

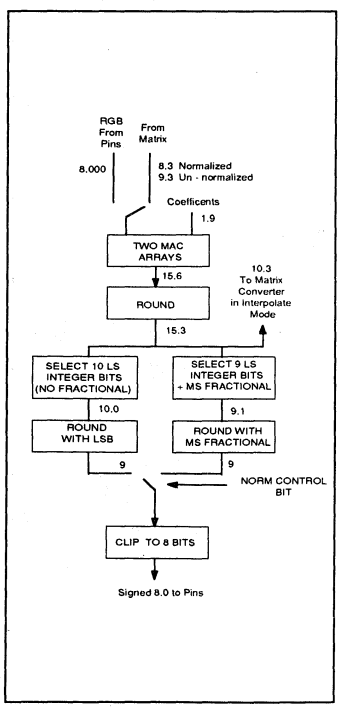


Figure 4. Bit significance

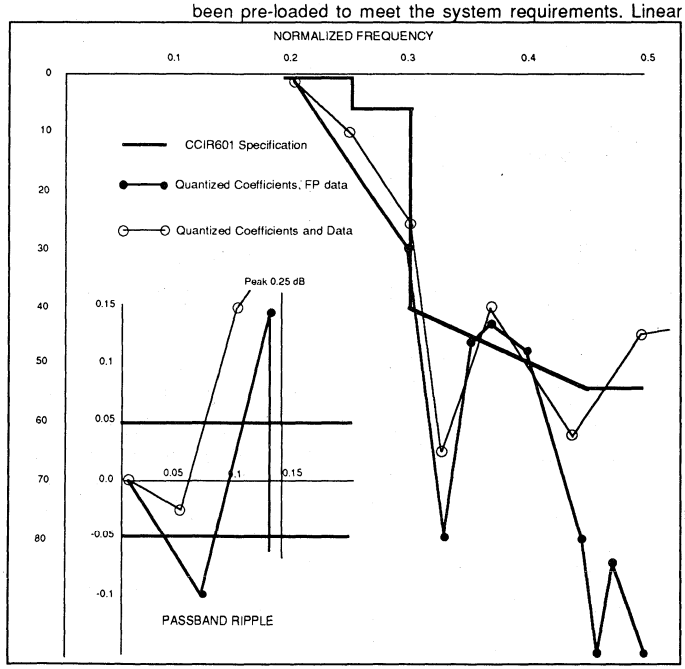
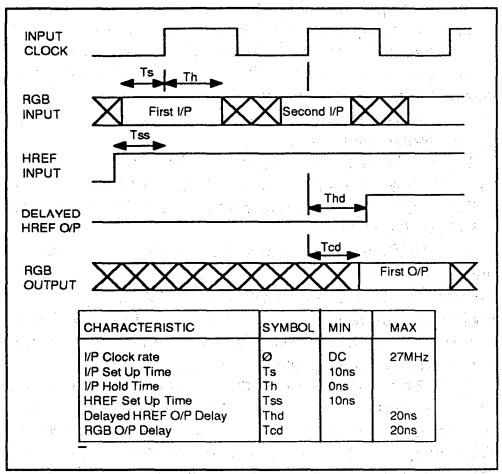


Figure 5. Response of the Chrominance Filters



CHARACTERISTIC	SYMBOL	MIN	MAX
I/P Clock rate	Ø	DC	27MHz
I/P Set Up Time	Ts	10ns	
I/P Hold Time	Th	0ns	
HREF Set Up Time	Tss	10ns	
Delayed HREF O/P Delay	Thd		20ns
RGB O/P Delay	Tcd		20ns

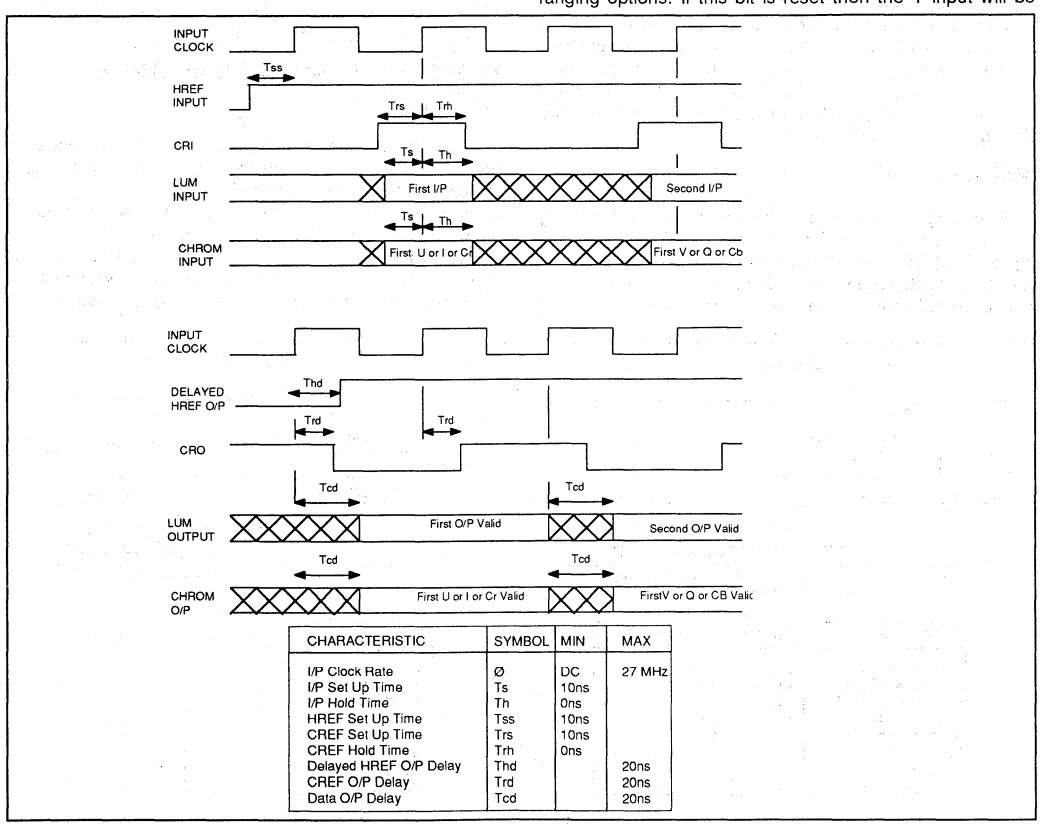
Figure 6. RGB I/O Timing (Advanced Data)

RGB data must normally be gamma corrected by the RAM's before colour space conversion.

LUMINANCE AND CHROMINANCE INPUTS

The 16 bit luminance and chrominance values must meet the set up and hold times, with respect to the rising edge of the clock, which are specified in Figure 7. Since the input rate will be half the clock rate an additional signal is required to indicate alternate clock periods. This signal (CRI) must also meet the set up and hold requirements given in Figure 7. On the first occurrence of CRI after HREF goes inactive (High), the 16 bit input bus must contain the first 8 bit luminance component plus the first 8 bit U,I, or Cr component, if the delay to the first correctly filtered output is to match the fixed pipeline delay to the HDLY and FO outputs. On the second occurrence it must contain the second luminance component plus the first V, Q, or Cb component. When HREF goes low the outputs will be forced low after the 39 clock pipeline delay.

YUV or YIQ data is directly applied to the interpolating filters by setting the BYPASS Bit in the Control Register. When Y Cr Cb data is to be used this bit should be reset, and the inputs will then be applied to the ranging and offset circuitry. The SEL bit in the Control Register is used to determine the ranging options. If this bit is reset then the Y input will be



CHARACTERISTIC	SYMBOL	MIN	MAX
I/P Clock Rate	Ø	DC	27 MHz
I/P Set Up Time	Ts	10ns	
I/P Hold Time	Th	0ns	
HREF Set Up Time	Tss	10ns	
CREF Set Up Time	Trs	10ns	
CREF Hold Time	Trh	0ns	
Delayed HREF O/P Delay	Thd		20ns
CREF O/P Delay	Trd		20ns
Data O/P Delay	Tcd		20ns

Figure 7. Chrominance I/O Timing (Advanced Data)

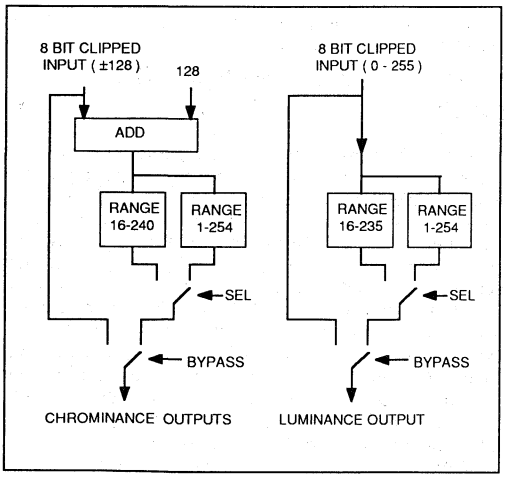


Figure 8. Chrominance and Luminance Output Options

adjusted to have a range of 16 - 235, and the Cr and Cb inputs will be adjusted to 16 - 240. If the SEL bit is set the range will be 1 - 254 for all three inputs. After either ranging option 128 is subtracted from the Cr and Cb channels before they are applied to the matrix converter. Note that if the incoming Y Cr Cb data is already correctly ranged then the range circuit will have no further action. The BYPASS pin must, however, still be reset or the offset of 128 will not be subtracted from the chrominance channels.

RGB OUTPUTS

RGB outputs will be valid after the delay from the rising edge of the clock given in Figure 6. A version of the HREF input is provided (HDLY), which has been delayed by the same number of clock periods as the data. This indicates when the first converted samples are available from each line.

In normal operation of the VP510 the clock input will be two times the sampling clock required to produce a given number of pixels per line. The device then produces RGB outputs at this double rate, and thus avoids the needed for analog anti aliasing filters after the D/A converters. Incoming luminance data is interpolated by two, and chrominance data by four, to achieve these output rates.

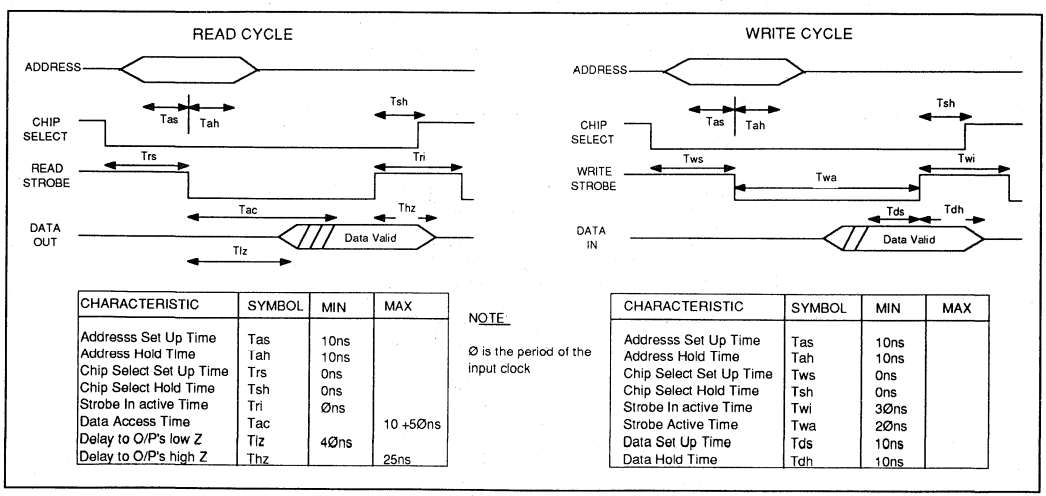
For standard CCIR601 video with 720 RGB pixels per line the clock needed would thus be 27 MHz. For square pixel NTSC a clock of 24.54 is needed, and square pixel PAL needs a clock of 29.5 MHz.

If the RGB outputs are connected to a frame store rather than driving a D/A converter, then these oversampled outputs are probably not needed. Since the RGB data will not contain any frequencies above one quarter the clock rate used by the VP510, then the user can simply just use every other output sample without causing aliasing effects.

Each 8 bit output value is obtained from the output of the matrix converter, which is internally represented by 13 bits. This comprises 10 signed integer bits plus three fractional bits. At this point the RGB values have a range of -512 to +511, which is sufficient to accommodate any overshoot or undershoot produced by the filters. If the most significant fractional bit is set, then the integer bits are incremented by one, and the result is then clipped. Negative values will be forced to zero, and values greater than +255 will be forced to saturate at +255. The resulting unsigned 8 bit number is made available on the output pins, as shown in Figure 2.

LUMINANCE AND CHROMINANCE OUTPUTS

The 16 bit output bus changes on alternate rising edges of the clock, with the delay specified in Figure 7. Each output remains valid for two clock periods and is either comprised of a luminance byte plus a U, I, or Cr component, or another luminance byte plus a V, Q, or Cb component. The sequence of events following the HREF delayed output is shown in Figure 7. The CRO signal can be used as a clock enable or a half rate clock for the next component in the system.



CHARACTERISTIC	SYMBOL	MIN	MAX
Addresss Set Up Time	Tas	10ns	
Address Hold Time	Tah	10ns	
Chip Select Set Up Time	Trs	0ns	
Chip Select Hold Time	Tsh	0ns	
Strobe In active Time	Tri	Øns	
Data Access Time	Tac		10 +5Øns
Delay to O/P's low Z	Tlz	4Øns	
Delay to O/P's high Z	Thz		25ns

NOTE

Ø is the period of the input clock

CHARACTERISTIC	SYMBOL	MIN	MAX
Addresss Set Up Time	Tas	10ns	
Address Hold Time	Tah	10ns	
Chip Select Set Up Time	Tws	0ns	
Chip Select Hold Time	Tsh	0ns	
Strobe In active Time	Twi	3Øns	
Strobe Active Time	Twa	2Øns	
Data Set Up Time	Tds	10ns	
Data Hold Time	Tdh	10ns	

Figure 9. Host Interface Timing (Advanced Data)

ADDR	FUNCTION	ADDR	FUNCTION
0	C1 L Byte	1	C1 H Byte
2	C2 L Byte	3	C2 H Byte
4	C3 L Byte	5	C3 H Byte
6	C4 L Byte	7	C4 H Byte
8	C5 L Byte	9	C5 H Byte
10	C6 L Byte	11	C6 H Byte
12	C7 L Byte	13	C7 H Byte
14	C8 L Byte	15	C8 H Byte
16	C9 L Byte	17	C9 H Byte
27	RAM Address Reset		
28	R/W Red RAM		
29	R/W Green RAM		
30	R/W Blue RAM		
31	Control Register		
18 - 26	Not Used		

Table 1. Internal Address Map

Internally the luminance component obtained from the decimating filter is represented by the 10 least significant integer bits plus 3 fractional bits. The 10 integer bits accommodate any undershoot or overshoot caused by the filter. If the most significant fractional bit is set, then the integer bits are incremented by one. The resulting 10 bit signed integer value ,representing ±512, is then clipped to provide an 8 bit, positive only, number. Negative values become zero, and values greater than 255 will saturate at 255.

The NORM bit in the Control Register determines which bits out of the 15.3 available are selected from the outputs of the chrominance filters. The choice is illustrated in Figure 4. If the user is working with normalized chrominance, then the matrix coefficients will have been chosen to produce outputs in the range of ±128 (representing ±0.5). This range only requires 8 signed integer bits, and the ninth bit going into the filter will be a repeated sign bit. The 9 least significant integer bits are then selected out of the 15 available from the output of the filter. These are then sufficient to accommodate any undershoot and overshoot beyond the 8 bit input, and are rounded with the most significant fractional bit. The resulting 9 bit signed value is clipped to an 8 bit signed number with a range of ±128, representing ±0.5. Values outside the range are clipped to the maximum values allowed.

When chrominance is not normalized the range becomes ±1, or ±256 in our internal notation. This range needs all 9 bits of the integer component going into the filter, and requires 10 integer bits coming out of the filter to allow for undershoot and overshoot. The 9 bit value expected by the clipping circuit is now produced by using the least significant integer bit to round the next 9 integer bits. This word is then clipped to an 8 bit signed value with a range of ±128, but now representing ±1 since higher order bits were selected at the output of the filter.

If the BYPASS bit is set in the Control Register, these values are passed directly to the output pins. If this bit is reset they are further modified in a manner determined by the SEL bit in the Control Register. This is illustrated in Figure 8.

If the SEL bit is set, then zero luminance values become 1 and value 255 is clipped at 254. If the SEL bit is reset, then values below 16 will be forced to decimal 16 and values greater than 235 will be forced to 235.

When the BYPASS bit is reset decimal 128 will be added to each chrominance channel, to provide a positive only number. The SEL bit then either limits the range to 1 to 254 or to 16 to 240. Values outside those ranges are respectively forced to the minimum or maximum values. Note that if the BYPASS pin is reset then the NORM bit must be set.

HOST INTERFACING

The VP510 utilizes a conventional microprocessor interface except that the RAM based look up tables are not directly addressable. The address inputs must meet set up and hold times with respect to the front edge of the read and write strobes. These are given in Figure 9. Note that the address inputs are internally latched, and need not stay valid for the whole of the strobe times. Chip select, however, must stay active for the whole of the strobe times.

Data, which is to be written to the RAM or Control Register, must meet set up and hold times with respect to the back edge of the write strobe. These are also given in Figure 9. The device clock must be present for the write operation to occur, and internal synchronization takes place. For this reason the write strobe must be active for at least 2 clock periods.

Reading data from the VP510 also requires the presence of the device clock. Data from the RAM is internally pipelined and the read strobe must be active for at least 5 clock periods (4 pipeline delays plus synchronization). The output bus will not go low impedance before this pipeline delay.

The matrix coefficients and the Control Register are directly addressable, and use the locations given in Table 1. Four addresses are used to access the three RAM's, and the scheme used is descibed in the section on the look up tables.

DEVICE CONFIGURATION

The device is configured by means of bits in a Control Register. A reset pulse must be applied, whilst the device clock is active, before loading the Control Register. The reset pulse will actually clear all the control bits to zero, and ensure that neither output bus is low impedance, even if OEN is low.

The significance of the bits is given below. For a fuller description of individual bits see the releant sections.

BIT	NAME	FUNCTION
0	OEI	This bit must be set and the OEN pin must be low for either the 24 or 16 bit output bus to be low impedance. The status of the MODE bit determines which bus is actually enabled as an output. With this arrangement either bus can be controlled by software or by driving a pin.
1	SEL	This bit controls the range of the luminance and chrominance data. When high the I/O range is 1-254. When low the luminance is 16-235 and the chrominance is 16-240.
2	MODE	This bit selects the direction of operation. When low the 24 bit bus represents RGB inputs and the 16 bit bus represents luminance and chrominance outputs. The filters then deci mate. When high the data flow reverses and the filters interpolate.

3 BYPASS This bit should be reset when Cr Cb data is to being processed. NORM must then be set.It should be set when the ranging and offset circuit is to be bypassed.

4 NORM When this bit is reset the chrominance outputs are not normalized, and the 8 bit outputs rep resent a range of ±1. When NORM is set the outputs will represents a range of ±0.5, still using 8 bits.

7:5 Reserved. Must all be reset.

CONVERSION BETWEEN RGB AND YUV

If incoming, gamma corrected, analog RGB is normalized to a range of 0 to 1, then the following coefficients will produce YUV outputs. Y will have a range of 0 to 1, U will have a range of ±0.436, and V will have a range of ±0.615. The NORM bit must be reset, and the BYPASS bit set. The 8 bit chrominance outputs then represent a possible range of ±1.

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ -0.147 & -0.289 & 0.436 \\ 0.615 & -0.51 & -0.100 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

The coefficients given below will produce gamma corrected RGB normalized to a range of ±1, when YUV have the ranges given above.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1.140 \\ 1 & -0.395 & -0.581 \\ 1 & 2.032 & 0 \end{bmatrix} \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

These coefficients translate to the following HEX values, which define the 12 bit number to be loaded. Note that these are given as simple three digit HEX values, without a separate 3 bit integer and 9 bit fractional part.

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} 099 & 12C & 03A \\ F64 & F6C & 0DF \\ 13A & EF8 & FCC \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 200 & 000 & 247 \\ 200 & F35 & ED6 \\ 200 & 410 & 000 \end{bmatrix} \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

If normalized digital UV components are required, the coefficients must be modified as given below. The NORM and BYPASS bits should then be set. The U I/O range is expanded to ±0.5, and the V I/O range is compressed to the same values. Y has an I/O range of 0 to 255. The 8 bit chrominance outputs now represent a range of ±0.5.

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ -0.169 & -0.331 & 0.500 \\ 0.5 & -0.419 & -0.081 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1.42 \\ 1 & -0.344 & -0.714 \\ 1 & 1.772 & 0 \end{bmatrix} \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

The equivalent HEX values which be loaded into the device are given below;

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} 099 & 12C & 03A \\ FA9 & F56 & 100 \\ 100 & F29 & FD6 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 200 & 000 & 2CD \\ 200 & F4F & E92 \\ 200 & 38B & 000 \end{bmatrix} \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

CONVERSION BETWEEN RGB AND YIQ

The coefficients for converting analog RGB to YIQ are given below. The gamma corrected RGB inputs have a range of 0 to 1. Analog I and Q have ranges of ±0.596 and ±0.525 respectively, and the NORM bit must be reset to produce 8 bit outputs representing a range of ±1. The BYPASS bit must be set.

$$\begin{bmatrix} Y \\ I \\ Q \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ 0.596 & -0.275 & -0.321 \\ 0.212 & -0.523 & 0.311 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

In the opposite direction the following coefficients produce gamma corrected RGB, when the YIQ inputs have the ranges given above.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0.956 & 0.620 \\ 1 & -0.272 & -0.647 \\ 1 & -1.108 & 1.705 \end{bmatrix} \begin{bmatrix} Y \\ I \\ Q \end{bmatrix}$$

In HEX these values become;

$$\begin{bmatrix} Y \\ I \\ Q \end{bmatrix} = \begin{bmatrix} 099 & 12C & 03A \\ 131 & F73 & F5B \\ 06C & EF4 & 09F \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 200 & 1E9 & 139 \\ 200 & F74 & EB4 \\ 200 & SDC8 & 368 \end{bmatrix} \begin{bmatrix} Y \\ I \\ Q \end{bmatrix}$$

The conversion between digital RGB and normalized digital YIQ requires the following coefficients. I and Q are then compressed to fall in the range of ±0.5, and the NORM bit must be set since the 8 bit chrominance outputs now represent ±0.5. The BYPASS bit must also be set.

$$\begin{bmatrix} Y \\ I \\ Q \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ 0.500 & -0.231 & -0.269 \\ 0.203 & -0.500 & 0.297 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 1.139 & 0.648 \\ 1 & -0.324 & -0.677 \\ 1 & -1.321 & 1.783 \end{bmatrix} \begin{bmatrix} Y \\ I \\ Q \end{bmatrix}$$

These correspond to the HEX coefficients gven below;

$$\begin{bmatrix} Y \\ I \\ Q \end{bmatrix} = \begin{bmatrix} 099 & 12C & 03A \\ 100 & F89 & F76 \\ 068 & F00 & 098 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

R		200	247	146		Y
G	=	200	F5A	EA5		I
B		200	D5B	391		Q

CONVERSION FROM Y Cr Cb TO RGB

The analog conversion matrix is given below;

R = Y + 1.402(Cr - 128)
G = Y - 0.714(Cr - 128) - 0.344(Cb - 128)
B = Y +1.772(Cb - 128)

If the Y Cr Cb ranges are all 1 to 254, then the RGB range produced will be 1 to 254. If the Y range is 16 to 235 and the Cr Cb ranges are 16 to 240, then the expected RGB range is 16 to 235. Incoming Y CR Cb data can be adjusted to either of these ranges by using the SEL bit in the Control Register. The input circuit also does the necessary subtraction of 128 from the Cr and Cb values (the BYPASS bit must be reset). The resulting HEX values which must be loaded into the coefficient store are given below;

C1	C2	C3		200	2CE	0
C4	C5	C6	=	200	E92	F50
C7	C8	C9		200	0	38B

The digital conversion matrix is given below;

R = Y + 1.37(Cr - 128)
G = Y - 0.698(Cr - 128) - 0.336(Cb - 128)
B Y + 1.73(Cb - 128)

The corresponding HEX values are given below;

C1	C2	C3		200	2BD	0
C4	C5	C6	=	200	E9B	F54
C7	C8	C9		200	0	376

The digital matrix only functions correctly when the Y range is 16 to 235 and the Cr Cb ranges are 16 to 240. The RGB range produced should then be 16 to 235. Both the SEL and BYPASS bits should thus be reset.

CONVERSION FROM RGB TO Y Cr Cb

The analog matrix is given below;

Y = 0.299R + 0.587G + 0.114B
Cr = 0.5R - 0.419G - 0.081B + 128
Cb = -0.169R - 0.331G + 0.5B + 128

This can handle RGB ranges of either 1 to 254 or 16 to 235. If necessary the RAM based look up tables can be used to limit the range of the incoming RGB. The BYPASS bit must always be reset, and the NORM bit set, when producing Cr and Cb data.

The SEL bit is used to limit the range of the YCr Cb values which are outputed. When SEL is set all three output ranges are 1 to 254. When it is reset the Y range is 16 to 235, and the Cr Cb ranges are 16 to 240. Values ouside the range limits will be forced to the correct maximum or minimum value. The offset of 128 is added to the Cr Cb values before the ranging is done.

The HEX values which correspond to the analog matrix are given below;

C1	C2	C3		99	12D	3A
C4	C5	C6	=	100	F29	FD7
C7	C8	C9		FA9	F57	100

In the CCIR601 specification the digital matrix is expressed as fractions of 256, and is given below;

Y = 77/256R + 150/256G + 29/256B
Cr = 131/256R - 110/256G - 21/256B + 128
Cb = -44/256R - 87/256G + 131/256B + 128

The HEX values which correspond to this digital matrix are given below;

C1	C2	C3		9A	12C	3A
C4	C5	C6	=	106	F24	FD6
C7	C8	C9		FA8	F52	106

This matrix expects the RGB inputs to be in the range of 16 to 235, and also the SEL bit to detemine the output range.

CONVERSION BETWEEN RGB AND Y,R-Y,AND B-Y

The analog matrices used to convert between RGB and Y Cr Cb can also be used with normalized colour difference information. The BYPASS bit must, however, be reset to avoid the 128 offset circuitry. RGB and Y inputs and outputs will have a range of 0 to 255. Colour difference inputs and outputs will have a range of -128 to +127 (±0.5). The NORM bit should always be set.

When working with analog colour difference values the following coefficients should be used, with the NORM bit reset. R - Y will have a range of ±0.701, and B - Y a range of ±0.886.

Y		0.299	0.587	0.114		R
R-Y	=	0.701	-0.587	-0.114		G
B-Y		-0.299	-0.587	0.886		B

R		1	1	0		Y
G	=	1	-0.509	-0.194		R-Y
B		1	0	1		B-Y

The corresponding HEX values are given below;

Y		099	12C	03A		R
R-Y	=	167	ED3	FC6		G
B-Y		F67	ED3	1C6		B

R		200	200	0		Y
G	=	200	EFB	F9D		R-Y
B		200	0	200		B-Y

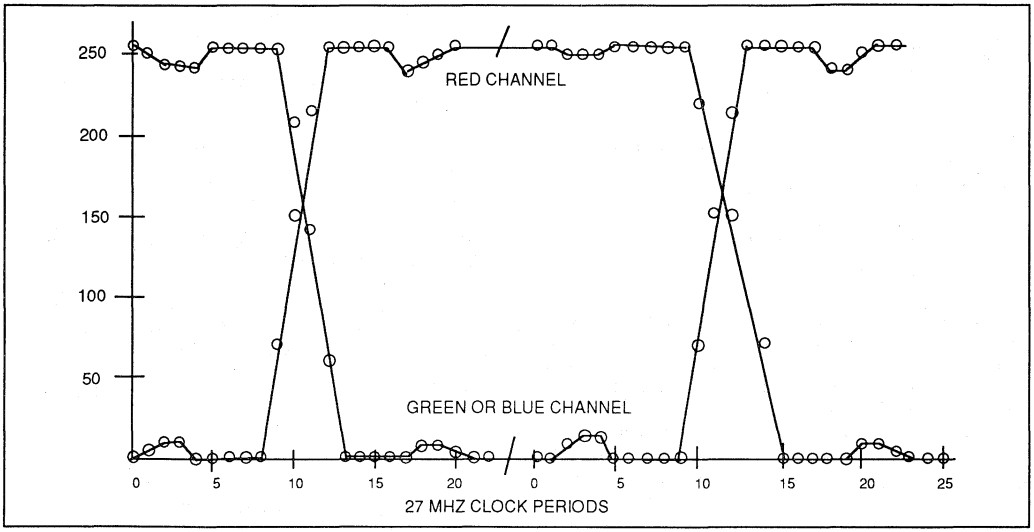


Figure 10. RGB Response to step changes in Y Cr Cb

RESPONSE TO INPUT STEP CHANGES

Figure 10 shows the actual response given by the RGB outputs to step changes in the Y Cr Cb inputs. Note that both negative undershoot and overshoot above 255 are prevented by the clipping circuit. The response of the Blue and Green filters will always be identical since they use identical circuits. The Red channel uses a different interpolating filter.

The Y Cr Cb changes were calculated to theoretically cause the RGB outputs to swing from maximum to minimum values, using the analog coefficients. Initial Y Cr Cb values were 151/20/43 with a step to 105/236/213. These should cause RGB to change from 0/255/0 to 255/0/255. The second transition was caused by changing the Y CR Cb values from 228/148/0 to 179/0/171. This should cause RGB to change from 255/255/0 to 0/255/255.

Figure 11 show the response of the Y Cr Cb outputs to maximum range step changes in RGB. The sequence used to cause the four transitions, and the theoretical results are given below.

	R	G	B	Y	Cr	Cb
Start	255	255	255	235	128	128
T1	255	255	0	226	149	16
T2	0	255	255	178	16	172
T3	0	255	0	148	21	44
T4	255	0	255	106	237	212

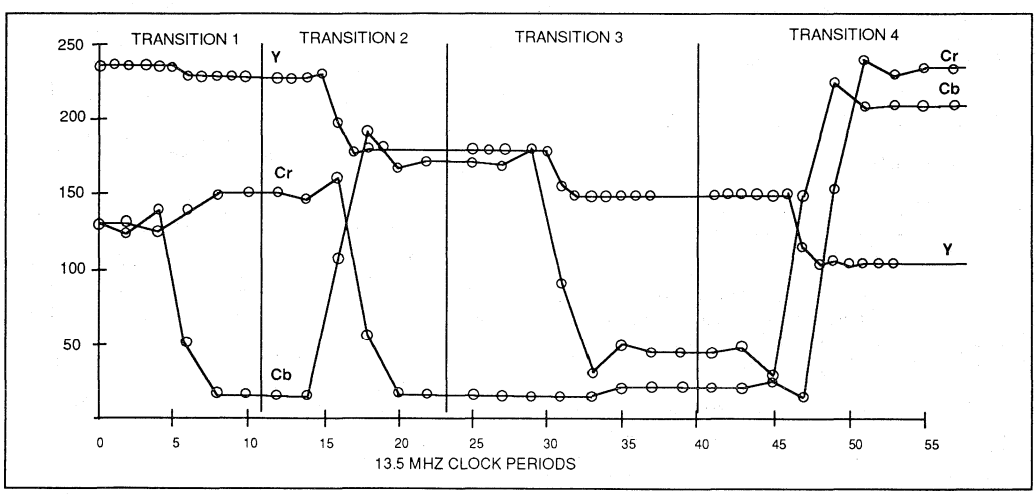


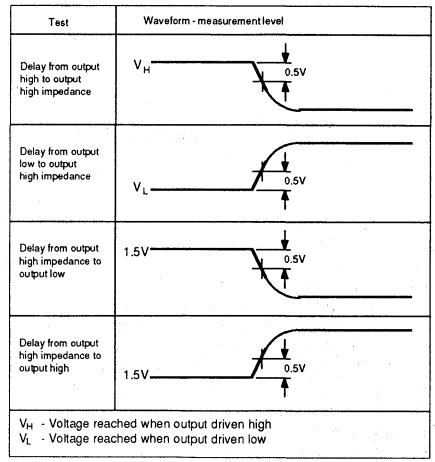
Figure 11. Y Cr Cb response to step changes in RGB

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage Vcc	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to Vcc + 0.5V
Output voltage V_{OUT}	-0.5V to Vcc + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HMB)	500V
Storage temperature T_S	-65°C to 150°C
Ambient temperature with power applied T_{AMB}	0°C to 70°C
Junction temperature	100°C
Package power dissipation	1000mW

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.



STATIC ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise stated)
Tamb = 0 C to +70°C Vcc = 5.0v ± 10%

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
Output high voltage	V_{OH}	3.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.0		-	V	3V for CLK
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{CC}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{CC}
Output S/C current	I_{SC}	10		300	mA	V_{CC} = Max

FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN
NC	1	R0	26	NC	51	C0	76
NC	2	GND	27	NC	52	NC	77
NC	3	NC	28	NC	53	GND	78
VDD	4	NC	29	VDD	54	NC	79
CLK	5	NC	30	Y7	55	NC	80
RES	6	VDD	31	Y6	56	VDD	81
GND	7	G7	32	NC	57	D7	82
OEN	8	G6	33	Y5	58	D6	83
GND	9	G5	34	NC	59	D5	84
FI	10	G4	35	Y4	60	D4	85
NC	11	G3	36	Y3	61	D3	86
HREF	12	G2	37	Y2	62	D2	87
FO	13	G1	38	Y1	63	D1	88
HDLY	14	G0	39	Y0	64	D0	89
CRI	15	GND	40	GND	65	GND	90
CRO	16	VDD	41	VDD	66	VDD	91
GND	17	B7	42	C7	67	A4	92
VDD	18	B6	43	C6	68	A3	93
R7	19	B5	44	C5	69	A2	94
R6	20	B4	45	C4	70	A1	95
R5	21	B3	46	C3	71	A0	96
R4	22	B2	47	C2	72	CS	97
R3	23	B1	48	NC	73	RD	98
R2	24	B0	49	C1	74	WR	99
R1	25	GND	50	NC	75	GND	100

Pin Out Diagram

VP5311A

NTSC/PAL DIGITAL VIDEO ENCODER

The VP5311 converts digital Y, Cr, Cb, data into analog NTSC/PAL composite video and S-video signals. The outputs are capable of driving doubly terminated 75 ohm loads with standard video levels.

The device accepts data inputs complying with CCIR Recommendation 601 and 656. The data is time multiplexed on an 8 bit bus at 27MHz and is formatted as Y, Cr, Y, Cb (i.e. 4:2:2). The video blanking and sync information from REC 656 is included in the data stream when the VP5311 is working in slave mode.

The output pixel rate is 27MHz and the input pixel rate is half this frequency, i.e. 13.5MHz.

All necessary synchronisation signals are generated internally when the device is operating in master mode. Digital horizontal and vertical sync outputs are available for use by the host system.

The rise and fall times of sync, burst envelope and video blanking are internally controlled to be within composite video specifications.

Three digital to analog converters (DACs) are used to convert the digital luminance, chrominance and composite data into true analog signals. An internally generated reference voltage provides the biasing for the DACs.

FEATURES

- Converts Y, Cr, Cb data to analog composite video and S-video
- Supports CCIR recommendations 601 and 656
- All digital video encoding
- Selectable master/slave mode for sync signals
- Switchable chrominance bandwidth
- Switchable pedestal with gain compensation
- SMPTE 170M NTSC or CCIR 624 PAL compatible outputs
- GENLOCK mode
- Line 21 Closed Caption encoding
- I²C bus serial microprocessor interface
- Supports Macrovision anti-taping format Rev. 6.

APPLICATIONS

- Digital Cable TV
- Digital Satellite TV
- Multi-media
- Video games
- Karaoke
- Digital VCRs

ORDERING INFORMATION

VP5311/CG/GP1R

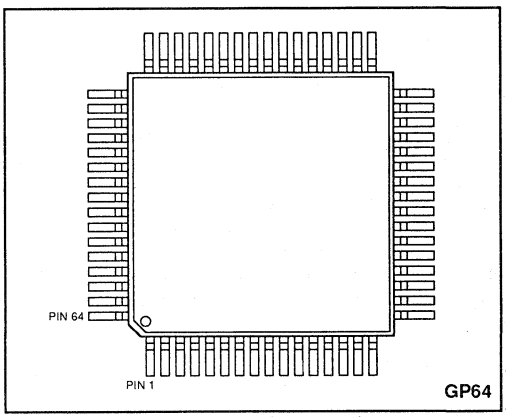


Fig.1 Pin connections (top view)

PIN	FUNCTION	PIN	FUNCTION
1	VDD	33	VDD
2	GND	34	$\overline{\text{RESET}}$
3	D0 (VS O/P)	35	REFSQ
4	D1 (HS O/P)	36	GND
5	D2 (FC0 O/P)	37	VDD
6	D3 (FC1 O/P)	38	GND
7	D4 (FC2 O/P)	39	PD7
8	D5	40	PD6
9	D6 (SCSYNC I/P)	41	PD5
10	D7 (PALID I/P)	42	PD4
11	GND	43	PD3
12	VDD	44	PD2
13	GND	45	PD1
14	GND	46	PD0
15	PXCK	47	GND
16	VDD	48	VDD
17	CLAMP	49	AGND
18	COMPSYNC	50	VREF
19	GND	51	DACGAIN
20	VDD	52	LUMACOMP
21	TDO	53	AVDD
22	TDI	54	LUMAOUT
23	TMS	55	AGND
24	TCK	56	COMPOUT
25	GND	57	AGND
26	SA1	58	CHROMAOUT
27	SA2	59	AVDD
28	SCL	60	COMPCOMP
29	VDD	61	N/C
30	SDA	62	AVDD
31	GND	63	AVDD
32	VDD	64	N/C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC CHARACTERISTICS

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Units
Digital Inputs TTL compatible (except SDA, SCL)						
Input high voltage		VIN	2.0			V
Input low voltage		VIL			0.8	V
Digital Inputs SDA, SCL						
Input high voltage		VIH	0.7 VDD			V
Input low voltage		VIL			0.3 VDD	V
Input high current	VIN = VDD	IIH			10	µA
Input low current	VIN = VSS	IIL			-10	µA
Digital Outputs CMOS compatible						
Output high voltage	IOH = -1mA	VOH	3.7			V
Output low voltage	IOL = +4mA	VOL			0.4	V
Digital Output SDA						
Output low voltage	IOL = +6mA	VOL			0.6	V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC CHARACTERISTICS DACs

Parameter	Symbol	Min.	Typ.	Max.	Units
Accuracy (each DAC)					
Integral linearity error	INL			±1.5	LSB
Diffential linearity error	DNL			±1	LSB
DAC matching error				±5	%
Monotonicity			guaranteed		
LSB size			66.83		µA
Internal reference voltage	V_{REF}	0.95	1.00	1.05	V
Internal reference voltage output impedance	Z_R		27k		Ω
Reference Current (V_{REF}/R_{REF}) R_{REF} = 730Ω	I_{REF}		1.3699		mA
DAC Gain Factor (V_{OUT} = K_{DAC} x IREF x R_L), V_{OUT} = DAC code 511	K_{DAC}		24.93		
Peak Glitch Energy (see fig.3)			50		pV-s
CVBS, Y and C - NTSC (pedestal enabled)					
Maximum output, relative to sync bottom			33.75		mA
White level relative to black level			17.64		mA
Black level relative to blank level			1.40		mA
Blank level relative to sync level			7.62		mA
Colour burst peak - peak			7.62		mA
DC offset (bottom sync)			0.40		mA
CVBS, Y and C - PAL					
Maximum output			34.15		mA
White level relative to black level			18.71		mA
White level relative to sync level			26.73		mA
Black level relative to sync level			8.02		mA
Colour burst peak - peak			8.02		mA
DC offset (bottom sync)			0.00		mA

Note: All figures are for: R_{REF} = 730Ω R_L = 37.5Ω. When the device is set up in NTSC mode there is a +0.25% error in the PAL levels. If R_L = 75Ω then R_{REF} = 1460Ω.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	VDD, AVDD	-0·3 to 7·0V
Voltage on any non power pin		-0·3 to VDD+0·3V
Ambient operating temperature		0 to 70°C
Storage temperature		-55°C to 150°C

Note: Stresses exceeding these listed under Absolute Maximum Ratings may induce failure. Exposure to Absolute Maximum Ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply voltage	VDD, AVDD	4.75	5.00	5.25	V
Power supply current (including analog outputs)	IDD		150		mA
Input clock frequency	PXCK	-50ppm	27.00	+50ppm	MHz
SCL clock frequency	fSCL			500	kHz
Analog video output load			37.5		Ω
DAC gain resistor			730		Ω
Ambient operating temperature		0		70	°C

VIDEO CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units
Luminance bandwidth			5.5		MHz
Chrominance bandwidth (Extended B/w mode)			1.3		MHz
Chrominance bandwidth (Reduced B/w mode)			650		kHz
Burst frequency (NTSC)			3.57954545		MHz
Burst frequency (PAL-B, D,G,H,I)			4.43361875		MHz
Burst frequency (PAL-M)			3.57561189		MHz
Burst frequency (PAL-N Argentina)			3.58205625		MHz
Burst cycles (NTSC and PAL-M,N)			9		Fsc cycles
Burst cycles (NTSC and PAL-B, D, G, H,I)			10		Fsc cycles
Burst envelope rise / fall time (NTSC and PAL-M,N)			300		ns
Burst envelope rise / fall time (NTSC and PAL-B, D, G, H,I)			300		ns
Analog video sync rise / fall time (NTSC and PAL-M,N)			145		ns
Analog video blank rise / fall time (NTSC and PAL-B, D, G, H,I)			245		ns
Differential gain			1.5		% pk-pk
Differential phase			TBD		° pk-pk
Signal to noise ratio (unmodulated ramp)			-61	-61	dB
Chroma AM signal to noise ratio (100% red field)			-56	-56	dB
Chroma PM signal to noise ratio (100% red field)			-58	-58	dB
Hue accuracy				2.5	%
Colour saturation accuracy				2.5	%
Residual sub carrier			-60		dB
Luminance / chrominance delay			10		ns

ESD COMPLIANCE

Pins	Test	Test Levels	Notes
All pins	Human body model	2kV on 100pF through 1k5Ω	Meets Mil-Std-883 Class 2
All pins	Machine model	200V on 200pF through 0Ω & 500nH	

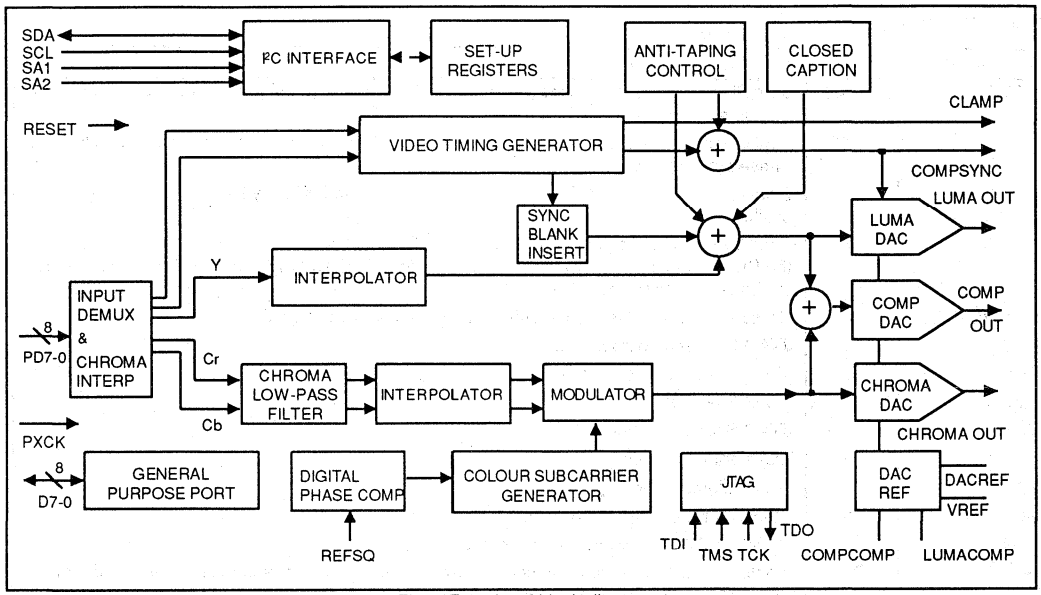


Fig.2 Functional block diagram

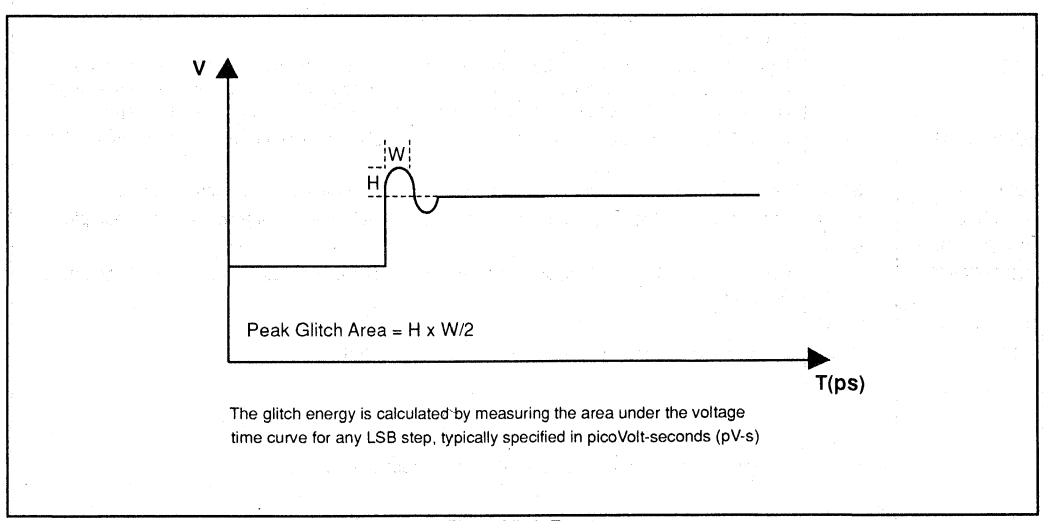


Fig.3 Glitch Energy

PIN DESCRIPTIONS

Pin Name	Pin No.	Description
PD0-7	39 - 46	8 Bit Pixel Data inputs clocked by PXCK. PD0 is the least significant bit, corresponding to Pin 46. These pins are internally pulled low.
D0-7	3 - 10	8 Bit General Purpose Port input/output. D0 is the least significant bit, corresponding to Pin 3. These pins are internally pulled low.
PXCK	15	27MHz Pixel Clock input. The VP5311 internally divides PXCK by two to provide the pixel clock.
CLAMP	17	The CLAMP output signal is synchronised to COMPSYNC output and indicates the position of the BURST pulse, (lines 10-263 and 273-525 for NTSC and PAL-M; lines 6-310 and 319-623 for PAL-B,D, G,I,N(Argentina)).
COMPSYNC	18	Composite sync pulse output. This is an active low output signal.
TDO	21	JTAG Data scan output port.
TDI	22	JTAG Data scan input port.
TMS	23	JTAG Scan select input.
TCK	24	JTAG Scan clock input.
SA1	26	Slave address select.
SA2	27	Slave address select.
SCL	28	Standard I²C bus serial clock input.
SDA	30	Standard I²C bus serial data input/output.
$\overline{\text{RESET}}$	34	Master reset. This is an asynchronous, active low, input signal and must be asserted for a minimum 200ns in order to reset the VP5311.
REFSQ	35	Reference square wave input used only during Genlock mode.
VREF	50	Voltage reference output. This output is nominally 1·0V and should be decoupled with a 100nF capacitor to GND.
DAC GAIN	51	DAC full scale current control. A resistor connected between this pin and GND sets the magnitude of the video output current. An internal loop amplifier controls a reference current flowing through this resistor so that the voltage across it is equal to the Vref voltage.
LUMACOMP	52	Luma DAC compensation. A 100nF ceramic capacitor must be connected between pin 52 and pin 53.
LUMAOUT	54	True luminance, composite and chrominance video signal outputs. These are high impedance current source outputs. A DC path to GND must exist from each of these pins.
COMPOUT	56	
CHROMAOUT	58	
COMPCOMP	60	Composite DAC compensation. A 100nF ceramic capacitor must be connected between pin 60 and pin 59.
NOT USED	61, 64	
VDD	1, 12, 16, 20, 29, 32, 33, 37, 48	Positive supply input. All VDD pins must be connected.
AVDD	53, 59 62, 63	Analog positive supply input. All AVDD pins must be connected.
GND	2, 11, 13, 14, 19, 25, 31, 36, 38, 47	Negative supply input. All GND pins must be connected.
AGND	49, 55, 57	Negative supply input. All AGND pins must be connected.

All other pins are N/C and should not be connected.

REGISTERS MAP

See Register Details for further explanations.

ADDRESS hex	REGISTER NAME	7	6	5	4	3	2	1	0	R/W	DEFAULT hex
	BAR	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	W	
00	PART ID2	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	R	13
01	PART ID1	ID0F	ID0E	ID0D	ID0C	ID0B	ID0A	ID09	ID08	R	66
02	PART ID0	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00	R	57
03	REV ID	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	R	04
04	GCR	-	-	YCDELAY	RAMPEN	-	-	VFS1	VFS0	R/W	00
05	VOCR	-	CLAMPDIS	CHRBW	SYNCDIS	BURDIS	LUMDIS	CHRDIS	PEDEN	R/W	00
06	HANC	-	-	DFI2	DFI1	DFI0	Reserved	Reserved	ACTREN	*	00
07	ANCID	AN7	AN6	AN5	AN4	AN3	AN2	AN1	PARITY	R/W	00
08	SC_ADJ	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	R/W	97
09	FREQ2	FR17	FR16	FR15	FR14	FR13	FR12	FR11	FR10	R/W	87
0A	FREQ1	FR0F	FR0E	FR0D	FR0C	FR0B	FR0A	FR09	FR08	R/W	C1
0B	FREQ0	FR07	FR06	FR05	FR04	FR03	FR02	FR01	FR00	R/W	F1
0C	SCHPHM	-	-	-	-	-	-	-	SCH8	R/W	00
0D	SCHPHL	SCH7	SCH6	SCH5	SCH4	SCH3	SCH2	SCH1	SCH0	R/W	00
0E to 1F	Reserved										
20	GPPCTL	CTL7	CTL6	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	W	FF
21	GPPRD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	R	-
22	GPPWR	WR7	WR6	WR5	WR4	WR3	WR2	WR1	WR0	W	00
23 to EF	Not used										
F0	CCREG1	-	F1W1D6	F1W1D5	F1W1D4	F1W1D3	F1W1D2	F1W1D1	F1W1D0	R/W	00
F1	CCREG2	-	F1W2D6	F1W2D5	F1W2D4	F1W2D3	F1W2D2	F1W2D1	F1W2D0	R/W	00
F2	CCREG3	-	F2W1D6	F2W1D5	F2W1D4	F2W1D3	F2W1D2	F2W1D1	F2W1D0	R/W	00
F3	CCREG4	-	F2W2D6	F2W2D5	F2W2D4	F2W2D3	F2W2D2	F2W2D1	F2W2D0	R/W	00
F4	CC_CTL	-	-	-	-	F2ST	F1ST	F2EN	F1EN	R/W	00
F8	HSOFFL	HSOFF7	HSOFF6	HSOFF5	HSOFF4	HSOFF3	HSOFF2	HSOFF1	HSOFF0	R/W	7E
F9	HSOFFM	-	-	-	-	-	-	HSOFF9	HSOFF8	R/W	00
FD	GPSDAC	-	-	LUMADIS	CHRMDIS		LUMCHKI	CHRCKHI	CMPCKHI	R/W	38
FE	GPSTST	PROGRESS	BISTO	DIGSH	TSTBLEV	STSYNCLO	-	CTRLC_1	CTRLC_0	R/W	00
FF	GPSCTL	FSC4SEL	GENDITH	GENLKEN	NOLOCK	PALIDEN	TSURST	CHRMCLIP	TRSEL	R/W	00

Table.1 Register map

NOTE * For register HANC, bits 3, 4 and 5 are read only. Bits 1 and 2 are reserved. N/A = not applicable.

Standard	Lines/ field	Field freq. HZ	Number of pixels/line at 27MHz	Horizontal freq. kHz. f_H	Subcarrier freq. kHz. f_{SC}	f_{SC}/f_H	SC_ADJ register hex	FREQ2-0 registers hex
NTSC (default)	525	59.94	1716	15.734266	3.57954545	(455/2)	xx	87 C1 F1
PAL-B, G, H, I	625	50	1728	15.625000	4.43361875	(1135/4+1/625)	9C	A8 26 2B
PAL-M	525	59.94	1716	15.734266	3.57561189	(909/4)	xx	87 9B C0
PAL-N (Argentina)	625	50	1728	15.625000	3.58205625	(917/4+1/625)	57	87 DA 51

Table.2 Line, field and subcarrier standards and register settings

xx = don't care.

The calculation of the FREQ register value is according to the following formula:-

$$FREQ = 2^{26} \times f_{SC}/f_{SC}/PXCK \text{ hex, where } PXCK = 27.00MHz$$

Both NTSC and PAL-M values are rounded UP from the decimal number. PAL-B, D, G, H, I and N (Argentina) are rounded DOWN. The SC_ADJ value is derived from the adjustment needed to be added after 8 fields to ensure accuracy of the Subcarrier frequency. Note the SC_ADJ value of 9C required for PAL-B, D, G, H, I, is different to the default state of the register.

REGISTER DETAILS

BAR — **Base register**
RA7-0 — Register address.

PART ID 2-0 — **Part number**
ID17-00 — Chip part identification (ID) number.

REV ID — **Revision number**
REV7-0 — Chip revision ID number.

GCR — **Global Control**
YCDELAY — Luma to Chroma delay.
High = 37ns luma delay, this may be used to compensate for group delay in external filters.
Low = normal operation (default).

RAMPEN — Modulated ramp enable.
High = ramp output for differential phase and gain measurements. A 27MHz clock must be applied to PXCK pin.
Low = normal operation (default).

VFS1-0 — Video format select

VFS1	VFS0	
0	0	NTSC (default)
0	1	PAL-B, D, G,H,I,N(Argentina)
1	0	PAL-M
1	1	Reserved

VOCR — **Video Output Control**
CLAMPDIS — High = Clamp signal disable
Low = normal operation with clamp signal enabled (default).

CHRBW — Chroma bandwidth select.
High = ±1·3MHz.
Low = ±650kHz (default)

SYNCDIS — High = Sync disable (in composite video signal). COMPSYNC is not affected.
Low = normal operation with sync enabled (default).

BURDIS — High = Chroma burst disable.
Low = normal operation, with burst enabled (default).

LUMDIS — High = Luma input disable - force black level with synchronisation pulses maintained.
Low = normal operation, with Luma input enabled (default).

CHRDIS — High = Chroma input disable - force monochrome.
Low = normal operation, with Chroma input enabled (default).

PEDEN — High = Pedestal (set-up) enable a 7·5 IRE pedestal on lines 23-262 and 286-525. Valid for NTSC/PAL-M only

HANC — **Horizontal Ancillary Data Control**
DFI2-0(read only) — Digital Field Identification, 000=Field1
ANCTREN — Ancillary timing reference enable. When High use FIELD COUNT from ancillary data stream. When low, data is ignored.

ANCID — **Ancillary data ID**
AN7-1 — Ancillary data ID
AN0 — Parity bit (odd)
Only ancillary data in REC 656 data stream with the same ID as this byte will be decoded by the VP5311 to produce H and V synchronisation and FIELD COUNT.

SC_ADJ — **Sub Carrier Adjust**
SC7-0 — Sub carrier frequency seed value, see table 2.

FREQ2-0 — **Sub carrier frequency**
FR17-00 — 24 bit Sub carrier frequency programmed via I²C bus, see table 2. FREQ2 is the most significant byte (MSB).

SCHPHM-L — **Sub carrier phase offset**
SCH9-0 — 9 bit Sub carrier phase relative to the 50% point of the leading edge of the horizontal part of composite sync. SCHPHM bit 0 is the MSB. The nominal value is zero. This register is used to compensate for delays external to the VP5311.

GPPCTL — **General purpose port control**
CTL7-0 — Each bit controls port direction
Low = output High = input

GPPRD — **General purpose port read data**
RD7-0 — I²C bus read from general purpose port (only INPUTS defined in GPPCTL)

GPPWR — **General purpose port write data**
WR7-0 — I²C bus write to general purpose port (only OUTPUTS defined in GPPCTL)

CCREG1 — **Closed Caption register 1**
F1W1D6-0 — Field one (line 21), first data byte

CCREG2 — **Closed Caption register 2**
F1W2D6-0 — Field one (line 21), second data byte

CCREG3 — **Closed Caption register 3**
F2W2D6-0 — Field two (line 284), first data byte

CCREG4 — **Closed Caption register 4**
F2W2D6-0 — Field two (line 284), second data byte

CCCTL — **Closed Caption control register**
F1ST — Field one (line 21) status
High = data has been encoded
Low = new data has been loaded to CCREG1-2

F2ST — Field two (line 284) status
High = data has been encoded
Low = new data has been loaded to CCREG3-4

F1EN — Closed Caption field one (line 21)
High = enable Low = disable (default)

F2EN — Closed Caption field two (line 284)
High = enable Low = disable (default)

HSOFFM-L
HSOFF9-0 — **HS offset**
This is a 10 bit number which allows the user to offset the start of digital data input with reference to the pulse HS.

GPSDAC
LUMADIS — **DAC test register**
1 = Normal operation
0 = Luma DAC input set zero

CHRMDIS — 1 = Normal operation
0 = Chroma DAC input set zero

LUMCKHI — 1 = Luma DAC clock input set to '1'

CHRCKHI — 0 = Normal operation
1 = Chroma DAC clock input set to '1'

GPSCTL
FSC4SEL — **GPS Control**
When high, REFSQ = 4xFSC and GPP bit D6 is forced to become an input for a SCSYNC signal (high = reset), which provides a synchronous phase reset for FSC divider. Low = normal operation with REFSQ = 1xFSC. (default).

GENDITH — 1 = Gen lock dither added.

GENLKEN — High = enable Genlock to REFSQ signal input.
Low = internal subcarrier generation (default).

NOLOCK — Genlock status bit (read only)
Low = Genlocked.
High = cannot lock to REFSQ. This bit is cleared by reading and set again if lock cannot be attained.

PALIDEN — High = enable external PAL ID phase control and GPP bit D7 is forced to become an input for PAL ID switch signal, (GPP bit D7 - Low = +135°, High = -135°).
Low = normal operation, internal PAL ID phase switch is used (default).

TSURST — High = chip soft reset. Registers are NOT reset to default values.
Low = normal operation (default).

CHRMCLIP — High = enable clipping of chroma data when luma goes below black level and is clipped.
Low = no chroma clipping (default).

TRSEL — High = master mode, GPP bits D0 - 4 are forced to become a video timing port with VS, HS and FIELD outputs.
Low = slave mode, timing from REC656.

I²C BUS CONTROL INTERFACE

I²C bus address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
0	0	0	1	1	SA2	SA1	X

The serial microprocessor interface is via the bi-directional port consisting of a data (SDA) and a clock (SCL) line. It is compatible to the Philips I²C bus standard (Jan. 1992 publication number 9398 393 40011). The interface is a slave transmitter - receiver with a sub-address capability. All communication is controlled by the microprocessor. The SCL line is input only. The most significant bit (MSB) is sent first. Data must be stable during SCL high periods.

A bus free state is indicated by both SDA and SCL lines being high. START of transmission is indicated by SDA being pulled low while SCL is high. The end of transmission, referred to as a STOP, is indicated by SDA going from low to high while SCL is high. The STOP state can be omitted if a repeated START is sent after the acknowledge bit. The reading device acknowledges each byte by pulling the SDA line low on the ninth clock pulse, after which the SDA line is released to allow the transmitting device access to the bus.

The device address can be partially programmed by the setting of the pins SA1 and SA2. This allows the device to respond to one of four addresses, providing for system flexibility. The I²C bus address is seven bits long with the last bit indicating read / $\overline{\text{write}}$ for subsequent bytes.

The first data byte sent after the device address, is the sub-address - BAR (base address register). The next byte will be written to the register addressed by BAR and subsequent bytes to the succeeding registers. The BAR maintains its data after a STOP signal.

NTSC/PAL Video Standards

Both NTSC (4-field, 525 lines) and PAL (8-field, 625 lines) video standards are supported by the VP5311. All raster synchronisation, colour sub-carrier and burst characteristics are adapted to the standard selected. The VP5311 generates outputs which follow the requirements of SMPTE 170M and CCIR 624 for PAL signals.

The device supports the following:
NTSC,
PAL B, D, G, H, I, N (Argentina) and M.

Video Blanking

The VP5311 automatically performs standard composite video blanking. Lines 1-9, 264-272 inclusive, as well as the last half of line 263 are blanked in NTSC mode. In PAL mode,

lines 1-5, 311-318, 624-625 inclusive, as well as the last half of line 623 are blanked.

The V bit within REC656 defines the video blanking when TRSEL (bit 0 of GPSCTL register) is set low. When in MASTER mode with TRSEL set high the video encoder is still enabled. Therefore if these lines are required to be blank they must have no video signal input.

Interpolator

The luminance and chrominance data are separately passed through interpolating filters to produce output sampling rates double that of the incoming pixel rate. This reduces the sinx/x distortion that is inherent in the digital to analog converters and also simplifies the analog reconstruction filter requirements.

Digital to Analog Converters

The VP5311 contained three 9 bit digital to analog converters which produce the analog video signals. The DACs use a current steering architecture in which bit currents are routed to one of two outputs; thus the DAC has true and complementary outputs. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed. An on-chip voltage reference of 1.0V (typ.) provides the necessary biasing. However, the VP5311 may be used in applications where an external 1V reference is provided on the VREF pin, to adjust the video levels. In this case, the external reference should be temperature compensated and provide a low impedance output.

The full-scale output currents of the DACs is set by external 730Ω resistor between the DACGAIN and VSS pins. An on-chip loop amplifier stabilises the full-scale output current against temperature and power supply variations.

The analog outputs of the VP5311 are capable of directly driving doubly terminated 75Ω load then the DACGAIN resistor is simply doubled.

Luminance, Chrominance and Composite Video Outputs

The Luminance video output (LUMAOUT pin 54) drives a 37.5Ω load at 1.0V, sync tip to peak white. It contains only the luminance content of the image plus the composite sync pulses. In the NTSC mode, a set-up level offset can be added during the active video portion of the raster.

The Chrominance video output (CHROMAOUT pin 58) drives a 37.5Ω load at levels proportional in amplitude to the luma output (40 IRE pk-pk burst). This output has a fixed offset current which will produce approximately a 0.5V DC bias across the 37.5Ω load. Burst is injected with the appropriate timing relative to the luma signal.

The composite video output (COMPOUT pin 56) will also drive a 37.5Ω loas at 1.0V, sync tip to peak white. It contains both the luminance and chrominance content of the signal plus the composite sync pulses.

Output sinx/x compensation filters are required on all video output, as shown in the typical application diagram, see figs. 8 & 9.

Video Timing - Slave sync mode

The VP5311 has an internal timing generator which produces video timing signals appropriate to the mode of operation. In the default (power up) slave mode, all timing signals are derived from the input clock, PXCK, which must be derived from a crystal controlled oscillator. Input pixel data is latched on the rising edge of the PXCK clock.

The video timing generator produces the internal blanking and burst gate pulses, together with the composite sync output signal, using timing data (TRS codes) from the Ancillary data stream in the REC656 input signal, (when TRSEL (bit 0 of GPSCTL register) is set low).

Video Timing - Master sync mode

When TRSEL (bit 0 of GPSCTL register) is set high, the VP5311 operates in a MASTER sync mode, all REC656 timing reference codes are ignored and GPP bits D0 - 4 become a video timing port with VS, HS and FIELD outputs. The PXCK signal is, however, still used to generate all internal clocks. When TRSEL is set high, the direction setting of bits 4 - 0 of the GPPCTL register is ignored.

VS is the start of the field sync datum in the middle of the equalisation pulses. HS is the line sync which is used by the preceding MPEG2 decoder to define when to output digital video data to the VP5311. The position of the falling edge of HS relative to the first data Cb0, can be programmed in HSOFFM-L registers, see fig. 4.

HS offset

The position of the falling edge of HS relative to the first data Cb0, can be programmed in HSOFFM-L registers, see figure 4, this is called the pipeline delay and may need adjusting for a particular application. This is done by programming a 10 bit number called HSOFF into the HSOFFM and HSOFFL registers, HSOFFM being the most significant two bits and HSOFFL the least significant eight bits. A default value of 07EH is held in the registers.

The value to program into HSOFF can be looked up in tables 3 &4:

Nck	HSOFF	Comment
0 to 120	126 to 6	HS normal (64 cks)
121 to 138	863 to 801	HS pulse shortened*
184 to 857	800 to 127	HS normal (64 cks)

Table.3 for NTSC and PAL-M

Nck	HSOFF	Comment
0 to 131	137 to 6	HS normal (64 cks)
132 to 194	869 to 807	HS pulse shortened*
195 to 863	806 to 138	HS normal (64 cks)

Table.4 for PAL-B, D, G, H, I, N

where Nck = number of 13.5MHz clock cycles between the falling edge of HS and Cb0 (first data I/P on PD7-0) see fig. 4. Decreasing HSOFF advances the HS pulse (numbers are in decimal).

*HS pulse shortened means that the width of the pulse will be less than the normal 64 13.5MHz clock cycles.

The interruption in the sequence of values is because the HS signal is jumping across a line boundary to the previous line as the offset is increased. The register default value is 7EH and this sets Nck to 0, ie. the HS negative edge and Cb0 are co-incident in NTSC mode.

Genlock using REFSQ input

The VP5311 can be Genlocked to another video source by setting GENLKEN high (in GPSCTL register) and feeding a phase coherent sub carrier frequency signal into REFSQ. Under normal circumstances, REFSQ will be the same frequency as the sub carrier. But by setting FSC4SEL high (in GPSCTL register), a 4 x sub carrier frequency signal may be input to REFSQ. In this case, the Genlock circuit can be reset to the required phase of REFSQ, by supplying a pulse to SCSYNC (pin 9). The frequency of SCSYNC can be at sub carrier frequency, but once per line, or once per field could be adequate, depending on the application. When GENLKEN is set high, the direction setting of bit 6 in the GPPCTL register is igonred.

PALID Input

When in Genlock mode with GENLKEN set high (in GPSCTL register), the VP5311 requires a PAL phase identification signal, to define the correct phase on every line. This is supplied to PALID input (pin 10), High = -135° and low = +135°. The signal is asynchronous and should be changed before the sub carrier burst signal. PALID input is enabled by setting PALIDEN high (in GPSCTL register). When GENLKEN is high, the direction setting of bit 7 of the GPPCTL register is ignored

Master Reset

The VP5311 must be initialised with the $\overline{\text{RESET}}$ pin 34. This is an asynchronous active low signal and must be active for a minimum of 200ns in order for the VP5311 to be reset. The device resets to line 64, start of horizontal sync (i.e. line blanking active). There is no on-chip power on reset circuitry.

Line 21 coding

Two bytes of data are coded on the line 21 of each field, see figure 7. In the NTSC Closed Caption service, the default state is to code on line 21 of field one only. An additional service can also be provided using line 21 (284) of the second field. The data is coded as NRZ with odd parity, after a clock run-in and framing code. The clock run-in frequency = 0.5034965MHz which is related to the nominal line period, D = H / 32.

$$D = 63.55555556 / 32\mu s$$

Two data bytes per field are loaded via I2C bus registers CCREG1-4. Each field can be independently enabled by programming the enable bits in the control register (CC_CTL). The data is cleared to zero in the Closed Caption shift registers after it has been encoded by the VP5311. A software read of the field count in register HANC should be made to ensure it has incremented by 2 before sending the next pair of data bytes. Otherwise, the existing Closed Caption data output could be overwritten. If a transmission slot is missed it (ie. no data received) the encoder will send Null characters. Null characters are invisible to a closed caption reciever. The MSB (bit 7) is the parity bit and is automatically added by the encoder.

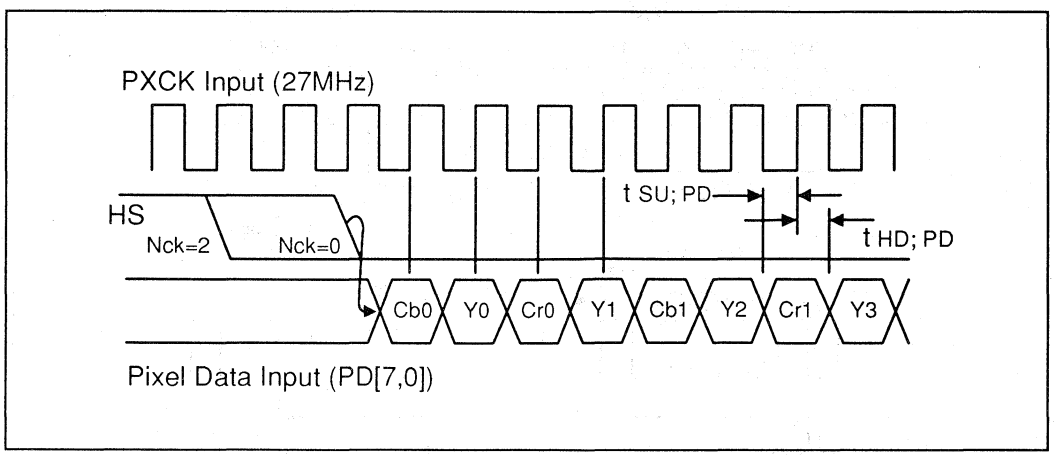


Fig.4 REC 656 interface with HS output timing

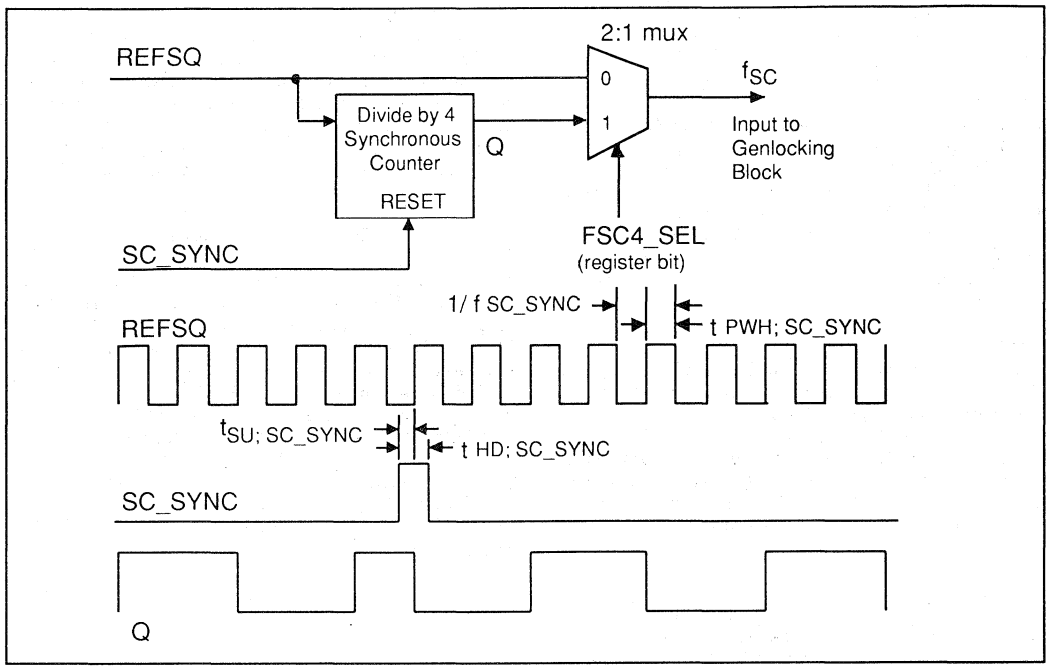


Fig.5 REFSQ and SC_SYNC input timing

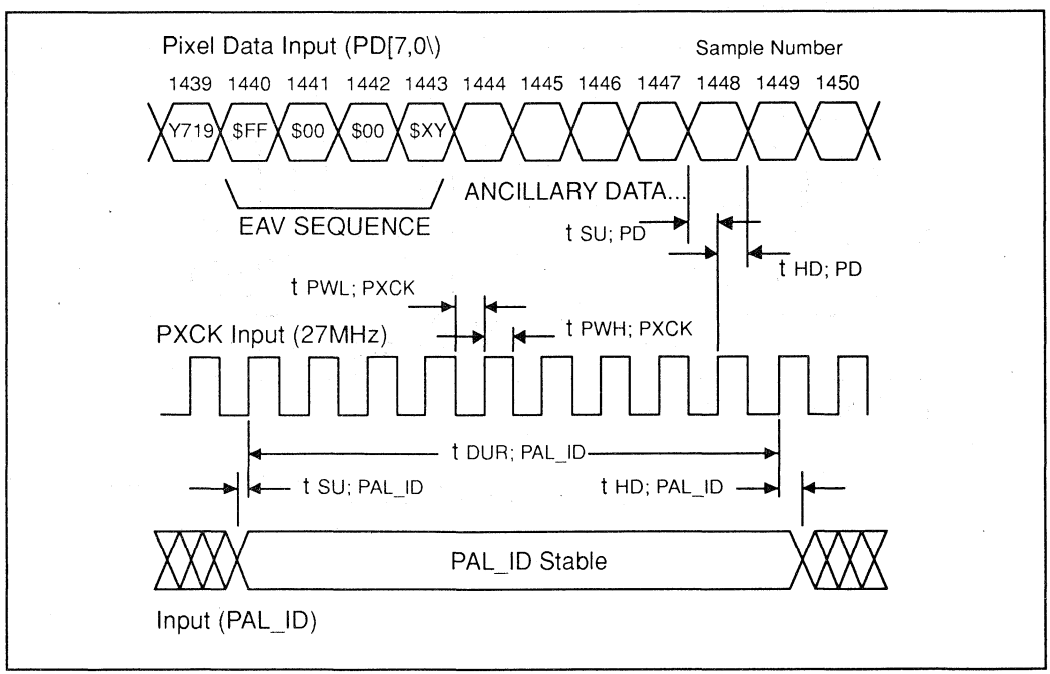


Fig.6 PAL_ID input timing

TIMING INFORMATION

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Units
Master clock frequency (PXCK input)		f_{PXCK}		27.0		MHz
PXCX pulse width, HIGH		$t_{PWH;\ PXCK}$	10			ns
PXCX pulse width, LOW		$t_{PWL;\ PXCK}$	14.5			ns
PXCX rise time	10% to 90% points	t_{RP}			TBD	ns
PXCX fall time	90% to 10% points	t_{FP}			TBD	ns
PD7-0 set up time		$t_{SU;PD}$	10			ns
PD7-0 hold time		$t_{HD;PD}$	5			ns
SC_SYNC set up time		$t_{SU;SC\_SYNC}$	10			ns
SC_SYNC hold time		$t_{HD;SC\_SYNC}$	0			ns
PAL_ID set up time		$t_{SU;PAL\_ID}$	10			ns
PAL_ID hold time		$t_{HD;PAL\_ID}$	0			ns
PAL_ID duration		$t_{DUR;PAL\_ID}$	9			PXCX periods
Output delay	PXCK to COMPSYNC PXCK to CLAMP	t_{DOS}			25	ns

Note: Timing reference points are at the 50% level. Digital C_{LOAD} <40pF.

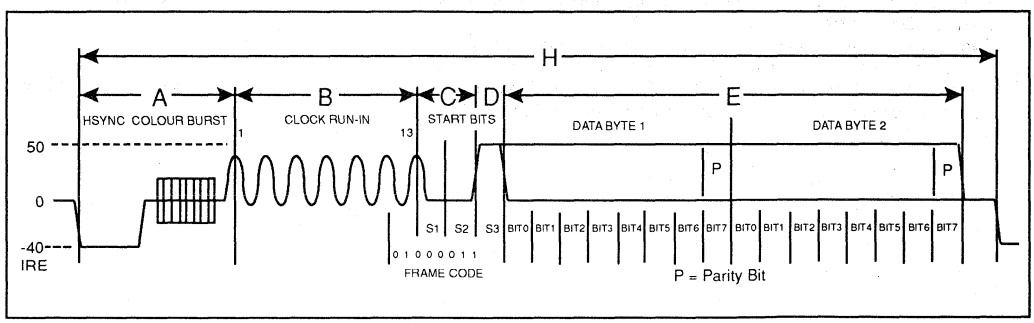


Fig.7 Closed Capation format

Interval	Description	Encoder minimum	Encoder nominal	Encoder maximum
A	H-sync to clock run-in	10.250µs	10.500µs	10.750µs
B	Clock run-in[2, 3]		6.5D (12.910µs)	
C	Clock run-in to third start bit[3]		2.0D (3.972µs)	
D	Data bit[1, 3]		1.0D (1.986µs)	
E	Data characters[4]		16.0D (31.778µs)	
H	Horizontal line[1]		32.0D (63.556)	
	Rise / fall time of data bit transitions[5]		0.240µs	0.288µs
	Data bit high (logic level one)[6] Clock run-in maximum	48 IRE	50 IRE	52 IRE
	Data bit low (logic level zero)[6] Clock run-in minimum	0 IRE	0 IRE	2 IRE
	Data bit differential (high - low) Clock run-in differential (max. - min)	48 IRE	50 IRE	52 IRE

Table. 5 Closed Caption data timing. (source EIA R - 4.3 Sept 16 1992)

Notes

1. The Horizontal line frequency f_H is nominally 15734.26Hz ±0.05Hz. Interval D shall be adjusted to $D = 1/(f_H \times 32)$ for the instantaneous f_H at line 21.
2. The clock run-in signal consists of 7.0 cycles of a 0.5034965MHz (1/D) sine wave when measured from the leading to trailing 0 IRE points. The sine wave is to be symmetrical about the 25 IRE level.
3. The negative going midpoints (half amplitude) of the clock run-in shall be coherent with the midpoints (half amplitude) of the Start and Data bit transitions.
4. Two characters, each consisting of 7 data bits and 1 odd parity bit.
5. 2 T Bar, measured between the 10% and 90% amplitude points.
6. The clock run-in maximum level shall not differ from the data bit high level by more than ±1 IRE. The clock run-in minimum level shall not differ from the data bit low level by more than ±1 IRE.

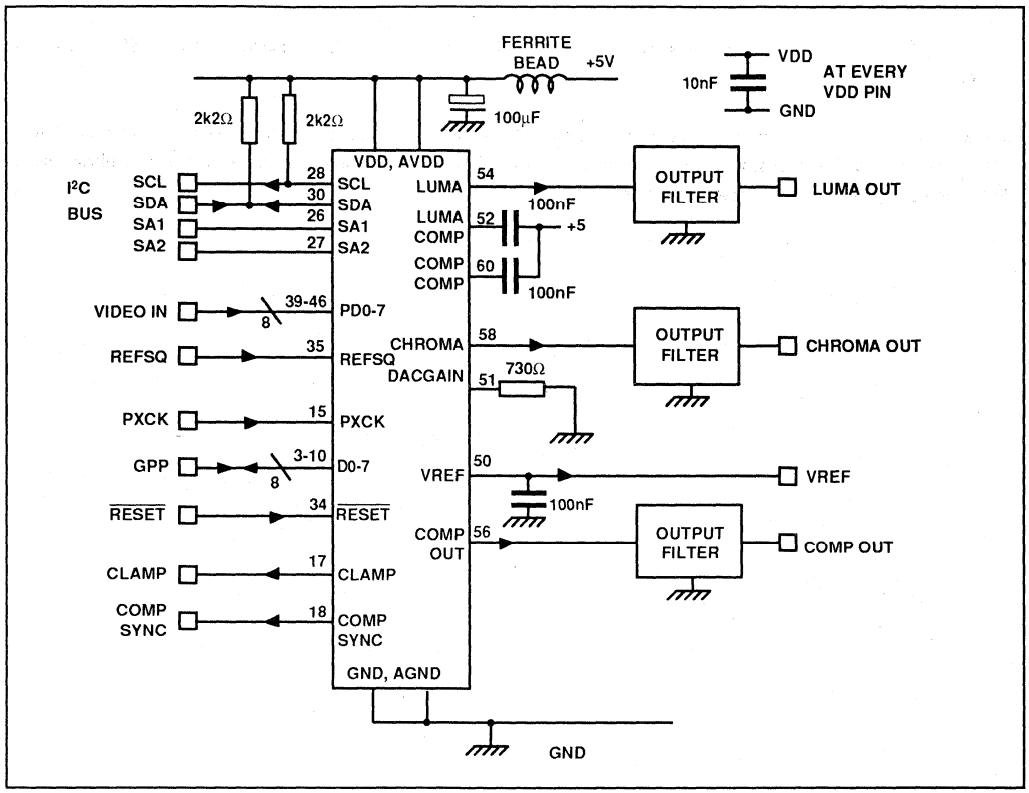


Fig.8 Typical application diagram, SLAVE mode. (Output filter - see Fig.9)

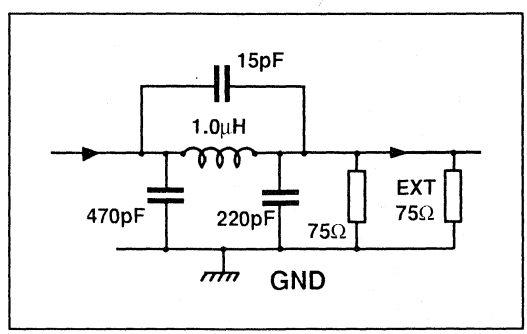


Fig.9 Output reconstruction filter

Note:
The VP5311 is only available to customers with a valid and existing authorisation to purchase issued by MACROVISION CORPORATION.

VP531D

NTSC/PAL DIGITAL VIDEO ENCODER

The VP531 converts digital Y, Cr, Cb, data into analog NTSC/PAL composite video and S-video signals The outputs are capable of driving doubly terminated 75 ohm loads with standard video levels.

The device accepts data inputs complying with CCIR Recommendation 601 and 656. The data is time multiplexed on an 8 bit bus at 27MHz and is formatted as Cb, Y, Cr, Y (i.e. 4:2:2). The video blanking and sync information from REC 656 is included in the data stream when the VP531 is working in slave mode.

The output pixel rate is 27MHz and the input pixel rate is half this frequency, i.e. 13.5MHz.

All necessary synchronisation signals are generated internally when the device is operating in master mode. Digital horizontal and vertical sync outputs are available for use by the host system.

The rise and fall times of sync, burst envelope and video blanking are internally controlled to be within composite video specifications.

Two 9 bit digital to analog converters (DACs) are used to convert the digital luminance and chrominance data into analog signals. An inverted composite video signal is generated by summing the complementary current outputs of each DAC. An internally generated reference voltage provides the biasing for the DACs.

FEATURES

- Converts Y, Cr, Cb data to analog composite video and S-video
- Supports CCIR recommendations 601 and 656
- All digital video encoding
- Selectable master/slave mode for sync signals
- Switchable chrominance bandwidth
- Switchable pedestal with gain compensation
- SMPTE 170M NTSC or CCIR 624 PAL compatible outputs
- GENLOCK mode
- I²C bus serial microprocessor interface
- 64 PQFP package
- Supports Macrovision anti-taping format Rev. 6.1

APPLICATIONS

- Digital Cable TV
- Digital Satellite TV
- Multi-media
- Video games
- Karaoke
- Digital VCRs

ORDERING INFORMATION

VP531D/CG/GP1R

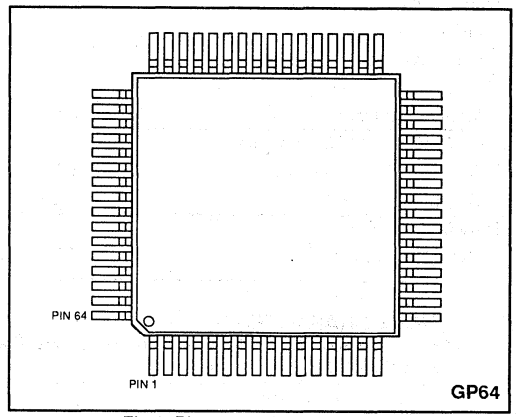


Fig.1 Pin connections (top view)

PIN	FUNCTION	PIN	FUNCTION
1	VDD	33	VDD
2	GND	34	$\overline{\text{RESET}}$
3	D0 (VS O/P)	35	REFSQ
4	D1 (HS O/P)	36	GND
5	D2 (FC0 O/P)	37	VDD
6	D3 (FC1 O/P)	38	GND
7	D4 (FC2 O/P)	39	PD7
8	D5	40	PD6
9	D6 (SCSYNC I/P)	41	PD5
10	D7 (PALID I/P)	42	PD4
11	GND	43	PD3
12	VDD	44	PD2
13	GND	45	PD1
14	GND	46	PD0
15	PXCK	47	GND
16	VDD	48	VDD
17	CLAMP	49	AGND
18	COMPSYNC	50	VREF
19	GND	51	DACGAIN
20	VDD	52	LUMACOMP
21	TDO	53	AVDD
22	TDI	54	LUMAOUT
23	TMS	55	AGND
24	TCK	56	$\overline{\text{COMPOUT}}$
25	GND	57	AGND
26	SA1	58	CHROMAOUT
27	SA2	59	AVDD
28	SCL	60	CHROMACOMP
29	VDD	61	N/C
30	SDA	62	AVDD
31	GND	63	AVDD
32	VDD	64	N/C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC CHARACTERISTICS

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Units
Digital Inputs TTL compatible (except SDA, SCL)						
Input high voltage		VIN	2.0			V
Input low voltage		VIL			0.8	V
Digital Inputs SDA, SCL						
Input high voltage		VIH	0.7 VDD			V
Input low voltage		VIL			0.3 VDD	V
Input high current	VIN = VDD	IIH			10	µA
Input low current	VIN = VSS	IIL			-10	µA
Digital Outputs CMOS compatible						
Output high voltage	IOH = -1mA	VOH	3.7			V
Output low voltage	IOL = +4mA	VOL			0.4	V
Digital Output SDA						
Output low voltage	IOL = +6mA	VOL			0.6	V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC CHARACTERISTICS DACs

Parameter	Symbol	Min.	Typ.	Max.	Units
Accuracy (each DAC)					
Integral linearity error	INL			±1.5	LSB
Diffential linearity error	DNL			±1	LSB
DAC matching error				±5	% grey
Monotonicity			guaranteed		
LSB size			66.83		µA
Internal reference voltage	V_{REF}	0.95	1.00	1.05	V
Internal reference voltage output impedance	Z_R		27k		Ω
Reference Current (V_{REF}/R_{REF}) R_{REF} = 730Ω	I_{REF}		1.3699		mA
DAC Gain Factor (V_{OUT} = K_{DAC} x I_{REF} x R_L). V_{OUT} = DAC code 511	K_{DAC}		24.93		
Peak Glitch Energy (see fig.3)			80		pV-s
CVBS (see note), Y and C - NTSC (pedestal enabled)					
Maximum output, relative to sync bottom			33.75		mA
White level relative to black level			17.64		mA
Black level relative to blank level			1.40		mA
Blank level relative to sync level			7.62		mA
Colour burst peak - peak			7.62		mA
DC offset (bottom of sync)			0.40		mA
CVBS, Y and C - PAL					
Maximum output			34.15		mA
White level relative to black level			18.71		mA
Black level relative to sync level			8.02		mA
Colour burst peak - peak			8.02		mA
DC offset (bottom of sync)			0.00		mA

Note: For the inverted CVBS output subtract the above currents from the maximum output (DAC code 511 = 34.12mA).
All figures are for: R_{REF} = 730Ω, R_L = 37.5Ω. When the device is set up in NTSC mode there is a +0.25% error in the PAL levels.
If R_L = 75Ω then R_{REF} = 1460Ω

ABSOLUTE MAXIMUM RATINGS

Supply voltage	VDD, AVDD	-0·3 to 7·0V
Voltage on any non power pin		-0·3 to VDD+0·3V
Ambient operating temperature		0 to 70°C
Storage temperature		-55°C to 150°C

Note: Stresses exceeding these listed under Absolute Maximum Ratings may induce failure. Exposure to Absolute Maximum Ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply voltage	VDD, AVDD	4.75	5.00	5.25	V
Power supply current (including analog outputs)	IDD		150		mA
Input clock frequency	PXCK	-50ppm	27.00	+50ppm	MHz
SCL clock frequency	fscl			500	kHz
Analog video output load			37.5		Ω
DAC gain resistor			730		Ω
Ambient operating temperature		0		70	°C

VIDEO CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units
Luminance bandwidth			5.5		MHz
Chrominance bandwidth (Extended B/w mode)			1.3		MHz
Chrominance bandwidth (Reduced B/w mode)			650		kHz
Burst frequency (NTSC)			3.57954545		MHz
Burst frequency (PAL-B, D,G, H, I)			4.43361875		MHz
Burst frequency (PAL-M)			3.57561149		MHz
Burst frequency (PAL-N Argentina)			3.58205625		MHz
Burst cycles (NTSC and PAL-M, N)			9		Fsc cycles
Burst cycles (NTSC and PAL-B, D, G, H,I)			10		Fsc cycles
Burst envelope rise / fall time (NTSC and PAL-M, N)			300		ns
Burst envelope rise / fall time (NTSC and PAL-B, D, G, H,I)			300		ns
Analog video sync rise / fall time (NTSC and PAL-M, N)			145		ns
Analog video blank rise / fall time (NTSC and PAL-B, D, G, H,I)			245		ns
Differential gain			1.5		% pk-pk
Differential phase			1		% pk-pk
Signal to noise ratio (unmodulated ramp)				-61	dB
Chroma AM signal to noise ratio (100% red field)				-56	dB
Chroma PM signal to noise ratio (100% red field)				-58	dB
Hue accuracy				2.5	%
Colour saturation accuracy				2.5	%
Residual sub carrier			-60		dB
Luminance / chrominance delay			10		ns

ESD COMPLIANCE

Pins	Test	Test Levels	Notes
All pins	Human body model	2kV on 100pF through 1k5Ω	Meets Mil-Std-883 Class 2
All pins	Machine model	200V on 200pF through 0Ω & 500nH	

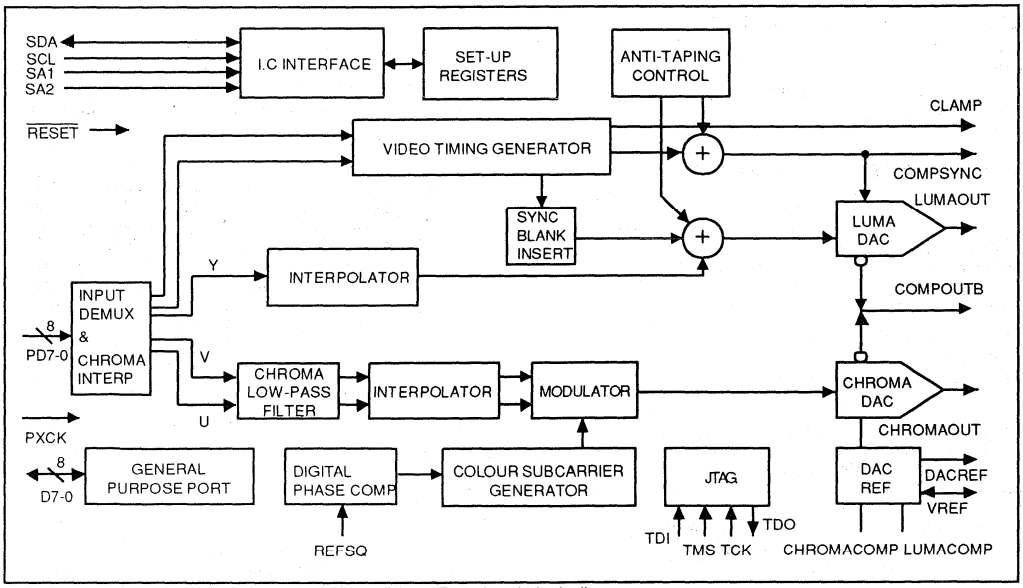


Fig.2 Functional block diagram

PIN DESCRIPTIONS

Pin Name	Pin No.	Description
PD0-7	39 - 46	8 Bit Pixel Data inputs clocked by PXCK. PD0 is the least significant bit, corresponding to Pin 46. These pins are internally pulled low.
D0-7	3 - 10	8 Bit General Purpose Port input/output. D0 is the least significant bit, corresponding to Pin 3. These pins are internally pulled low.
PXCK	15	27MHz Pixel Clock input. The VP531 internally divides PXCK by two to provide the pixel clock.
CLAMP	17	The CLAMP output signal is synchronised to COMPSYNC output and indicates the position of the BURST pulse, (lines 10-263 and 273-525 for NTSC and PAL-M; lines 6-310 and 319-623 for PAL-B,D, G,I,N(Argentina)).
COMPSYNC	18	Composite sync pulse output. This is an active low output signal.
TDO	21	JTAG Data scan output port.
TDI	22	JTAG Data scan input port.
TMS	23	JTAG Scan select input.
TCK	24	JTAG Scan clock input.
SA1	26	Slave address select.
SA2	27	Slave address select.
SCL	28	Standard I²C bus serial clock input.
SDA	30	Standard I²C bus serial data input/output.
$\overline{\text{RESET}}$	34	Master reset. This is an asynchronous active low input signal and must be asserted for a minimum of 200ns in order to reset the VP531.
REFSQ	35	Reference square wave input used only during Genlock mode.
VREF	50	Voltage reference output. This output is nominally 1·0V and should be decoupled with a 100nF capacitor to GND.
DAC GAIN	51	DAC full sacle current control. A resistor connected between this pin and GND sets the magnitude of the video output current. An internal loop amplifier control a reference current flowing through this resistor so that the voltage across it is equal to the Vref voltage.
LUMACOMP	52	Luma DAC compensation. A 100nF ceramic capacitor must be connected between pin 52 and pin 53.
LUMAOUT	54	True luminance, true chrominance and inverted composite video signal outputs. These are high impedance current source outputs. A DC path to GND must exist from each of these pins
COMPOUT	56	
CHROMAOUT	58	
CHROMA-COMP	60	Chroma DAC compensation. A 100nF ceramic capacitor must be connected between pin 60 and pin 59.
NOT USED	61, 64	
VDD	1, 12, 16, 20, 29, 32, 33, 37, 48	Positive supply input. All VDD pins must be connected.
AVDD	53, 59 62, 63	Analog positive supply input. All AVDD pins must be connected.
GND	2, 11, 13, 14, 19, 25, 31, 36, 38, 47	Negative supply input. All GND pins must be connected.
AGND	49, 55, 57	Negative supply input. All AGND pins must be connected.

REGISTERS MAP

See Register Details for further explanations.

ADDRESS hex	REGISTER NAME	7	6	5	4	3	2	1	0	R/W	DEFAULT hex
	BAR	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	W	
00	PART ID2	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	R	13
01	PART ID1	ID0F	ID0E	ID0D	ID0C	ID0B	ID0A	ID09	ID08	R	66
02	PART ID0	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00	R	57
03	REV ID	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	R	04
04	GCR	-	-	YCDELAY	RAMPEN	-	-	VFS1	VFS0	R/W	00
05	VOCR	-	CLAMPDIS	CHRBW	SYNCDIS	BURDIS	LUMDIS	CHRDIS	PEDEN	R/W	00
06	HANC	-	-	DFI2	DFI1	DFI0	Reserved	Reserved	ACTREN	*	00
07	ANCID	AN7	AN6	AN5	AN4	AN3	AN2	AN1	PARITY	R/W	00
08	SC_ADJ	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	R/W	97
09	FREQ2	FR17	FR16	FR15	FR14	FR13	FR12	FR11	FR10	R/W	87
0A	FREQ1	FR0F	FR0E	FR0D	FR0C	FR0B	FR0A	FR09	FR08	R/W	C1
0B	FREQ0	FR07	FR06	FR05	FR04	FR03	FR02	FR01	FR00	R/W	F1
0C	SCHPHM	-	-	-	-	-	-	-	SCH8	R/W	00
0D	SCHPHL	SCH7	SCH6	SCH5	SCH4	SCH3	SCH2	SCH1	SCH0	R/W	00
0E to 1F	Reserved										
20	GPPCTL	CTL7	CTL6	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	W	FF
21	GPPRD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	R	-
22	GPPWR	WR7	WR6	WR5	WR4	WR3	WR2	WR1	WR0	W	00
23 to EF	Not used										
F0	Reserved									R/W	00
F1	Reserved									R/W	00
F2	Reserved									R/W	00
F3	Reserved									R/W	00
F4	Reserved									R/W	00
F8	HSOFFL	HSOFF7	HSOFF6	HSOFF5	HSOFF4	HSOFF3	HSOFF2	HSOFF1	HS0FF0	R/W	7E
F9	HSOFFM	-	-	-	-	-	-	HSOFF9	HSOFF8	R/W	00
FD	GPSDAC	-	-	LUMADIS	CHRMDIS		LUMCHKI	CHRCKHI	CMPCKHI	R/W	38
FE	GPSTST	PROGRESS	BISTO	DIGSH	TSTBLEV	STSYNCLO	-	CTRLC_1	CTRLC_0	R/W	00
FF	GPSCTL	FSC4SEL	GENDITH	GENLKEN	NOLOCK	PALIDEN	TSURST	CHRMCLIP	TRSEL	R/W	00

Table.1 Register map

NOTE * For register HANC, bits 3, 4 and 5 are read only. Bits 1 and 2 are reserved. N/A = not applicable.

Standard	Lines/ field	Field freq. HZ	Number of pixels/line at 27MHz	Horizontal freq. kHz. f_H	Subcarrier freq. kHz. f_{SC}	f_{SC}/f_H	SC_ADJ register hex	FREQ2-0 registers hex
NTSC (default)	525	59.94	1716	15.734266	3.57954545	(455/2)	xx	87 C1 F1
PAL-B, D, G, H, I	625	50	1728	15.625000	4.43361875	(1135/4+1/625)	9C	A8 26 2B
PAL-M	525	59.94	1716	15.734266	3.57561189	(909/4)	xx	87 9B C0
PAL-N (Argentina)	625	50	1728	15.625000	3.58205625	(917/4+1/625)	57	87 DA 51

Table.2 Line, field and subcarrier standards and register settings

xx = don't care.

The calculation of the FREQ register value is according to the following formula:-

$$FREQ = (2^{26} \times f_{SC}/f_H) / (\text{number of pixels/line}) \quad \text{hex}$$

Both NTSC and PAL-M values are rounded UP from the decimal number. PAL-B, D, G, H, I and N (Argentina) are rounded DOWN. The SC_ADJ value is derived from the adjustment needed to be added after 8 fields to ensure accuracy of the Subcarrier frequency. Note the SC_ADJ value of 9C required for PAL-B, D, G, H, I, is different to the default state of the register.

REGISTER DETAILS

BAR — **Base register**
RA7-0 — Register address.

PART ID 2-0 — **Part number**
ID17-00 — Chip part identification (ID) number.

REV ID — **Revision number**
REV7-0 — Chip revision ID number.

GCR — **Global Control**
YCDELAY — Luma to Chroma delay.
High = 37ns luma delay, this may be used to compensate for group delay in external filters.
Low = normal operation (default).

RAMPEN — Modulated ramp enable.
High = ramp output for differential phase and gain measurements. A 27MHz clock must be applied to PXCK pin.
Low = normal operation (default).

VFS1-0 — Video format select

VFS1	VFS0	
0	0	NTSC (default)
0	1	PAL-B,D,G,H,I,N(Argentina)
1	0	PAL-M
1	1	Reserved

VOCR — **Video Output Control**
CLAMPDIS — High = Clamp signal disable
Low = normal operation with clamp signal enabled (default).

CHRBW — Chroma bandwidth select.
High = ±1·3MHz.
Low = ±650kHz (default)

SYNCDIS — High = Sync disable (in composite video signal). COMPSYNC is not affected.
Low = normal operation with sync enabled (default).

BURDIS — High = Chroma burst disable.
Low = normal operation, with burst enabled (default).

LUMDIS — High = Luma input disable - force black level with synchronisation pulses maintained.
Low = normal operation, with Luma input enabled (default).

CHRDIS — High = Chroma input disable - force monochrome.
Low = normal operation, with Chroma input enabled (default).

PEDEN — High = Pedestal (set-up) enable a 7·5 IRE pedestal on lines 23-262 and 286-525. Valid for NTSC/PAL-M only

HANC — **Horizontal Ancillary Data Control**
DFI2-0(read only) — Digital Field Identification, 000=Field1
ANCTREN — Ancillary timing reference enable. When High use FIELD COUNT from ancillary data stream. When low, data is ignored.

ANCID — **Ancillary data ID**
AN7-1 — Ancillary data ID
AN0 — Parity bit (odd)
Only ancillary data in REC 656 data stream with the same ID as this byte will be decoded by the VP531 to produce H and V synchronisation and FIELD COUNT.

SC_ADJ — **Sub Carrier Adjust**
SC7-0 — Sub carrier frequency seed value, see table 2.

FREQ2-0 — **Sub carrier frequency**
FR17-00 — 24 bit Sub carrier frequency programmed via I²C bus, see table 2. FREQ2 is the most significant byte (MSB).

SCHPHM-L — **Sub carrier phase offset**
SCH9-0 — 9 bit Sub carrier phase relative to the 50% point of the leading edge of the horizontal part of composite sync. SCHPHM bit 0 is the MSB. The nominal value is zero. This register is used to compensate for delays external to the VP531.

GPPCTL — **General purpose port control**
CTL7-0 — Each bit controls port direction
Low = output High = input

GPPRD — **General purpose port read data**
RD7-0 — I²C bus read from general purpose port (only INPUTS defined in GPPCTL)

GPPWR — **General purpose port write data**
WR7-0 — I²C bus write to general purpose port (only OUTPUTS defined in GPPCTL)

HSOFFM-L — **HS offset**
HSOFF9-0 — This is a 10 bit number which allows the user to offset the start of digital data input with reference to the pulse HS.

GPSDAC — **DAC test register**
LUMADIS — 1 = Normal operation
0 = Luma DAC input set zero

CHRMDIS — 1 = Normal operation
0 = Chroma DAC input set zero

LUMCKHI — 1 = Luma DAC clock input set to '1'

CHRCKHI — 0 = Normal operation
1 = Chroma DAC clock input set to '1'

GPSCTL **GPS Control**

FSC4SEL — When high, REFSQ = 4xFSC and GPP bit D6 is forced to become an input for a SCSYNC signal (high = reset), which provides a synchronous phase reset for FSC divider. Low = normal operation with REFSQ = 1xFSC. (default).

GENDITH — 1 = Gen lock dither added.

GENLKEN — High = enable Genlock to REFSQ signal input.
Low = internal subcarrier generation (default).

NOLOCK — Genlock status bit (read only)
Low = Genlocked.
High = cannot lock to REFSQ. This bit is cleared by reading and set again if lock cannot be attained.

PALIDEN — High = enable external PAL ID phase control and GPP bit D7 is forced to become an input for PAL ID switch signal, (GPP bit D7 - Low = +135°, High = -135°).
Low = normal operation, internal PAL ID phase switch is used (default).

TSURST — High = chip soft reset. Registers are NOT reset to default values.
Low = normal operation (default).

CHRMCLIP — High = enable clipping of chroma data when luma goes below black level and is clipped.
Low = no chroma clipping (default).

TRSEL — High = master mode, GPP bits D0 - 4 are forced to become a video timing port with VS, HS and FIELD outputs.
Low = slave mode, timing from REC656.

I²C BUS CONTROL INTERFACE

I²C bus address

A6	A5	A4	A3	A2	A1	A0	R/ $\overline{W}$
0	0	0	1	1	SA2	SA1	X

The serial microprocessor interface is via the bi-directional port consisting of a data (SDA) and a clock (SCL) line. It is compatible to the Philips I²C bus standard (Jan. 1992 publication number 9398 393 40011). The interface is a slave transmitter - receiver with a sub-address capability. All communication is controlled by the microprocessor. The SCL line is input only. The most significant bit (MSB) is sent first. Data must be stable during SCL high periods.

A bus free state is indicated by both SDA and SCL lines being high. START of transmission is indicated by SDA being pulled low while SCL is high. The end of transmission, referred to as a STOP, is indicated by SDA going from low to high while SCL is high. The STOP state can be omitted if a repeated START is sent after the acknowledge bit. The reading device acknowledges each byte by pulling the SDA line low on the ninth clock pulse, after which the SDA line is released to allow the transmitting device access to the bus.

The device address can be partially programmed by the setting of the pins SA1 and SA2. This allows the device to respond to one of four addresses, providing for system flexibility. The I²C bus address is seven bits long with the last bit indicating read / $\overline{\text{write}}$ for subsequent bytes.

The first data byte sent after the device address, is the sub-address - BAR (base address register). The next byte will be written to the register addressed by BAR and subsequent bytes to the succeeding registers. The BAR maintains its data after a STOP signal.

NTSC/PAL Video Standards

Both NTSC (4-field, 525 lines) and PAL (8-field, 625 lines) video standards are supported by the VP531. All raster synchronisation, colour sub-carrier and burst characteristics are adapted to the standard selected. The VP531 generates outputs which follow the requirements of SMPTE 170M and CCIR 624 for PAL signals.

The device supports the following:
NTSC,
PAL B, D, G, H, I, N (Argentina) and M.

Video Timing - Slave sync mode

The VP531 has an internal timing generator which produces video timing signals appropriate to the mode of operation. In the default (power up) slave mode, all timing signals are derived from the input clock, PXCK, which must be derived from a crystal controlled oscillator. Input pixel data is latched on the rising edge of the PXCK clock.

The video timing generator produces the internal blanking and burst gate pulses, together with the composite sync output signal, using timing data (TRS codes) from the Ancillary data stream in the REC656 input signal, (when TRSEL (bit 0 of GPSCTL register) is set low).

Video Timing - Master sync mode

When TRSEL (bit 0 of GPSCTL register) is set high, the VP531 operates in a MASTER sync mode, all REC656 timing reference codes are ignored and GPP bits D0 - 4 become a video timing port with VS, HS and FIELD outputs. The PXCK signal is, however, still used to generate all internal clocks. When TRSEL is set high, the direction setting of bits 4 - 0 of the GPPCTL register is ignored.

VS is the start of the field sync datum in the middle of the equalisation pulses. HS is the line sync which is used by the preceding MPEG2 decoder to define when to output digital video data to the VP531. The position of the falling edge of HS relative to the first data Cb0, can be programmed in HSOFFM-L registers, see table. 4.

Video Blanking

The VP531 automatically performs standard composite video blanking. Lines 1-9, 264-272 inclusive, as well as the last half of line 263 are blanked in NTSC mode. In PAL mode, lines 1-5, 311-318, 624-625 inclusive, as well as the last half of line 623 are blanked.

The V bit within REC656 defines the video blanking when TRSEL (bit 0 of GPSCTL register) is set low. When in MASTER mode with TRSEL set high the video encoder is still enabled. Therefore if these lines are required to be blank they must have no video signal input.

Interpolator

The luminance and chrominance data are separately passed through interpolating filters to produce output sampling rates double that of the incoming pixel rate. This reduces the sinx/x distortion that is inherent in the digital to analog converters and also simplifies the analog reconstruction filter requirements.

Digital to Analog Converters

The VP531 contains two 9 bit digital to analog converters which produce the analog video signals. The DACs use a current steering architecture in which bit currents are routed to one of two outputs; thus the DAC has true and complementary outputs. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed. An on-chip voltage reference of 1.0V (typ.) provides the necessary biasing. if required this can be overridden by an external reference.

The full-scale output currents of the DACs is set by external resistors between the DACGAIN and VSS pins. An on-chip loop amplifier stabilises the full-scale output current against temperature and power supply variations.

By summing the complementary luma and chroma DAC current outputs an inverted composite output is generated. Note that this signal has a DC offset and therefore usally needs to be capacitively coupled. The analog outputs of the VP531 are capable of directly driving doubly terminated 75Ω co-axial cable. If it is required only to drive a single 75Ω load then DACGAIN resistor is simply doubled.

Luminance, Chrominance and Composite Video Outputs

The Luminance video output (LUMAOUT pin 54) drives a 37.5Ω load at 1.0V, sync tip to peak white. It contains only the luminance content of the image plus the composite sync pulses. In the NTSC mode, a set-up level (pedestal) offset can be added during the active video portion of the raster. The pedestal is programmed by PEDEN bit in VOCR register.

The Chrominance video output (CHROMAOUT pin 58) drives a 37.5Ω load at levels proportional in amplitude to the luma output (40 IRE pk-pk burst). This output has a fixed offset current which will produce approximately a 0.5V DC bias across the 37.5Ω load. Burst is injected with the appropriate timing relative to the luma signal.

The inverted composite video output (COMPOUTB pin 56) will also drive a 37.5Ω loas at 1.0V, sync tip to peak white. It contains both the luminance and chrominance content of the signal plus the composite sync pulses.

Output sinx/x compensation filters are required on all video output, as shown in the typical application diagram, see figs. 6 & 7.

HS offset

The position of the falling edge of HS relative to the first data Cb0, can be programmed in HSOFFM-L registers, see figure 4, this is called the pipeline delay and may need adjusting for a particular application. This is done by programming a 10 bit number called HSOFF into the HSOFFM and HSOFFL registers, HSOFFM being the most significant two bits and HSOFFL the least significant eight bits. A default value of 07EH is held in the registers.

The value to program into HSOFF can be looked up in tables 3 &4:

Nck	HSOFF	Comment
0 to 120	126 to 6	HS normal (64 cks)
121 to 138	863 to 801	HS pulse shortened*
184 to 857	800 to 127	HS normal (64 cks)

Table.3 for NTSC and PAL-M

Nck	HSOFF	Comment
0 to 131	137 to 6	HS normal (64 cks)
132 to 194	869 to 807	HS pulse shortened*
195 to 863	806 to 138	HS normal (64 cks)

Table.4 for NTSC and PAL-B, D, G, H, I, N

**HS pulse shortened means that the width of the pulse will be less than the normal 64 13.5MHz clock cycles.*

where Nck = number of 13.5MHz clock cycles between the falling edge of HS and Cb0 (first data I/P on PD7-0) see fig. 4. Decreasing HSOFF advances the HS pulse (numbers are in decimal).

The interruption in the sequence of values is because the HS signal is jumping across a line boundary to the previous line as the offset is increased. The register default value is 7EH and this sets Nck to 0, ie. the HS negative edge and Cb0 are co-incident in NTSC mode.

Genlock using REFSQ input

The VP531 can be Genlocked to another video source by setting GENLKEN high (in GPSCTL register) and feeding a phase coherent sub carrier frequency signal into REFSQ. Under normal circumstances, REFSQ will be the same frequency as the sub carrier. But by setting FSC4SEL high (in GPSCTL register), a 4 x sub carrier frequency signal may be input to REFSQ. In this case, the Genlock circuit can be reset to the required phase of REFSQ, by supplying a pulse to SCSYNC (pin 9). The frequency of SCSYNC can be at sub carrier frequency, but once per line, or once per field could be adequate, depending on the application. When GENLKEN is SET high, the direction setting of bit 6 of the GPPCTL register is ignored.

PALID Input

When in Genlock mode with GENLKEN set high (in GPSCTL register), the VP531 requires a PAL phase identification signal, to define the correct phase on every line. This is supplied to PALID input (pin 10), High = -135° and low = +135°. The signal is asynchronous and should be changed before the sub carrier burst signal. PALID input is enabled by setting PALIDEN high (in GPSCTL register). When GENLKEN is high, the direction setting of bit 7 of the GPPCTL register is ignored

Master Reset

The VP531 must be initialised with the $\overline{\text{RESET}}$ pin 34. This is an asynchronous active low signal and must be active for a minimum of 200ns in order for the VP531 to be reset. The device resets to line 64, start of horizontal sync (i.e. line blanking active). There is no on-chip power on reset circuitry.

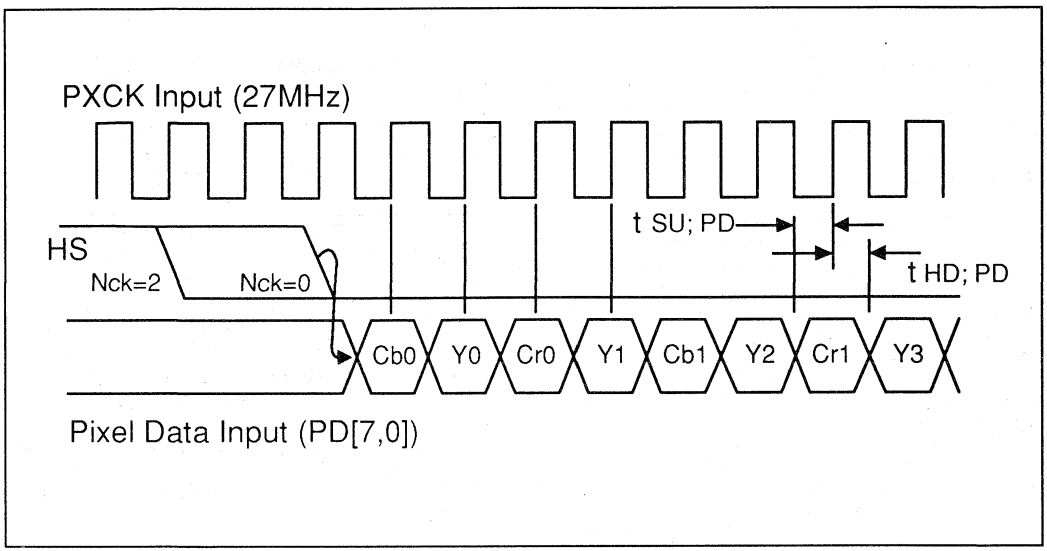


Fig.3 REC 656 interface with HS output timing

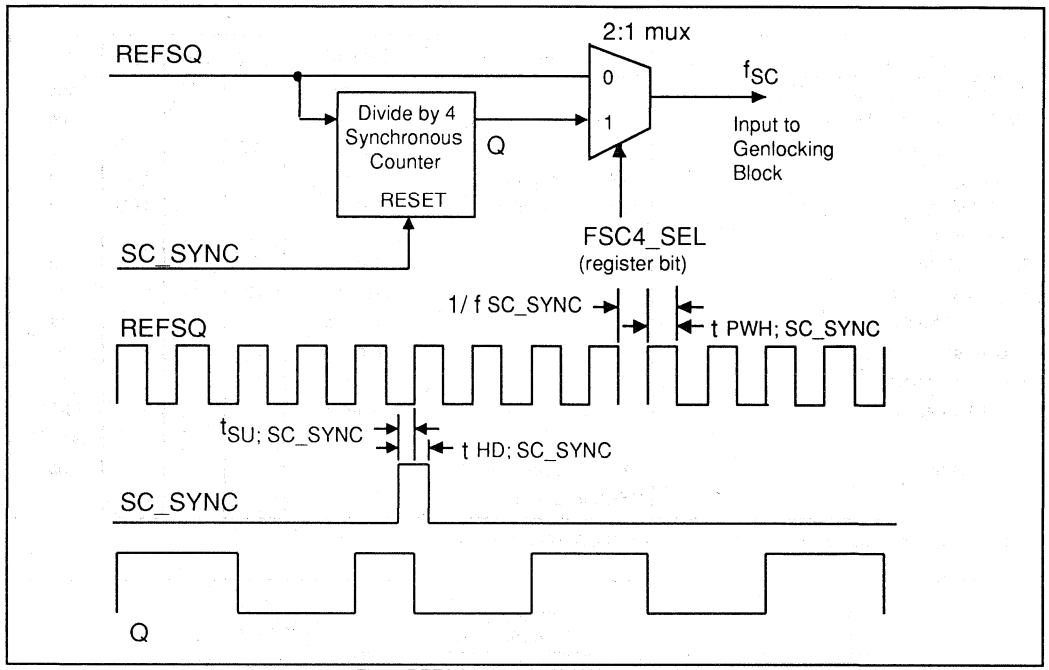


Fig.4 REFSQ and SC_SYNC input timing

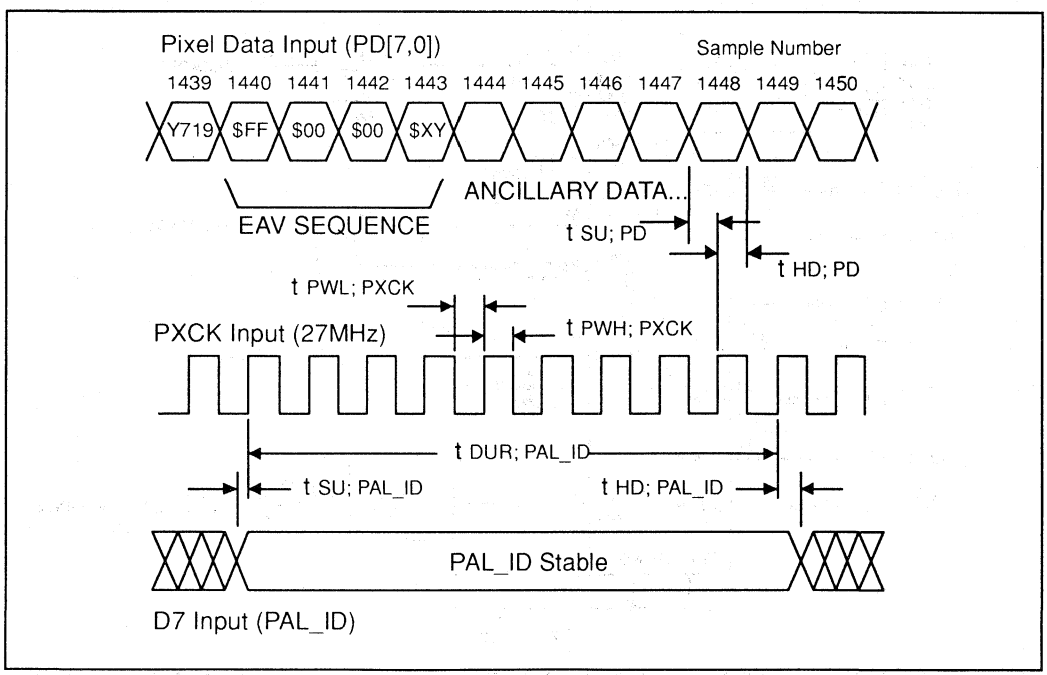


Fig.5 PAL_ID input timing

TIMING INFORMATION

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Units
Master clock frequency (PXCK input)		f_{PXCK}		27.0		MHz
PXCK pulse width, HIGH		$t_{PWH;\ PXCK}$	10			ns
PXCK pulse width, LOW		$t_{PWL;\ PXCK}$	14.5			ns
PXCK rise time	10% to 90% points	t_{RP}			TBD	ns
PXCK fall time	90% to 10% points	t_{FP}			TBD	ns
PD7-0 set up time		$t_{SU;PD}$	10			ns
PD7-0 hold time		$t_{HD;PD}$	5			ns
SC_SYNC set up time		$t_{SU;SC\_SYNC}$	10			ns
SC_SYNC hold time		$t_{HD;SC\_SYNC}$	0			ns
PAL_ID set up time		$t_{SU;PAL\_ID}$	10			ns
PAL_ID hold time		$t_{HD;PAL\_ID}$	0			ns
PAL_ID duration		$t_{DUR;PAL\_ID}$	9			PXCK periods
Output delay	PXCK to COMPSYNC PXCK to CLAMP	t_{DOS}			25	ns

Note: Timing reference points are at the 50% level. Digital C_{LOAD} <40pF.

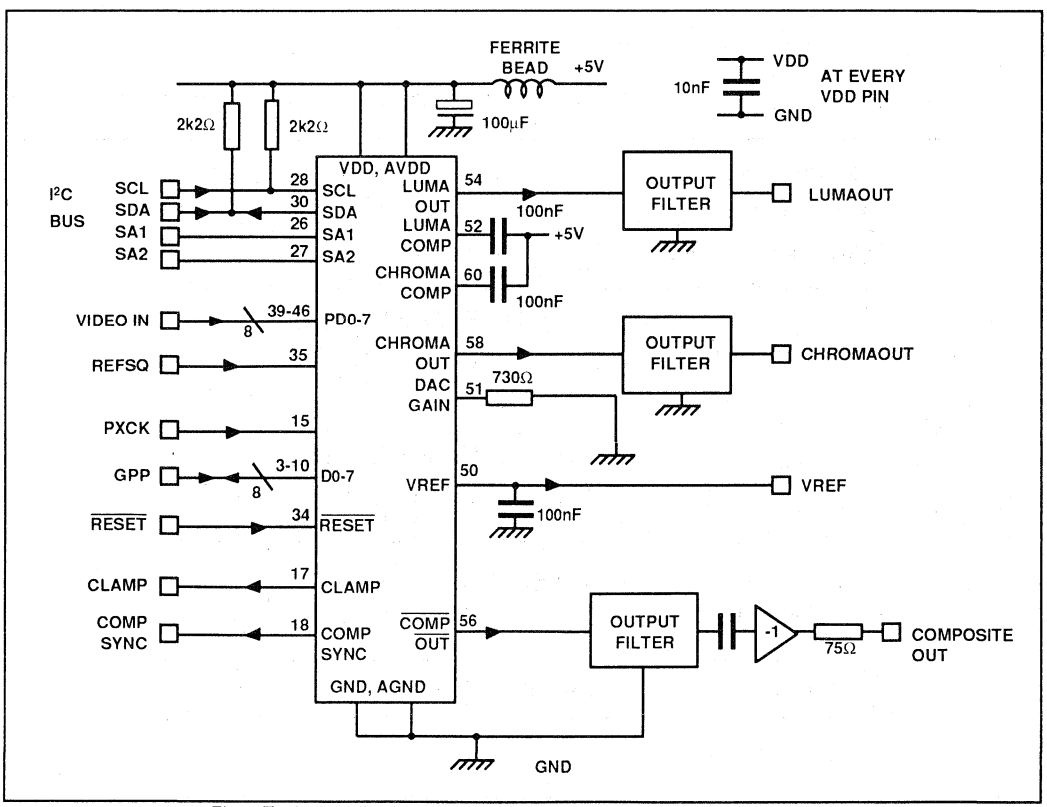


Fig.6 Typical application diagram, SLAVE mode. (Output filter - see Fig.8)

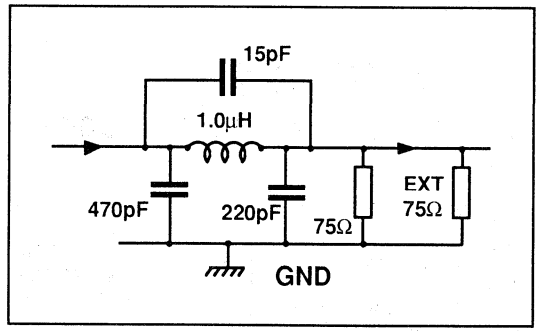


Fig.7 Output reconstruction filter

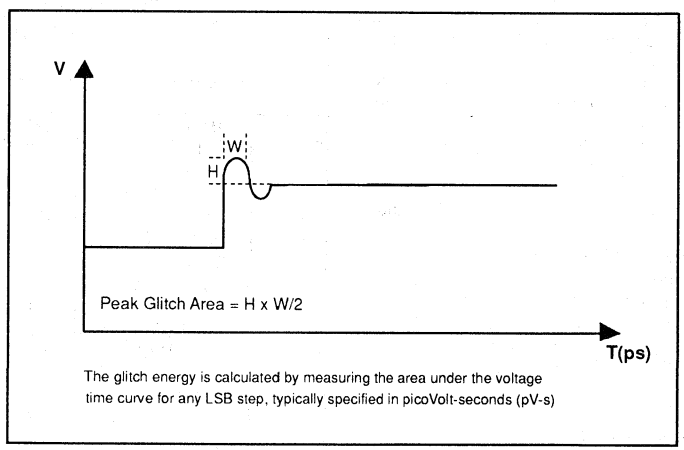


Fig.8 Glitch Energy

VP5511A

NTSC/PAL DIGITAL VIDEO ENCODER

The VP5511A converts digital Y, Cr, Cb, data into analog NTSC/PAL composite video and S-video signals. The outputs are capable of driving doubly terminated 75 ohm loads with standard video levels.

The device accepts data inputs complying with CCIR Recommendation 601 and 656. The data is time multiplexed on an 8 bit bus at 27MHz and is formatted as Y, Cr, Y, Cb (i.e. 4:2:2). The video blanking and sync information from REC 656 is included in the data stream when the VP5511A is working in slave mode.

The output pixel rate is 27MHz and the input pixel rate is half this frequency, i.e. 13.5MHz.

All necessary synchronisation signals are generated internally when the device is operating in master mode. Digital horizontal and vertical sync outputs are available for use by the host system.

The rise and fall times of sync, burst envelope and video blanking are internally controlled to be within composite video specifications.

Three digital to analog converters (DACs) are used to convert the digital luminance, chrominance and composite data into true analog signals. An internally generated reference voltage provides the biasing for the DACs.

FEATURES

- Converts Y, Cr, Cb data to analog composite video and S-video
- Supports CCIR recommendations 601 and 656
- All digital video encoding
- Selectable master/slave mode for sync signals
- Switchable chrominance bandwidth
- Switchable pedestal with gain compensation
- SMPTE 170M NTSC or CCIR 624 PAL compatible outputs
- GENLOCK mode
- Line 21 Closed Caption encoding
- I²C bus serial microprocessor interface

APPLICATIONS

- Digital Cable TV
- Digital Satellite TV
- Multi-media
- Video games
- Karaoke
- Digital VCRs

ORDERING INFORMATION

VP5511A/CG/GP1R

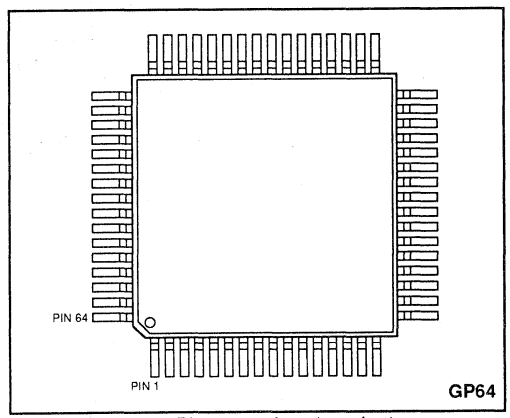


Fig.1 Pin connections (top view)

PIN	FUNCTION	PIN	FUNCTION
1	VDD	33	VDD
2	GND	34	$\overline{\text{RESET}}$
3	D0 (VS O/P)	35	REFSQ
4	D1 (HS O/P)	36	GND
5	D2 (FC0 O/P)	37	VDD
6	D3 (FC1 O/P)	38	GND
7	D4 (FC2 O/P)	39	PD7
8	D5	40	PD6
9	D6 (SCSYNC I/P)	41	PD5
10	D7 (PALID I/P)	42	PD4
11	GND	43	PD3
12	VDD	44	PD2
13	GND	45	PD1
14	GND	46	PD0
15	PXCK	47	GND
16	VDD	48	VDD
17	CLAMP	49	AGND
18	COMPSYNC	50	VREF
19	GND	51	DACGAIN
20	VDD	52	LUMACOMP
21	TDO	53	AVDD
22	TDI	54	LUMAOUT
23	TMS	55	AGND
24	TCK	56	COMPOUT
25	GND	57	AGND
26	SA1	58	CHROMAOUT
27	SA2	59	AVDD
28	SCL	60	COMPCOMP
29	VDD	61	N/C
30	SDA	62	AVDD
31	GND	63	AVDD
32	VDD	64	N/C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC CHARACTERISTICS

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Units
Digital Inputs TTL compatible (except SDA, SCL)						
Input high voltage		VIN	2.0			V
Input low voltage		VIL			0.8	V
Digital Inputs SDA, SCL						
Input high voltage		VIH	0.7 VDD			V
Input low voltage		VIL			0.3 VDD	V
Input high current	VIN = VDD	IIH			10	µA
Input low current	VIN = VSS	IIL			-10	µA
Digital Outputs CMOS compatible						
Output high voltage	IOH = -1mA	VOH	3.7			V
Output low voltage	IOL = +4mA	VOL			0.4	V
Digital Output SDA						
Output low voltage	IOL = +6mA	VOL			0.6	V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC CHARACTERISTICS DACs

Parameter	Symbol	Min.	Typ.	Max.	Units
Accuracy (each DAC)					
Integral linearity error	INL			±1.5	LSB
Diffential linearity error	DNL			±1	LSB
DAC matching error				±5	%
Monotonicity			guaranteed		
LSB size			66.83		µA
Internal reference voltage	V_{REF}	0.95	1.00	1.05	V
Internal reference voltage output impedance	Z_R		27k		Ω
Reference Current (V_{REF}/R_{REF}) R_{REF} = 730Ω	I_{REF}		1.3699		mA
DAC Gain Factor (V_{OUT} = K_{DAC} x IREF x R_L), V_{OUT} = DAC code 511	K_{DAC}		24.93		
Peak Glitch Energy (see fig.3)			50		pV-s
CVBS, Y and C - NTSC (pedestal enabled)					
Maximum output, relative to sync bottom			33.75		mA
White level relative to black level			17.64		mA
Black level relative to blank level			1.40		mA
Blank level relative to sync level			7.62		mA
Colour burst peak - peak			7.62		mA
DC offset (bottom sync)			0.40		mA
CVBS, Y and C - PAL					
Maximum output			34.15		mA
White level relative to black level			18.71		mA
White level relative to sync level			26.73		mA
Black level relative to sync level			8.02		mA
Colour burst peak - peak			8.02		mA
DC offset (bottom sync)			0.00		mA

Note: All figures are for: R_{REF} = 730Ω R_L = 37.5Ω. When the device is set up in NTSC mode there is a +0.25% error in the PAL levels. If R_L = 75Ω then R_{REF} = 1460Ω.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	VDD, AVDD	-0·3 to 7·0V
Voltage on any non power pin		-0·3 to VDD+0·3V
Ambient operating temperature		0 to 70°C
Storage temperature		-55°C to 150°C

Note: Stresses exceeding these listed under Absolute Maximum Ratings may induce failure. Exposure to Absolute Maximum Ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply voltage	VDD, AVDD	4.75	5.00	5.25	V
Power supply current (including analog outputs)	IDD		150		mA
Input clock frequency	PXCK	-50ppm	27.00	+50ppm	MHz
SCL clock frequency	fSCL			500	kHz
Analog video output load			37.5		Ω
DAC gain resistor			730		Ω
Ambient operating temperature		0		70	°C

VIDEO CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units
Luminance bandwidth			5.5		MHz
Chrominance bandwidth (Extended B/w mode)			1.3		MHz
Chrominance bandwidth (Reduced B/w mode)			650		kHz
Burst frequency (NTSC)			3.57954545		MHz
Burst frequency (PAL-B, D,G,H,I)			4.43361875		MHz
Burst frequency (PAL-M)			3.57561189		MHz
Burst frequency (PAL-N Argentina)			3.58205625		MHz
Burst cycles (NTSC and PAL-M,N)			9		Fsc cycles
Burst cycles (NTSC and PAL-B, D, G, H,I)			10		Fsc cycles
Burst envelope rise / fall time (NTSC and PAL-M,N)			300		ns
Burst envelope rise / fall time (NTSC and PAL-B, D, G, H,I)			300		ns
Analog video sync rise / fall time (NTSC and PAL-M,N)			145		ns
Analog video blank rise / fall time (NTSC and PAL-B, D, G, H,I)			245		ns
Differential gain			1.5		% pk-pk
Differential phase			TBD		° pk-pk
Signal to noise ratio (unmodulated ramp)			-61	-61	dB
Chroma AM signal to noise ratio (100% red field)			-56	-56	dB
Chroma PM signal to noise ratio (100% red field)			-58	-58	dB
Hue accuracy				2.5	%
Colour saturation accuracy				2.5	%
Residual sub carrier			-60		dB
Luminance / chrominance delay			10		ns

ESD COMPLIANCE

Pins	Test	Test Levels	Notes
All pins	Human body model	2kV on 100pF through 1k5Ω	Meets Mil-Std-883 Class 2
All pins	Machine model	200V on 200pF through 0Ω & 500nH	

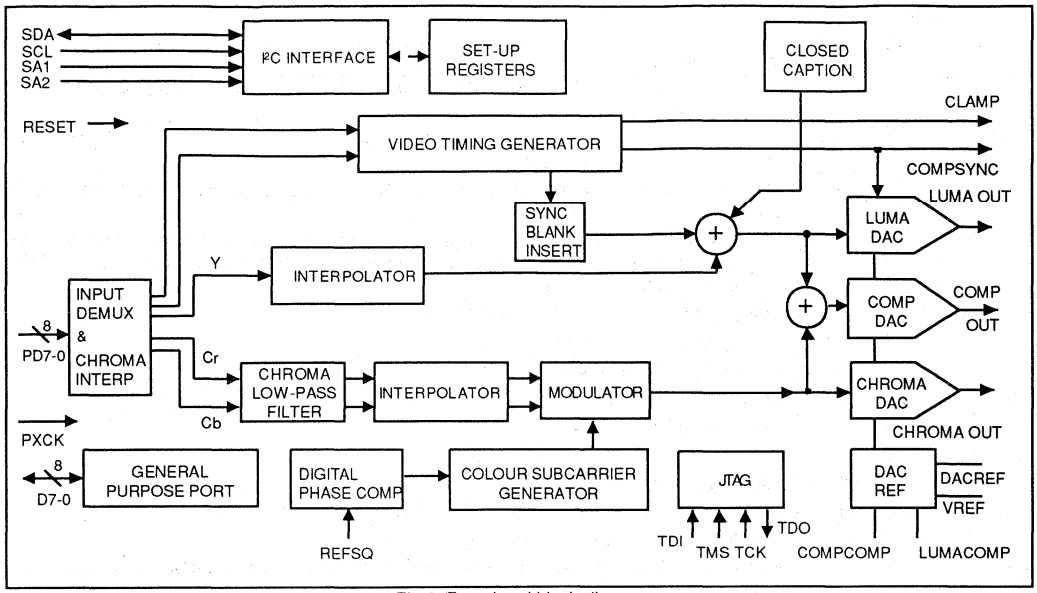


Fig.2 Functional block diagram

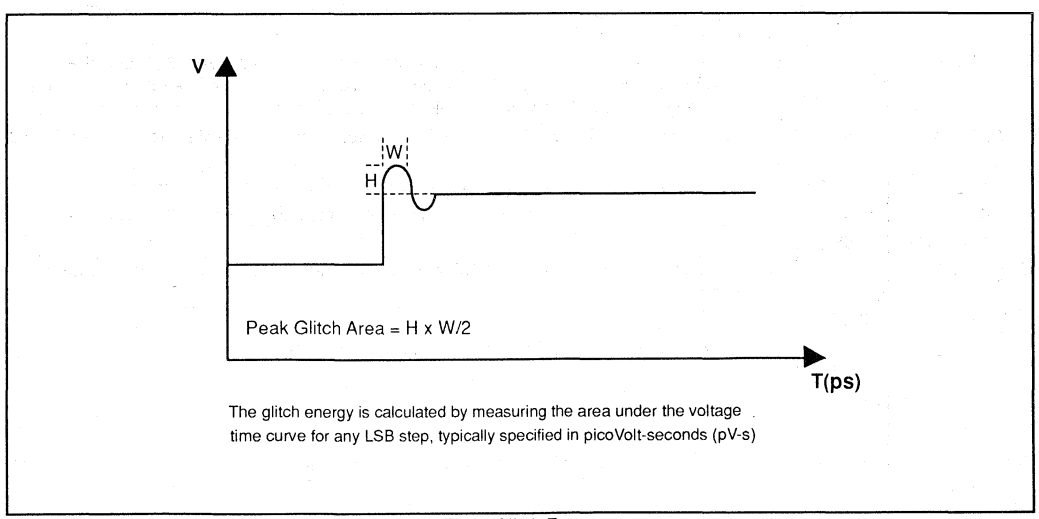


Fig.3 Glitch Energy

PIN DESCRIPTIONS

Pin Name	Pin No.	Description
PD0-7	39 - 46	8 Bit Pixel Data inputs clocked by PXCK. PD0 is the least significant bit, corresponding to Pin 46. These pins are internally pulled low.
D0-7	3 - 10	8 Bit General Purpose Port input/output. D0 is the least significant bit, corresponding to Pin 3. These pins are internally pulled low.
PXCK	15	27MHz Pixel Clock input. The VP5511A internally divides PXCK by two to provide the pixel clock.
CLAMP	17	The CLAMP output signal is synchronised to COMPSYNC output and indicates the position of the BURST pulse, (lines 10-263 and 273-525 for NTSC and PAL-M; lines 6-310 and 319-623 for PAL-B,D, G,I,N(Argentina)).
COMPSYNC	18	Composite sync pulse output. This is an active low output signal.
TDO	21	JTAG Data scan output port.
TDI	22	JTAG Data scan input port.
TMS	23	JTAG Scan select input.
TCK	24	JTAG Scan clock input.
SA1	26	Slave address select.
SA2	27	Slave address select.
SCL	28	Standard I²C bus serial clock input.
SDA	30	Standard I²C bus serial data input/output.
$\overline{\text{RESET}}$	34	Master reset. This is an asynchronous, active low, input signal and must be asserted for a minimum 200ns in order to reset the VP5511A.
REFSQ	35	Reference square wave input used only during Genlock mode.
VREF	50	Voltage reference output. This output is nominally 1·0V and should be decoupled with a 100nF capacitor to GND.
DAC GAIN	51	DAC full scale current control. A resistor connected between this pin and GND sets the magnitude of the video output current. An internal loop amplifier controls a reference current flowing through this resistor so that the voltage across it is equal to the Vref voltage.
LUMACOMP	52	Luma DAC compensation. A 100nF ceramic capacitor must be connected between pin 52 and pin 53.
LUMAOUT	54	True luminance, composite and chrominance video signal outputs. These are high impedance current source outputs. A DC path to GND must exist from each of these pins.
COMPOUT	56	
CHROMAOUT	58	
COMPCOMP	60	Composite DAC compensation. A 100nF ceramic capacitor must be connected between pin 60 and pin 59.
NOT USED	61, 64	
VDD	1, 12, 16, 20, 29, 32, 33, 37, 48	Positive supply input. All VDD pins must be connected.
AVDD	53, 59 62, 63	Analog positive supply input. All AVDD pins must be connected.
GND	2, 11, 13, 14, 19, 25, 31, 36, 38, 47	Negative supply input. All GND pins must be connected.
AGND	49, 55, 57	Negative supply input. All AGND pins must be connected.

All other pins are N/C and should not be connected.

REGISTERS MAP

See Register Details for further explanations.

ADDRESS hex	REGISTER NAME	7	6	5	4	3	2	1	0	R/W	DEFAULT hex
	BAR	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	W	
00	PART ID2	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	R	13
01	PART ID1	ID0F	ID0E	ID0D	ID0C	ID0B	ID0A	ID09	ID08	R	66
02	PART ID0	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00	R	57
03	REV ID	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	R	AA
04	GCR	-	-	YCDELAY	RAMPEN	-	-	VFS1	VFS0	R/W	00
05	VOCR	-	CLAMPDIS	CHRBW	SYNCDIS	BURDIS	LUMDIS	CHRDIS	PEDEN	R/W	00
06	HANC	-	-	DFI2	DFI1	DFI0	Reserved	Reserved	ACTREN	*	00
07	ANCID	AN7	AN6	AN5	AN4	AN3	AN2	AN1	PARITY	R/W	00
08	SC_ADJ	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	R/W	97
09	FREQ2	FR17	FR16	FR15	FR14	FR13	FR12	FR11	FR10	R/W	87
0A	FREQ1	FR0F	FR0E	FR0D	FR0C	FR0B	FR0A	FR09	FR08	R/W	C1
0B	FREQ0	FR07	FR06	FR05	FR04	FR03	FR02	FR01	FR00	R/W	F1
0C	SCHPHM	-	-	-	-	-	-	-	SCH8	R/W	00
0D	SCHPHL	SCH7	SCH6	SCH5	SCH4	SCH3	SCH2	SCH1	SCH0	R/W	00
0E to 1F	Reserved										
20	GPPCTL	CTL7	CTL6	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	W	FF
21	GPPRD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	R	-
22	GPPWR	WR7	WR6	WR5	WR4	WR3	WR2	WR1	WR0	W	00
23 to EF	Not used										
F0	CCREG1	-	F1W1D6	F1W1D5	F1W1D4	F1W1D3	F1W1D2	F1W1D1	F1W1D0	R/W	00
F1	CCREG2	-	F1W2D6	F1W2D5	F1W2D4	F1W2D3	F1W2D2	F1W2D1	F1W2D0	R/W	00
F2	CCREG3	-	F2W1D6	F2W1D5	F2W1D4	F2W1D3	F2W1D2	F2W1D1	F2W1D0	R/W	00
F3	CCREG4	-	F2W2D6	F2W2D5	F2W2D4	F2W2D3	F2W2D2	F2W2D1	F2W2D0	R/W	00
F4	CC_CTL	-	-	-	-	F2ST	F1ST	F2EN	F1EN	R/W	00
F8	HSOFFL	HSOFF7	HSOFF6	HSOFF5	HSOFF4	HSOFF3	HSOFF2	HSOFF1	HSOFF0	R/W	7E
F9	HSOFFM	-	-	-	-	-	-	HSOFF9	HSOFF8	R/W	00
FD	GPSDAC	-	-	LUMADIS	CHRMDIS		LUMCHKI	CHRCKHI	CMPCKHI	R/W	38
FE	GPSTST	PROGRESS	BISTO	DIGSH	TSTBLEV	STSYNCLO	-	CTRLC_1	CTRLC_0	R/W	00
FF	GPSCTL	FSC4SEL	GENDITH	GENLKEN	NOLOCK	PALIDEN	TSURST	CHRMCLIP	TRSEL	R/W	00

Table.1 Register map

NOTE * For register HANC, bits 3, 4 and 5 are read only. Bits 1 and 2 are reserved. N/A = not applicable.

Standard	Lines/ field	Field freq. HZ	Number of pixels/line at 27MHz	Horizontal freq. kHz. f_H	Subcarrier freq. kHz. f_{SC}	f_{SC}/f_H	SC_ADJ register hex	FREQ2-0 registers hex
NTSC (default)	525	59.94	1716	15.734266	3.57954545	(455/2)	xx	87 C1 F1
PAL-B, G, H, I	625	50	1728	15.625000	4.43361875	(1135/4+1/625)	9C	A8 26 2B
PAL-M	525	59.94	1716	15.734266	3.57561189	(909/4)	xx	87 9B C0
PAL-N (Argentina)	625	50	1728	15.625000	3.58205625	(917/4+1/625)	57	87 DA 51

Table.2 Line, field and subcarrier standards and register settings

xx = don't care.

The calculation of the FREQ register value is according to the following formula:-

$$FREQ = 2^{26} \times f_{SC}/f_{SC/PXCK}\ \text{hex, where PXCK} = 27.00\text{MHz}$$

Both NTSC and PAL-M values are rounded UP from the decimal number. PAL-B, D, G, H, I and N (Argentina) are rounded DOWN. The SC_ADJ value is derived from the adjustment needed to be added after 8 fields to ensure accuracy of the Subcarrier frequency. Note the SC_ADJ value of 9C required for PAL-B, D, G, H, I, is different to the default state of the register.

REGISTER DETAILS

BAR — **Base register**
RA7-0 — Register address.

PART ID 2-0 — **Part number**
ID17-00 — Chip part identification (ID) number.

REV ID — **Revision number**
REV7-0 — Chip revision ID number.

GCR — **Global Control**
YCDELAY — Luma to Chroma delay.
High = 37ns luma delay, this may be used to compensate for group delay in external filters.
Low = normal operation (default).

RAMPEN — Modulated ramp enable.
High = ramp output for differential phase and gain measurements. A 27MHz clock must be applied to PXCK pin.
Low = normal operation (default).

VFS1-0 — Video format select

VFS1	VFS0	
0	0	NTSC (default)
0	1	PAL-B, D, G,H,I,N(Argentina)
1	0	PAL-M
1	1	Reserved

VOCR — **Video Output Control**
CLAMPDIS — High = Clamp signal disable
Low = normal operation with clamp signal enabled (default).

CHRBW — Chroma bandwidth select.
High = ±1·3MHz.
Low = ±650kHz (default)

SYNCDIS — High = Sync disable (in composite video signal). COMPSYNC is not affected.
Low = normal operation with sync enabled (default).

BURDIS — High = Chroma burst disable.
Low = normal operation, with burst enabled (default).

LUMDIS — High = Luma input disable - force black level with synchronisation pulses maintained.
Low = normal operation, with Luma input enabled (default).

CHRDIS — High = Chroma input disable - force monochrome.
Low = normal operation, with Chroma input enabled (default).

PEDEN — High = Pedestal (set-up) enable a 7·5 IRE pedestal on lines 23-262 and 286-525. Valid for NTSC/PAL-M only

HANC — **Horizontal Ancillary Data Control**
DFI2-0(read only) — Digital Field Identification, 000=Field1
ANCTREN — Ancillary timing reference enable. When High use FIELD COUNT from ancillary data stream. When low, data is ignored.

ANCID — **Ancillary data ID**
AN7-1 — Ancillary data ID
AN0 — Parity bit (odd)
Only ancillary data in REC 656 data stream with the same ID as this byte will be decoded by the VP5511A to produce H and V synchronisation and FIELD COUNT.

SC_ADJ — **Sub Carrier Adjust**
SC7-0 — Sub carrier frequency seed value, see table 2.

FREQ2-0 — **Sub carrier frequency**
FR17-00 — 24 bit Sub carrier frequency programmed via I²C bus, see table 2. FREQ2 is the most significant byte (MSB).

SCHPHM-L — **Sub carrier phase offset**
SCH9-0 — 9 bit Sub carrier phase relative to the 50% point of the leading edge of the horizontal part of composite sync. SCHPHM bit 0 is the MSB. The nominal value is zero. This register is used to compensate for delays external to the VP5511A.

GPPCTL — **General purpose port control**
CTL7-0 — Each bit controls port direction
Low = output High = input

GPPRD — **General purpose port read data**
RD7-0 — I²C bus read from general purpose port (only INPUTS defined in GPPCTL)

GPPWR — **General purpose port write data**
WR7-0 — I²C bus write to general purpose port (only OUTPUTS defined in GPPCTL)

CCREG1 — **Closed Caption register 1**
F1W1D6-0 — Field one (line 21), first data byte

CCREG2 — **Closed Caption register 2**
F1W2D6-0 — Field one (line 21), second data byte

CCREG3 — **Closed Caption register 3**
F2W2D6-0 — Field two (line 284), first data byte

CCREG4 — **Closed Caption register 4**
F2W2D6-0 — Field two (line 284), second data byte

CCCTL — **Closed Caption control register**
F1ST — Field one (line 21) status
High = data has been encoded
Low = new data has been loaded to CCREG1-2

F2ST — Field two (line 284) status
High = data has been encoded
Low = new data has been loaded to CCREG3-4

F1EN — Closed Caption field one (line 21)
High = enable Low = disable (default)

F2EN — Closed Caption field two (line 284)
High = enable Low = disable (default)

HSOFFM-L
HSOFF9-0 — **HS offset**
This is a 10 bit number which allows the user to offset the start of digital data input with reference to the pulse HS.

GPSDAC — **DAC test register**
LUMADIS — 1 = Normal operation
0 = Luma DAC input set zero

CHRMDIS — 1 = Normal operation
0 = Chroma DAC input set zero

LUMCKHI — 1 = Luma DAC clock input set to '1'

CHRCKHI — 0 = Normal operation
1 = Chroma DAC clock input set to '1'

GPSCTL — **GPS Control**
FSC4SEL — When high, REFSQ = 4xFSC and GPP bit D6 is forced to become an input for a SCSYNC signal (high = reset), which provides a synchronous phase reset for FSC divider. Low = normal operation with REFSQ = 1xFSC. (default).

GENDITH — 1 = Gen lock dither added.

GENLKEN — High = enable Genlock to REFSQ signal input.
Low = internal subcarrier generation (default).

NOLOCK — Genlock status bit (read only)
Low = Genlocked.
High = cannot lock to REFSQ. This bit is cleared by reading and set again if lock cannot be attained.

PALIDEN — High = enable external PAL ID phase control and GPP bit D7 is forced to become an input for PAL ID switch signal, (GPP bit D7 - Low = +135°, High = -135°).
Low = normal operation, internal PAL ID phase switch is used (default).

TSURST — High = chip soft reset. Registers are NOT reset to default values.
Low = normal operation (default).

CHRMCLIP — High = enable clipping of chroma data when luma goes below black level and is clipped.
Low = no chroma clipping (default).

TRSEL — High = master mode, GPP bits D0 - 4 are forced to become a video timing port with VS, HS and FIELD outputs.
Low = slave mode, timing from REC656.

I²C BUS CONTROL INTERFACE

I²C bus address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
0	0	0	1	1	SA2	SA1	X

The serial microprocessor interface is via the bi-directional port consisting of a data (SDA) and a clock (SCL) line. It is compatible to the Philips I²C bus standard (Jan. 1992 publication number 9398 393 40011). The interface is a slave transmitter - receiver with a sub-address capability. All communication is controlled by the microprocessor. The SCL line is input only. The most significant bit (MSB) is sent first. Data must be stable during SCL high periods.

A bus free state is indicated by both SDA and SCL lines being high. START of transmission is indicated by SDA being pulled low while SCL is high. The end of transmission, referred to as a STOP, is indicated by SDA going from low to high while SCL is high. The STOP state can be omitted if a repeated START is sent after the acknowledge bit. The reading device acknowledges each byte by pulling the SDA line low on the ninth clock pulse, after which the SDA line is released to allow the transmitting device access to the bus.

The device address can be partially programmed by the setting of the pins SA1 and SA2. This allows the device to respond to one of four addresses, providing for system flexibility. The I²C bus address is seven bits long with the last bit indicating read / $\overline{\text{write}}$ for subsequent bytes.

The first data byte sent after the device address, is the sub-address - BAR (base address register). The next byte will be written to the register addressed by BAR and subsequent bytes to the succeeding registers. The BAR maintains its data after a STOP signal.

NTSC/PAL Video Standards

Both NTSC (4-field, 525 lines) and PAL (8-field, 625 lines) video standards are supported by the VP5511A. All raster synchronisation, colour sub-carrier and burst characteristics are adapted to the standard selected. The VP5511A generates outputs which follow the requirements of SMPTE 170M and CCIR 624 for PAL signals.

The device supports the following:
NTSC,
PAL B, D, G, H, I, N (Argentina) and M.

Video Blanking

The VP5511A automatically performs standard composite video blanking. Lines 1-9, 264-272 inclusive, as well as the last half of line 263 are blanked in NTSC mode. In

PAL mode, lines 1-5, 311-318, 624-625 inclusive, as well as the last half of line 623 are blanked.

The V bit within REC656 defines the video blanking when TRSEL (bit 0 of GPSCTL register) is set low. When in MASTER mode with TRSEL set high the video encoder is still enabled. Therefore if these lines are required to be blank they must have no video signal input.

Interpolator

The luminance and chrominance data are separately passed through interpolating filters to produce output sampling rates double that of the incoming pixel rate. This reduces the sinx/x distortion that is inherent in the digital to analog converters and also simplifies the analog reconstruction filter requirements.

Digital to Analog Converters

The VP5511A contained three 9 bit digital to analog converters which produce the analog video signals. The DACs use a current steering architecture in which bit currents are routed to one of two outputs; thus the DAC has true and complementary outputs. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed. An on-chip voltage reference of 1.0V (typ.) provides the necessary biasing. However, the VP5511A may be used in applications where an external 1V reference is provided on the VREF pin, to adjust the video levels. In this case, the external reference should be temperature compensated and provide a low impedance output.

The full-scale output currents of the DACs is set by external 730Ω resistor between the DACGAIN and VSS pins. An on-chip loop amplifier stabilises the full-scale output current against temperature and power supply variations.

The analog outputs of the VP5511A are capable of directly driving doubly terminated 75Ω load then the DACGAIN resistor is simply doubled.

Luminance, Chrominance and Composite Video Outputs

The Luminance video output (LUMAOUT pin 54) drives a 37.5Ω load at 1.0V, sync tip to peak white. It contains only the luminance content of the image plus the composite sync pulses. In the NTSC mode, a set-up level offset can be added during the active video portion of the raster.

The Chrominance video output (CHROMAOUT pin 58) drives a 37.5Ω load at levels proportional in amplitude to the luma output (40 IRE pk-pk burst). This output has a fixed offset current which will produce approximately a 0.5V DC bias across the 37.5Ω load. Burst is injected with the appropriate timing relative to the luma signal.

The composite video output (COMPOUT pin 56) will also drive a 37.5Ω loas at 1.0V, sync tip to peak white. It contains both the luminance and chrominance content of the signal plus the composite sync pulses.

Output sinx/x compensation filters are required on all video output, as shown in the typical application diagram, see figs. 8 & 9.

Video Timing - Slave sync mode

The VP5511A has an internal timing generator which produces video timing signals appropriate to the mode of operation. In the default (power up) slave mode, all timing signals are derived from the input clock, PXCK, which must be derived from a crystal controlled oscillator. Input pixel data is latched on the rising edge of the PXCK clock.

The video timing generator produces the internal blanking and burst gate pulses, together with the composite sync output signal, using timing data (TRS codes) from the Ancillary data stream in the REC656 input signal, (when TRSEL (bit 0 of GPSCTL register) is set low).

Video Timing - Master sync mode

When TRSEL (bit 0 of GPSCTL register) is set high, the VP5511A operates in a MASTER sync mode, all REC656 timing reference codes are ignored and GPP bits D0 - 4 become a video timing port with VS, HS and FIELD outputs. The PXCK signal is, however, still used to generate all internal clocks. When TRSEL is set high, the direction setting of bits 4 - 0 of the GPPCTL register is ignored.

VS is the start of the field sync datum in the middle of the equalisation pulses. HS is the line sync which is used by the preceding MPEG2 decoder to define when to output digital video data to the VP5511A. The position of the falling edge of HS relative to the first data Cb0, can be programmed in HSOFFM-L registers, see fig. 4.

HS offset

The position of the falling edge of HS relative to the first data Cb0, can be programmed in HSOFFM-L registers, see figure 4, this is called the pipeline delay and may need adjusting for a particular application. This is done by programming a 10 bit number called HSOFF into the HSOFFM and HSOFFL registers, HSOFFM being the most significant two bits and HSOFFL the least significant eight bits. A default value of 07EH is held in the registers.

The value to program into HSOFF can be looked up in tables 3 &4:

Nck	HSOFF	Comment
0 to 120	126 to 6	HS normal (64 cks)
121 to 138	863 to 801	HS pulse shortened*
184 to 857	800 to 127	HS normal (64 cks)

Table.3 for NTSC and PAL-M

Nck	HSOFF	Comment
0 to 131	137 to 6	HS normal (64 cks)
132 to 194	869 to 807	HS pulse shortened*
195 to 863	806 to 138	HS normal (64 cks)

Table.4 for PAL-B, D, G, H, I, N

where Nck = number of 13.5MHz clock cycles between the falling edge of HS and Cb0 (first data I/P on PD7-0) see fig. 4. Decreasing HSOFF advances the HS pulse (numbers are in decimal).

*HS pulse shortened means that the width of the pulse will be less than the normal 64 13.5MHz clock cycles.

The interruption in the sequence of values is because the HS signal is jumping across a line boundary to the previous line as the offset is increased. The register default value is 7EH and this sets Nck to 0, ie. the HS negative edge and Cb0 are co-incident in NTSC mode.

Genlock using REFSQ input

The VP5511A can be Genlocked to another video source by setting GENLKEN high (in GPSCTL register) and feeding a phase coherent sub carrier frequency signal into REFSQ. Under normal circumstances, REFSQ will be the same frequency as the sub carrier. But by setting FSC4SEL high (in GPSCTL register), a 4 x sub carrier frequency signal may be input to REFSQ. In this case, the Genlock circuit can be reset to the required phase of REFSQ, by supplying a pulse to SCSYNC (pin 9). The frequency of SCSYNC can be at sub carrier frequency, but once per line, or once per field could be adequate, depending on the application. When GENLKEN is set high, the direction setting of bit 6 in the GPPCTL register is igonred.

PALID Input

When in Genlock mode with GENLKEN set high (in GPSCTL register), the VP5511A requires a PAL phase identification signal, to define the correct phase on every line. This is supplied to PALID input (pin 10), High = -135° and low = +135°. The signal is asynchronous and should be changed before the sub carrier burst signal. PALID input is enabled by setting PALIDEN high (in GPSCTL register). When GENLKEN is high, the direction setting of bit 7 of the GPPCTL register is ignored

Master Reset

The VP5511A must be initialised with the $\overline{\text{RESET}}$ pin 34. This is an asynchronous active low signal and must be active for a minimum of 200ns in order for the VP5511A to be reset. The device resets to line 64, start of horizontal sync (i.e. line blanking active). There is no on-chip power on reset circuitry.

Line 21 coding

Two bytes of data are coded on the line 21 of each field, see figure 7. In the NTSC Closed Caption service, the default state is to code on line 21 of field one only. An additional service can also be provided using line 21 (284) of the second field. The data is coded as NRZ with odd parity, after a clock run-in and framing code. The clock run-in frequency = 0.5034965MHz which is related to the nominal line period, D = H / 32.

$$D = 63.55555556 / 32\mu s$$

Two data bytes per field are loaded via I2C bus registers CCREG1-4. Each field can be independently enabled by programming the enable bits in the control register (CC_CTL). The data is cleared to zero in the Closed Caption shift registers after it has been encoded by the VP5511A. A software read of the field count in register HANC should be made to ensure it has incremented by 2 before sending the next pair of data bytes. Otherwise, the existing Closed Caption data output could be overwritten. If a transmission slot is missed it (ie. no data received) the encoder will send Null characters. Null characters are invisible to a closed caption reciever. The MSB (bit 7) is the parity bit and is automatically added by the encoder.

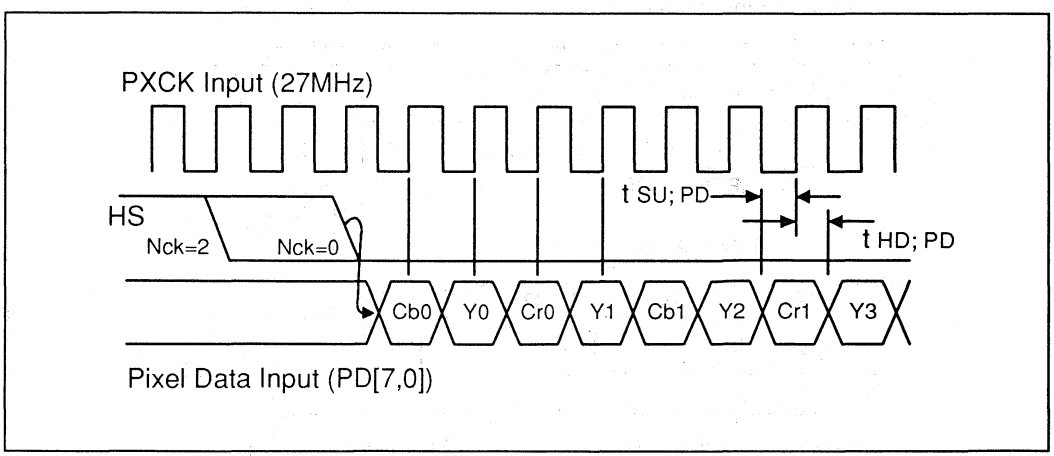


Fig.4 REC 656 interface with HS output timing

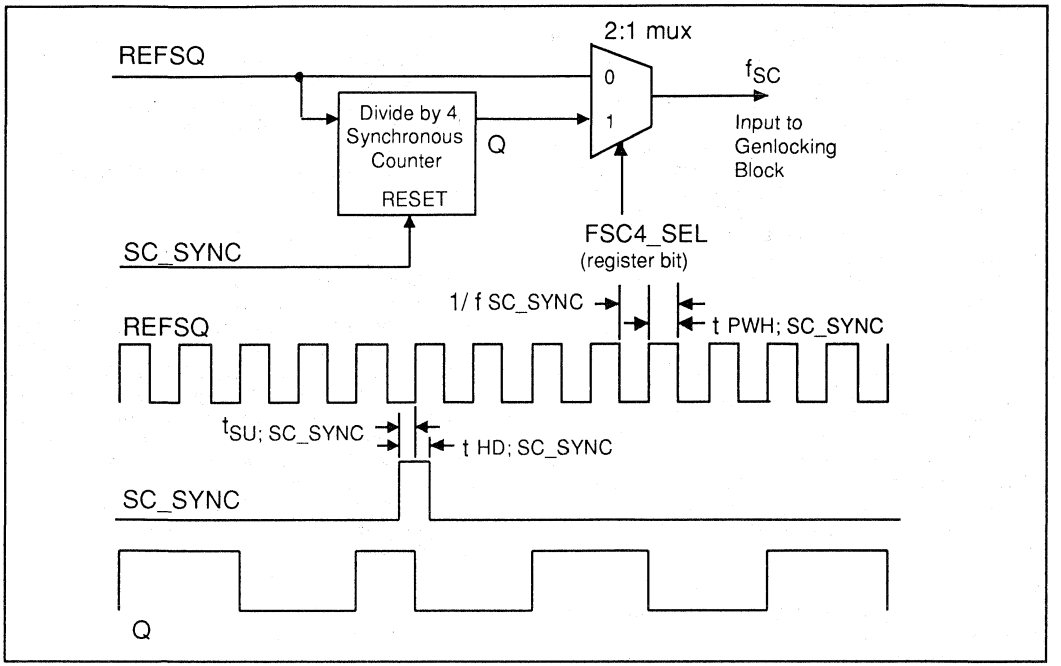


Fig.5 REFSQ and SC_SYNC input timing

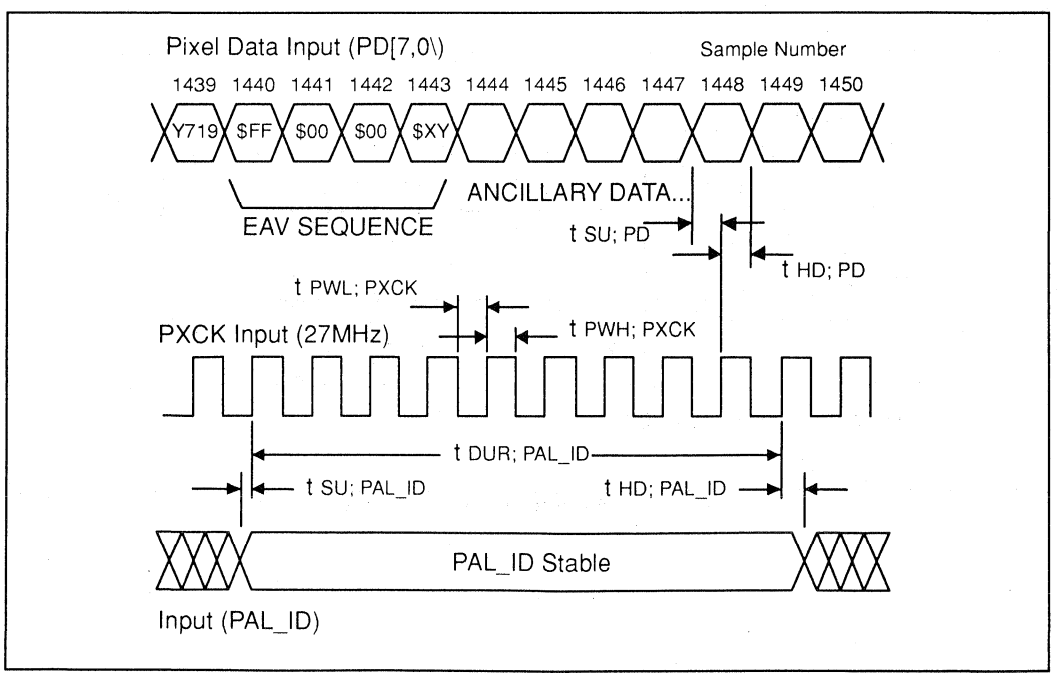


Fig.6 PAL_ID input timing

TIMING INFORMATION

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Units
Master clock frequency (PXCK input)		f_{PXCK}		27.0		MHz
PXCX pulse width, HIGH		$t_{PWH;\ PXCK}$	10			ns
PXCX pulse width, LOW		$t_{PWL;\ PXCK}$	14.5			ns
PXCX rise time	10% to 90% points	t_{RP}			TBD	ns
PXCX fall time	90% to 10% points	t_{FP}			TBD	ns
PD7-0 set up time		$t_{SU;PD}$	10			ns
PD7-0 hold time		$t_{HD;PD}$	5			ns
SC_SYNC set up time		$t_{SU;SC\_SYNC}$	10			ns
SC_SYNC hold time		$t_{HD;SC\_SYNC}$	0			ns
PAL_ID set up time		$t_{SU;PAL\_ID}$	10			ns
PAL_ID hold time		$t_{HD;PAL\_ID}$	0			ns
PAL_ID duration		$t_{DUR;PAL\_ID}$	9			PXCX periods
Output delay	PXCK to COMPSYNC PXCK to CLAMP	t_{DOS}			25	ns

Note: Timing reference points are at the 50% level. Digital C_{LOAD} <40pF.

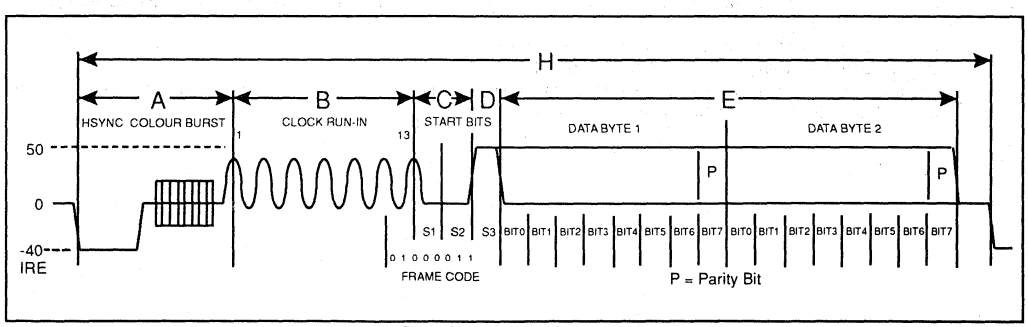


Fig.7 Closed Capation format

Interval	Description	Encoder minimum	Encoder nominal	Encoder maximum
A	H-sync to clock run-in	10.250µs	10.500µs	10.750µs
B	Clock run-in[2,3]		6.5D (12.910µs)	
C	Clock run-in to third start bit[3]		2.0D (3.972µs)	
D	Data bit[1,3]		1.0D (1.986µs)	
E	Data characters[4]		16.0D (31.778µs)	
H	Horizontal line[1]		32.0D (63.556)	
	Rise / fall time of data bit transitions[5]		0.240µs	0.288µs
	Data bit high (logic level one)[6] Clock run-in maximum	48 IRE	50 IRE	52 IRE
	Data bit low (logic level zero)[6] Clock run-in minimum	0 IRE	0 IRE	2 IRE
	Data bit differential (high - low) Clock run-in differential (max. - min)	48 IRE	50 IRE	52 IRE

Table. 5 Closed Caption data timing. (source EIA R - 4.3 Sept 16 1992)

Notes

1. The Horizontal line frequency f_H is nominally 15734.26Hz ±0.05Hz. Interval D shall be adjusted to $D = 1/(f_H \times 32)$ for the instantaneous f_H at line 21.
2. The clock run-in signal consists of 7.0 cycles of a 0.5034965MHz (1/D) sine wave when measured from the leading to trailing 0 IRE points. The sine wave is to be symmetrical about the 25 IRE level.
3. The negative going midpoints (half amplitude) of the clock run-in shall be coherent with the midpoints (half amplitude) of the Start and Data bit transitions.
4. Two characters, each consisting of 7 data bits and 1 odd parity bit.
5. 2 T Bar, measured between the 10% and 90% amplitude points.
6. The clock run-in maximum level shall not differ from the data bit high level by more than ±1 IRE. The clock run-in minimum level shall not differ from the data bit low level by more than ±1 IRE.

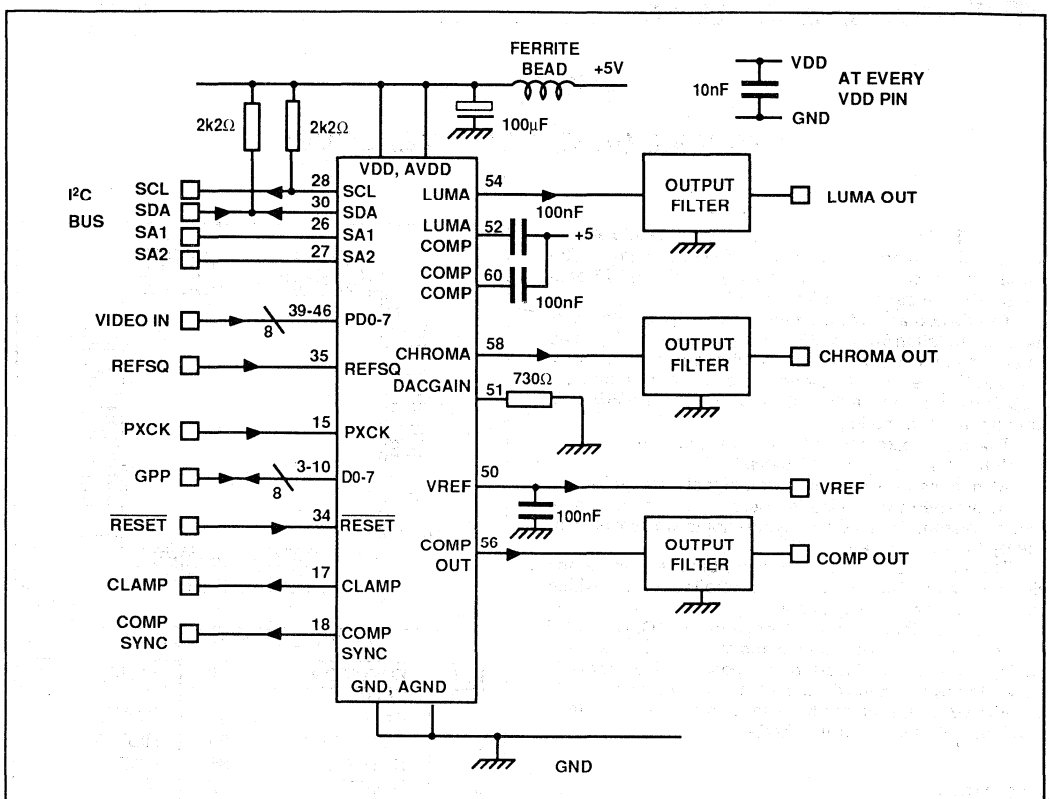


Fig.8 Typical application diagram, SLAVE mode. (Output filter - see Fig.9)

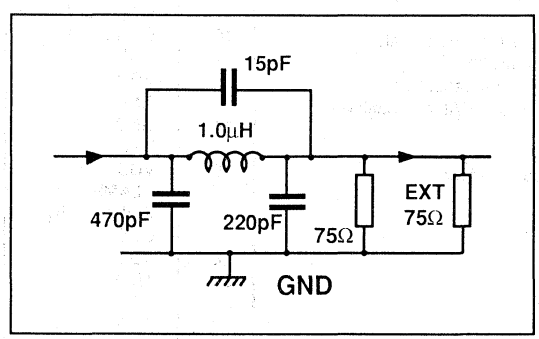


Fig.9 Output reconstruction filter

VP551D

NTSC/PAL DIGITAL VIDEO ENCODER

The VP551 converts digital Y, Cr, Cb, data into analog NTSC/PAL composite video and S-video signals The outputs are capable of driving doubly terminated 75 ohm loads with standard video levels.

The device accepts data inputs complying with CCIR Recommendation 601 and 656. The data is time multiplexed on an 8 bit bus at 27MHz and is formatted as Cb, Y, Cr, Y (i.e. 4:2:2). The video blanking and sync information from REC 656 is included in the data stream when the VP551 is working in slave mode.

The output pixel rate is 27MHz and the input pixel rate is half this frequency, i.e. 13.5MHz.

All necessary synchronisation signals are generated internally when the device is operating in master mode. Digital horizontal and vertical sync outputs are available for use by the host system.

The rise and fall times of sync, burst envelope and video blanking are internally controlled to be within composite video specifications.

Two 9 bit digital to analog converters (DACs) are used to convert the digital luminance and chrominance data into analog signals. An inverted composite video signal is generated by summing the complementary current outputs of each DAC. An internally generated reference voltage provides the biasing for the DACs.

FEATURES

- Converts Y, Cr, Cb data to analog composite video and S-video
- Supports CCIR recommendations 601 and 656
- All digital video encoding
- Selectable master/slave mode for sync signals
- Switchable chrominance bandwidth
- Switchable pedestal with gain compensation
- SMPTE 170M NTSC or CCIR 624 PAL compatible outputs
- GENLOCK mode
- I²C bus serial microprocessor interface
- 64 PQFP package

APPLICATIONS

- Digital Cable TV
- Digital Satellite TV
- Multi-media
- Video games
- Karaoke
- Digital VCRs

ORDERING INFORMATION

VP551D/CG/GP1R

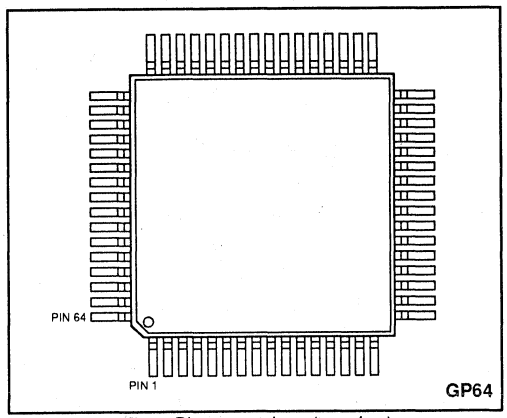


Fig.1 Pin connections (top view)

PIN	FUNCTION	PIN	FUNCTION
1	VDD	33	VDD
2	GND	34	$\overline{\text{RESET}}$
3	D0 (VS O/P)	35	REFSQ
4	D1 (HS O/P)	36	GND
5	D2 (FC0 O/P)	37	VDD
6	D3 (FC1 O/P)	38	GND
7	D4 (FC2 O/P)	39	PD7
8	D5	40	PD6
9	D6 (SCSYNC I/P)	41	PD5
10	D7 (PALID I/P)	42	PD4
11	GND	43	PD3
12	VDD	44	PD2
13	GND	45	PD1
14	GND	46	PD0
15	PXCK	47	GND
16	VDD	48	VDD
17	CLAMP	49	AGND
18	COMPSYNC	50	VREF
19	GND	51	DACGAIN
20	VDD	52	LUMACOMP
21	TDO	53	AVDD
22	TDI	54	LUMAOUT
23	TMS	55	AGND
24	TCK	56	$\overline{\text{COMPOUT}}$
25	GND	57	AGND
26	SA1	58	CHROMAOUT
27	SA2	59	AVDD
28	SCL	60	CHROMACOMP
29	VDD	61	N/C
30	SDA	62	AVDD
31	GND	63	AVDD
32	VDD	64	N/C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC CHARACTERISTICS

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Units
Digital Inputs TTL compatible (except SDA, SCL)						
Input high voltage		VIN	2.0			V
Input low voltage		VIL			0.8	V
Digital Inputs SDA, SCL						
Input high voltage		VIH	0.7 VDD			V
Input low voltage		VIL			0.3 VDD	V
Input high current	VIN = VDD	IIH			10	µA
Input low current	VIN = VSS	IIL			-10	µA
Digital Outputs CMOS compatible						
Output high voltage	IOH = -1mA	VOH	3.7			V
Output low voltage	IOL = +4mA	VOL			0.4	V
Digital Output SDA						
Output low voltage	IOL = +6mA	VOL			0.6	V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC CHARACTERISTICS DACs

Parameter	Symbol	Min.	Typ.	Max.	Units
Accuracy (each DAC)					
Integral linearity error	INL			±1.5	LSB
Diffential linearity error	DNL			±1	LSB
DAC matching error				±5	% grey
Monotonicity			guaranteed		
LSB size			66.83		µA
Internal reference voltage	V_{REF}	0.95	1.00	1.05	V
Internal reference voltage output impedance	Z_R		27k		Ω
Reference Current (V_{REF}/R_{REF}) R_{REF} = 730Ω	I_{REF}		1.3699		mA
DAC Gain Factor ($V_{OUT} = K_{DAC} \times I_{REF} \times R_L$). V_{OUT} = DAC code 511	K_{DAC}		24.93		
Peak Glitch Energy (see fig.3)			80		pV-s
CVBS (see note), Y and C - NTSC (pedestal enabled)					
Maximum output, relative to sync bottom			33.75		mA
White level relative to black level			17.64		mA
Black level relative to blank level			1.40		mA
Blank level relative to sync level			7.62		mA
Colour burst peak - peak			7.62		mA
DC offset (bottom of sync)			0.40		mA
CVBS, Y and C - PAL					
Maximum output			34.15		mA
White level relative to black level			18.71		mA
Black level relative to sync level			8.02		mA
Colour burst peak - peak			8.02		mA
DC offset (bottom of sync)			0.00		mA

Note: For the inverted CVBS output subtract the above currents from the maximum output (DAC code 511 = 34.12mA).
All figures are for: R_{REF} = 730Ω, R_L = 37.5Ω. When the device is set up in NTSC mode there is a +0.25% error in the PAL levels.
If R_L = 75Ω then R_{REF} = 1460Ω

ABSOLUTE MAXIMUM RATINGS

Supply voltage	VDD, AVDD	-0·3 to 7·0V
Voltage on any non power pin		-0·3 to VDD+0·3V
Ambient operating temperature		0 to 70°C
Storage temperature		-55°C to 150°C

Note: Stresses exceeding these listed under Absolute Maximum Ratings may induce failure. Exposure to Absolute Maximum Ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply voltage	VDD, AVDD	4.75	5.00	5.25	V
Power supply current (including analog outputs)	IDD		150		mA
Input clock frequency	PXCK	-50ppm	27.00	+50ppm	MHz
SCL clock frequency	fscl			500	kHz
Analog video output load			37.5		Ω
DAC gain resistor			730		Ω
Ambient operating temperature		0		70	°C

VIDEO CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units
Luminance bandwidth			5.5		MHz
Chrominance bandwidth (Extended B/w mode)			1.3		MHz
Chrominance bandwidth (Reduced B/w mode)			650		kHz
Burst frequency (NTSC)			3.57954545		MHz
Burst frequency (PAL-B, D,G, H, I)			4.43361875		MHz
Burst frequency (PAL-M)			3.57561149		MHz
Burst frequency (PAL-N Argentina)			3.58205625		MHz
Burst cycles (NTSC and PAL-M, N)			9		Fsc cycles
Burst cycles (NTSC and PAL-B, D, G, H,I)			10		Fsc cycles
Burst envelope rise / fall time (NTSC and PAL-M, N)			300		ns
Burst envelope rise / fall time (NTSC and PAL-B, D, G, H,I)			300		ns
Analog video sync rise / fall time (NTSC and PAL-M, N)			145		ns
Analog video blank rise / fall time (NTSC and PAL-B, D, G, H,I)			245		ns
Differential gain			1.5		% pk-pk
Differential phase			1		% pk-pk
Signal to noise ratio (unmodulated ramp)				-61	dB
Chroma AM signal to noise ratio (100% red field)				-56	dB
Chroma PM signal to noise ratio (100% red field)				-58	dB
Hue accuracy				2.5	%
Colour saturation accuracy				2.5	%
Residual sub carrier			-60		dB
Luminance / chrominance delay			10		ns

ESD COMPLIANCE

Pins	Test	Test Levels	Notes
All pins	Human body model	2kV on 100pF through 1k5Ω	Meets Mil-Std-883 Class 2
All pins	Machine model	200V on 200pF through 0Ω & 500nH	

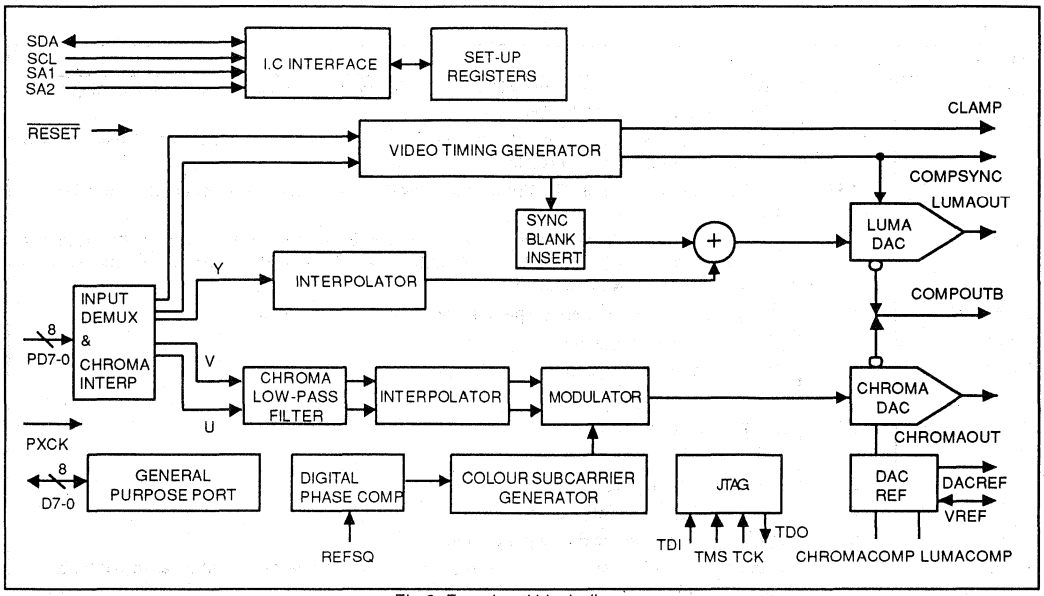


Fig.2 Functional block diagram

PIN DESCRIPTIONS

Pin Name	Pin No.	Description
PD0-7	39 - 46	8 Bit Pixel Data inputs clocked by PXCK. PD0 is the least significant bit, corresponding to Pin 46. These pins are internally pulled low.
D0-7	3 - 10	8 Bit General Purpose Port input/output. D0 is the least significant bit, corresponding to Pin 3. These pins are internally pulled low.
PXCK	15	27MHz Pixel Clock input. The VP551 internally divides PXCK by two to provide the pixel clock.
CLAMP	17	The CLAMP output signal is synchronised to COMPSYNC output and indicates the position of the BURST pulse, (lines 10-263 and 273-525 for NTSC and PAL-M; lines 6-310 and 319-623 for PAL-B,D, G,I,N(Argentina)).
COMPSYNC	18	Composite sync pulse output. This is an active low output signal.
TDO	21	JTAG Data scan output port.
TDI	22	JTAG Data scan input port.
TMS	23	JTAG Scan select input.
TCK	24	JTAG Scan clock input.
SA1	26	Slave address select.
SA2	27	Slave address select.
SCL	28	Standard I²C bus serial clock input.
SDA	30	Standard I²C bus serial data input/output.
$\overline{\text{RESET}}$	34	Master reset. This is an asynchronous active low input signal and must be asserted for a minimum of 200ns in order to reset the VP551.
REFSQ	35	Reference square wave input used only during Genlock mode.
VREF	50	Voltage reference output. This output is nominally 1·0V and should be decoupled with a 100nF capacitor to GND.
DAC GAIN	51	DAC full sacle current control. A resistor connected between this pin and GND sets the magnitude of the video output current. An internal loop amplifier control a reference current flowing through this resistor so that the voltage across it is equal to the Vref voltage.
LUMACOMP	52	Luma DAC compensation. A 100nF ceramic capacitor must be connected between pin 52 and pin 53.
LUMAOUT	54	True luminance, true chrominance and inverted composite video signal outputs. These are high impedance current source outputs. A DC path to GND must exist from each of these pins
COMPOUT	56	
CHROMAOUT	58	
CHROMA-COMP	60	Chroma DAC compensation. A 100nF ceramic capacitor must be connected between pin 60 and pin 59.
NOT USED	61, 64	
VDD	1, 12, 16, 20, 29, 32, 33, 37, 48	Positive supply input. All VDD pins must be connected.
AVDD	53, 59 62, 63	Analog positive supply input. All AVDD pins must be connected.
GND	2, 11, 13, 14, 19, 25, 31, 36, 38, 47	Negative supply input. All GND pins must be connected.
AGND	49, 55, 57	Negative supply input. All AGND pins must be connected.

REGISTERS MAP

See Register Details for further explanations.

ADDRESS hex	REGISTER NAME	7	6	5	4	3	2	1	0	R/W	DEFAULT hex
	BAR	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	W	
00	PART ID2	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	R	13
01	PART ID1	ID0F	ID0E	ID0D	ID0C	ID0B	ID0A	ID09	ID08	R	66
02	PART ID0	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00	R	57
03	REV ID	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	R	AA
04	GCR	-	-	YCDELAY	RAMPEN	-	-	VFS1	VFS0	R/W	00
05	VOCR	-	CLAMPDIS	CHRBW	SYNCDIS	BURDIS	LUMDIS	CHRDIS	PEDEN	R/W	00
06	HANC	-	-	DFI2	DFI1	DFI0	Reserved	Reserved	ACTREN	*	00
07	ANCID	AN7	AN6	AN5	AN4	AN3	AN2	AN1	PARITY	R/W	00
08	SC_ADJ	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	R/W	97
09	FREQ2	FR17	FR16	FR15	FR14	FR13	FR12	FR11	FR10	R/W	87
0A	FREQ1	FR0F	FR0E	FR0D	FR0C	FR0B	FR0A	FR09	FR08	R/W	C1
0B	FREQ0	FR07	FR06	FR05	FR04	FR03	FR02	FR01	FR00	R/W	F1
0C	SCHPHM	-	-	-	-	-	-	-	SCH8	R/W	00
0D	SCHPHL	SCH7	SCH6	SCH5	SCH4	SCH3	SCH2	SCH1	SCH0	R/W	00
0E to 1F	Reserved										
20	GPPCTL	CTL7	CTL6	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	W	FF
21	GPPRD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	R	-
22	GPPWR	WR7	WR6	WR5	WR4	WR3	WR2	WR1	WR0	W	00
23 to EF	Not used										
F0	Reserved									R/W	00
F1	Reserved									R/W	00
F2	Reserved									R/W	00
F3	Reserved									R/W	00
F4	Reserved									R/W	00
F8	HSOFFL	HSOFF7	HSOFF6	HSOFF5	HSOFF4	HSOFF3	HSOFF2	HSOFF1	HS0FF0	R/W	7E
F9	HSOFFM	-	-	-	-	-	-	HSOFF9	HSOFF8	R/W	00
FD	GPSDAC	-	-	LUMADIS	CHRMDIS		LUMCHKI	CHRCKHI	CMPCKHI	R/W	38
FE	GPSTST	PROGRESS	BISTO	DIGSH	TSTBLEV	STSYNCLO	-	CTRLC_1	CTRLC_0	R/W	00
FF	GPSCTL	FSC4SEL	GENDITH	GENLKEN	NOLOCK	PALIDEN	TSURST	CHRMCLIP	TRSEL	R/W	00

Table.1 Register map

NOTE * For register HANC, bits 3, 4 and 5 are read only. Bits 1 and 2 are reserved. N/A = not applicable.

Standard	Lines/ field	Field freq. HZ	Number of pixels/line at 27MHz	Horizontal freq. kHz. f_H	Subcarrier freq. kHz. f_{SC}	f_{SC}/f_H	SC_ADJ register hex	FREQ2-0 registers hex
NTSC (default)	525	59.94	1716	15.734266	3.57954545	(455/2)	xx	87 C1 F1
PAL-B, D, G, H, I	625	50	1728	15.625000	4.43361875	(1135/4+1/625)	9C	A8 26 2B
PAL-M	525	59.94	1716	15.734266	3.57561189	(909/4)	xx	87 9B C0
PAL-N (Argentina)	625	50	1728	15.625000	3.58205625	(917/4+1/625)	57	87 DA 51

Table.2 Line, field and subcarrier standards and register settings

xx = don't care.

The calculation of the FREQ register value is according to the following formula:-

$$FREQ = (2^{26} \times f_{SC}/f_H) / (\text{number of pixels/line}) \text{ hex}$$

Both NTSC and PAL-M values are rounded UP from the decimal number. PAL-B, D, G, H, I and N (Argentina) are rounded DOWN. The SC_ADJ value is derived from the adjustment needed to be added after 8 fields to ensure accuracy of the Subcarrier frequency. Note the SC_ADJ value of 9C required for PAL-B, D, G, H, I, is different to the default state of the register.

REGISTER DETAILS

BAR **Base register**
RA7-0 Register address.

PART ID 2-0 **Part number**
ID17-00 Chip part identification (ID) number.

REV ID **Revision number**
REV7-0 Chip revision ID number.

GCR **Global Control**
YCDELAY Luma to Chroma delay.
High = 37ns luma delay, this may be used to compensate for group delay in external filters.
Low = normal operation (default).

RAMPEN Modulated ramp enable.
High = ramp output for differential phase and gain measurements. A 27MHz clock must be applied to PXCK pin.
Low = normal operation (default).

VFS1-0 Video format select

VFS1	VFS0	
0	0	NTSC (default)
0	1	PAL-B,D,G,H,I,N(Argentina)
1	0	PAL-M
1	1	Reserved

VOCR **Video Output Control**
CLAMPDIS High = Clamp signal disable
Low = normal operation with clamp signal enabled (default).

CHRBW Chroma bandwidth select.
High = ±1·3MHz.
Low = ±650kHz (default)

SYNCDIS High = Sync disable (in composite video signal). COMPSYNC is not affected.
Low = normal operation with sync enabled (default).

BURDIS High = Chroma burst disable.
Low = normal operation, with burst enabled (default).

LUMDIS High = Luma input disable - force black level with synchronisation pulses maintained.
Low = normal operation, with Luma input enabled (default).

CHRDIS High = Chroma input disable - force monochrome.
Low = normal operation, with Chroma input enabled (default).

PEDEN High = Pedestal (set-up) enable a 7·5 IRE pedestal on lines 23-262 and 286-525. Valid for NTSC/PAL-M only

HANC **Horizontal Ancillary Data Control**
DFI2-0(read only) Digital Field Identification, 000=Field1
ANCTREN Ancillary timing reference enable. When High use FIELD COUNT from ancillary data stream. When low, data is ignored.

ANCID **Ancillary data ID**
AN7-1 Ancillary data ID
AN0 Parity bit (odd)
Only ancillary data in REC 656 data stream with the same ID as this byte will be decoded by the VP551 to produce H and V synchronisation and FIELD COUNT.

SC_ADJ **Sub Carrier Adjust**
SC7-0 Sub carrier frequency seed value, see table 2.

FREQ2-0 **Sub carrier frequency**
FR17-00 24 bit Sub carrier frequency programmed via I²C bus, see table 2. FREQ2 is the most significant byte (MSB).

SCHPHM-L **Sub carrier phase offset**
SCH9-0 9 bit Sub carrier phase relative to the 50% point of the leading edge of the horizontal part of composite sync. SCHPHM bit 0 is the MSB. The nominal value is zero. This register is used to compensate for delays external to the VP551.

GPPCTL **General purpose port control**
CTL7-0 Each bit controls port direction
Low = output High = input

GPPRD **General purpose port read data**
RD7-0 I²C bus read from general purpose port (only INPUTS defined in GPPCTL)

GPPWR **General purpose port write data**
WR7-0 I²C bus write to general purpose port (only OUTPUTS defined in GPPCTL)

HSOFFM-L **HS offset**
HSOFF9-0 This is a 10 bit number which allows the user to offset the start of digital data input with reference to the pulse HS.

GPSDAC **DAC test register**
LUMADIS 1 = Normal operation
0 = Luma DAC input set zero

CHRMDIS 1 = Normal operation
0 = Chroma DAC input set zero

LUMCKHI 1 = Luma DAC clock input set to '1'

CHRCKHI 0 = Normal operation
1 = Chroma DAC clock input set to '1'

GPSCTL **GPS Control**

FSC4SEL When high, REFSQ = 4xFSC and GPP bit D6 is forced to become an input for a SCSYNC signal (high = reset), which provides a synchronous phase reset for FSC divider. Low = normal operation with REFSQ = 1xFSC. (default).

GENDITH 1 = Gen lock dither added.

GENLKEN High = enable Genlock to REFSQ signal input.
Low = internal subcarrier generation (default).

NOLOCK Genlock status bit (read only)
Low = Genlocked.
High = cannot lock to REFSQ. This bit is cleared by reading and set again if lock cannot be attained.

PALIDEN High = enable external PAL ID phase control and GPP bit D7 is forced to become an input for PAL ID switch signal, (GPP bit D7 - Low = +135°, High = -135°).
Low = normal operation, internal PAL ID phase switch is used (default).

TSURST High = chip soft reset. Registers are NOT reset to default values.
Low = normal operation (default).

CHRMCLIP High = enable clipping of chroma data when luma goes below black level and is clipped.
Low = no chroma clipping (default).

TRSEL High = master mode, GPP bits D0 - 4 are forced to become a video timing port with VS, HS and FIELD outputs.
Low = slave mode, timing from REC656.

I²C BUS CONTROL INTERFACE

I²C bus address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
0	0	0	1	1	SA2	SA1	X

The serial microprocessor interface is via the bi-directional port consisting of a data (SDA) and a clock (SCL) line. It is compatible to the Philips I²C bus standard (Jan. 1992 publication number 9398 393 40011). The interface is a slave transmitter - receiver with a sub-address capability. All communication is controlled by the microprocessor. The SCL line is input only. The most significant bit (MSB) is sent first. Data must be stable during SCL high periods.

A bus free state is indicated by both SDA and SCL lines being high. START of transmission is indicated by SDA being pulled low while SCL is high. The end of transmission, referred to as a STOP, is indicated by SDA going from low to high while SCL is high. The STOP state can be omitted if a repeated START is sent after the acknowledge bit. The reading device acknowledges each byte by pulling the SDA line low on the ninth clock pulse, after which the SDA line is released to allow the transmitting device access to the bus.

The device address can be partially programmed by the setting of the pins SA1 and SA2. This allows the device to respond to one of four addresses, providing for system flexibility. The I²C bus address is seven bits long with the last bit indicating read / $\overline{\text{write}}$ for subsequent bytes.

The first data byte sent after the device address, is the sub-address - BAR (base address register). The next byte will be written to the register addressed by BAR and subsequent bytes to the succeeding registers. The BAR maintains its data after a STOP signal.

NTSC/PAL Video Standards

Both NTSC (4-field, 525 lines) and PAL (8-field, 625 lines) video standards are supported by the VP551. All raster synchronisation, colour sub-carrier and burst characteristics are adapted to the standard selected. The VP551 generates outputs which follow the requirements of SMPTE 170M and CCIR 624 for PAL signals.

The device supports the following:
NTSC,
PAL B, D, G, H, I, N (Argentina) and M.

Video Timing - Slave sync mode

The VP551 has an internal timing generator which produces video timing signals appropriate to the mode of operation. In the default (power up) slave mode, all timing signals are derived from the input clock, PXCK, which must be derived from a crystal controlled oscillator. Input pixel data is latched on the rising edge of the PXCK clock.

The video timing generator produces the internal blanking and burst gate pulses, together with the composite sync output signal, using timing data (TRS codes) from the Ancillary data stream in the REC656 input signal, (when TRSEL (bit 0 of GPSCTL register) is set low).

Video Timing - Master sync mode

When TRSEL (bit 0 of GPSCTL register) is set high, the VP551 operates in a MASTER sync mode, all REC656 timing reference codes are ignored and GPP bits D0 - 4 become a video timing port with VS, HS and FIELD outputs. The PXCK signal is, however, still used to generate all internal clocks. When TRSEL is set high, the direction setting of bits 4 - 0 of the GPPCTL register is ignored.

VS is the start of the field sync datum in the middle of the equalisation pulses. HS is the line sync which is used by the preceding MPEG2 decoder to define when to output digital video data to the VP551. The position of the falling edge of HS relative to the first data Cb0, can be programmed in HSOFFM-L registers, see table. 4.

Video Blanking

The VP551 automatically performs standard composite video blanking. Lines 1-9, 264-272 inclusive, as well as the last half of line 263 are blanked in NTSC mode. In PAL mode, lines 1-5, 311-318, 624-625 inclusive, as well as the last half of line 623 are blanked.

The V bit within REC656 defines the video blanking when TRSEL (bit 0 of GPSCTL register) is set low. When in MASTER mode with TRSEL set high the video encoder is still enabled. Therefore if these lines are required to be blank they must have no video signal input.

Interpolator

The luminance and chrominance data are separately passed through interpolating filters to produce output sampling rates double that of the incoming pixel rate. This reduces the sinx/x distortion that is inherent in the digital to analog converters and also simplifies the analog reconstruction filter requirements.

Digital to Analog Converters

The VP551 contains two 9 bit digital to analog converters which produce the analog video signals. The DACs use a current steering architecture in which bit currents are routed to one of two outputs; thus the DAC has true and complementary outputs. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed. An on-chip voltage reference of 1.0V (typ.) provides the necessary biasing. if required this can be overridden by an external reference.

The full-scale output currents of the DACs is set by external resistors between the DACGAIN and VSS pins. An on-chip loop amplifier stabilises the full-scale output current against temperature and power supply variations.

By summing the complementary luma and chroma DAC current outputs an inverted composite output is generated. Note that this signal has a DC offset and therefore usally needs to be capacitively coupled. The analog outputs of the VP551 are capable of directly driving doubly terminated 75Ω co-axial cable. If it is required only to drive a single 75Ω load then DACGAIN resistor is simply doubled.

Luminance, Chrominance and Composite Video Outputs

The Luminance video output (LUMAOUT pin 54) drives a 37.5Ω load at 1.0V, sync tip to peak white. It contains only the luminance content of the image plus the composite sync pulses. In the NTSC mode, a set-up level (pedestal) offset can be added during the active video portion of the raster. The pedestal is programmed by PEDEN bit in VOCR register.

The Chrominance video output (CHROMAOUT pin 58) drives a 37.5Ω load at levels proportional in amplitude to the luma output (40 IRE pk-pk burst). This output has a fixed offset current which will produce approximately a 0.5V DC bias across the 37.5Ω load. Burst is injected with the appropriate timing relative to the luma signal.

The inverted composite video output (COMPOUTB pin 56) will also drive a 37.5Ω loas at 1.0V, sync tip to peak white. It contains both the luminance and chrominance content of the signal plus the composite sync pulses.

Output sinx/x compensation filters are required on all video output, as shown in the typical application diagram, see figs. 6 & 7.

HS offset

The position of the falling edge of HS relative to the first data Cb0, can be programmed in HSOFFM-L registers, see figure 4, this is called the pipeline delay and may need adjusting for a particular application. This is done by programming a 10 bit number called HSOFF into the HSOFFM and HSOFFL registers, HSOFFM being the most significant two bits and HSOFFL the least significant eight bits. A default value of 07EH is held in the registers.

The value to program into HSOFF can be looked up in tables 3 &4:

Nck	HSOFF	Comment
0 to 120	126 to 6	HS normal (64 cks)
121 to 138	863 to 801	HS pulse shortened*
184 to 857	800 to 127	HS normal (64 cks)

Table.3 for NTSC and PAL-M

Nck	HSOFF	Comment
0 to 131	137 to 6	HS normal (64 cks)
132 to 194	869 to 807	HS pulse shortened*
195 to 863	806 to 138	HS normal (64 cks)

Table.4 for NTSC and PAL-B, D, G, H, I, N

**HS pulse shortened means that the width of the pulse will be less than the normal 64 13.5MHz clock cycles.*

where Nck = number of 13.5MHz clock cycles between the falling edge of HS and Cb0 (first data I/P on PD7-0) see fig. 4. Decreasing HSOFF advances the HS pulse (numbers are in decimal).

The interruption in the sequence of values is because the HS signal is jumping across a line boundary to the previous line as the offset is increased. The register default value is 7EH and this sets Nck to 0, ie. the HS negative edge and Cb0 are co-incident in NTSC mode.

Genlock using REFSQ input

The VP551 can be Genlocked to another video source by setting GENLKEN high (in GPSCTL register) and feeding a phase coherent sub carrier frequency signal into REFSQ. Under normal circumstances, REFSQ will be the same frequency as the sub carrier. But by setting FSC4SEL high (in GPSCTL register), a 4 x sub carrier frequency signal may be input to REFSQ. In this case, the Genlock circuit can be reset to the required phase of REFSQ, by supplying a pulse to SCSYNC (pin 9). The frequency of SCSYNC can be at sub carrier frequency, but once per line, or once per field could be adequate, depending on the application. When GENLKEN is SET high, the direction setting of bit 6 of the GPPCTL register is ignored.

PALID Input

When in Genlock mode with GENLKEN set high (in GPSCTL register), the VP551 requires a PAL phase identification signal, to define the correct phase on every line. This is supplied to PALID input (pin 10), High = -135° and low = +135°. The signal is asynchronous and should be changed before the sub carrier burst signal. PALID input is enabled by setting PALIDEN high (in GPSCTL register). When GENLKEN is high, the direction setting of bit 7 of the GPPCTL register is ignored

Master Reset

The VP551 must be initialised with the $\overline{\text{RESET}}$ pin 34. This is an asynchronous active low signal and must be active for a minimum of 200ns in order for the VP551 to be reset. The device resets to line 64, start of horizontal sync (i.e. line blanking active). There is no on-chip power on reset circuitry.

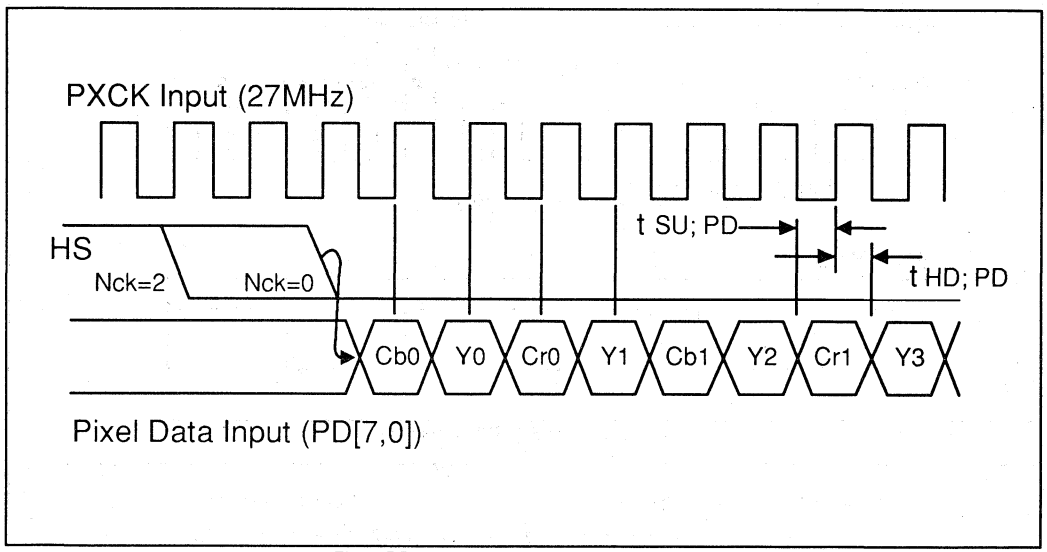


Fig.3 REC 656 interface with HS output timing

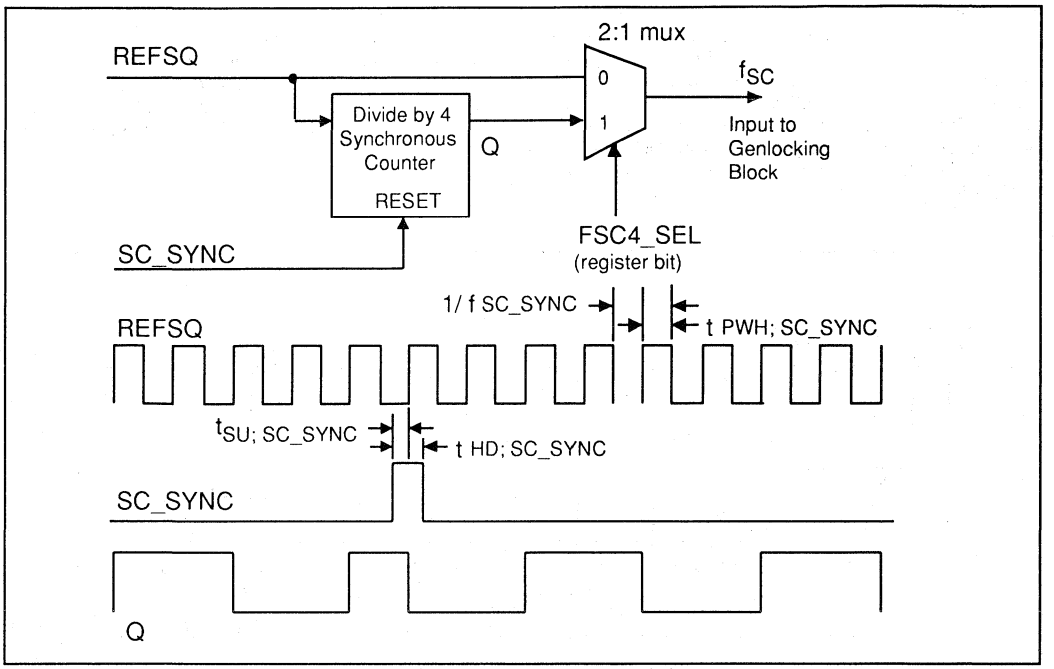


Fig.4 REFSQ and SC_SYNC input timing

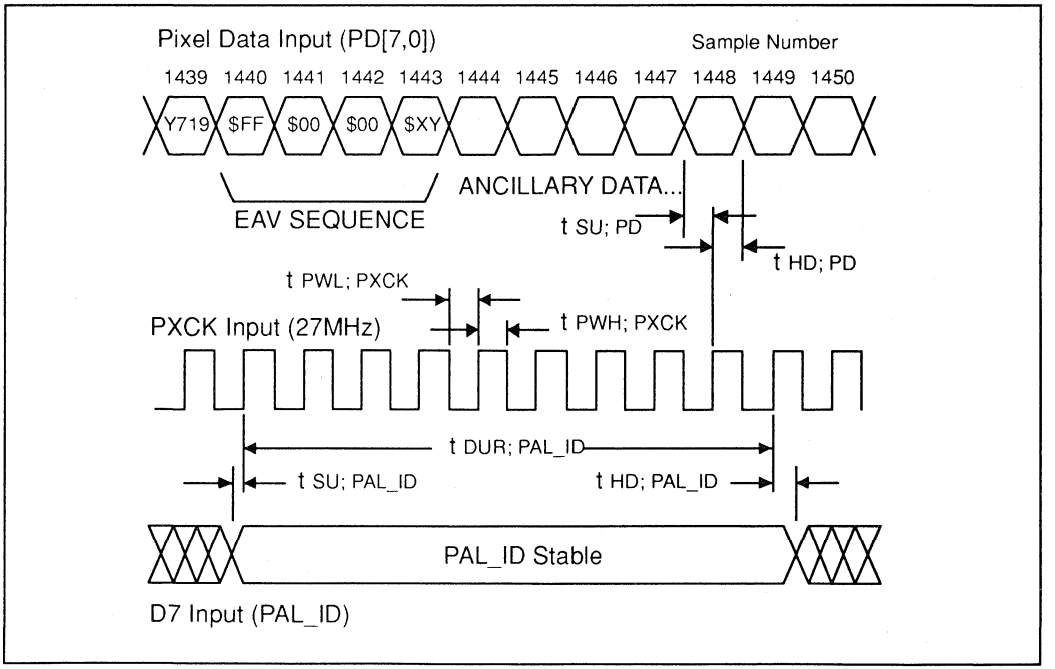


Fig.5 PAL_ID input timing

TIMING INFORMATION

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Units
Master clock frequency (PXCK input)		f_{PXCK}		27.0		MHz
PXCK pulse width, HIGH		$t_{PWH;\ PXCK}$	10			ns
PXCK pulse width, LOW		$t_{PWL;\ PXCK}$	14.5			ns
PXCK rise time	10% to 90% points	t_{RP}			TBD	ns
PXCK fall time	90% to 10% points	t_{FP}			TBD	ns
PD7-0 set up time		$t_{SU;PD}$	10			ns
PD7-0 hold time		$t_{HD;PD}$	5			ns
SC_SYNC set up time		$t_{SU;SC\_SYNC}$	10			ns
SC_SYNC hold time		$t_{HD;SC\_SYNC}$	0			ns
PAL_ID set up time		$t_{SU;PAL\_ID}$	10			ns
PAL_ID hold time		$t_{HD;PAL\_ID}$	0			ns
PAL_ID duration		$t_{DUR;PAL\_ID}$	9			PXCK periods
Output delay	PXCK to COMPSYNC PXCK to CLAMP	t_{DOS}			25	ns

Note: Timing reference points are at the 50% level. Digital C_{LOAD} <40pF.

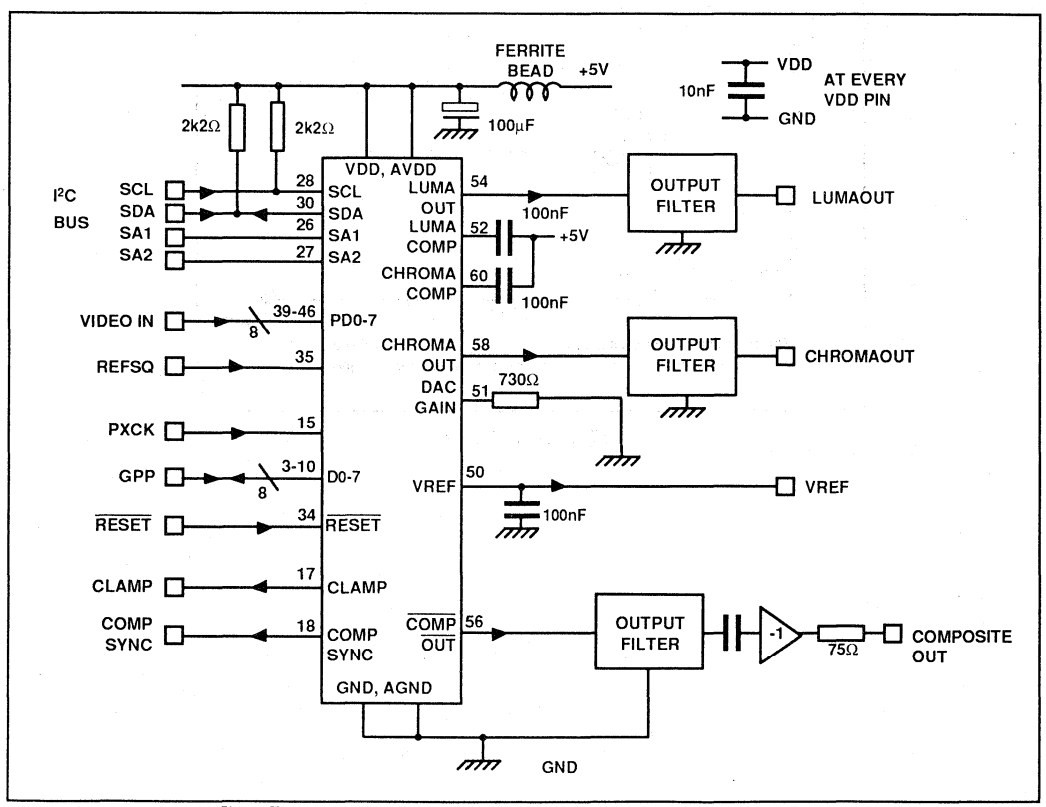


Fig.6 Typical application diagram, SLAVE mode. (Output filter - see Fig.8)

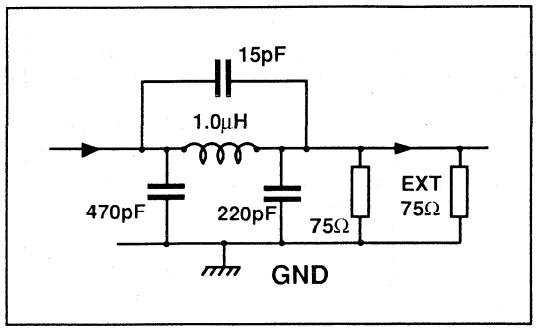


Fig.7 Output reconstruction filter

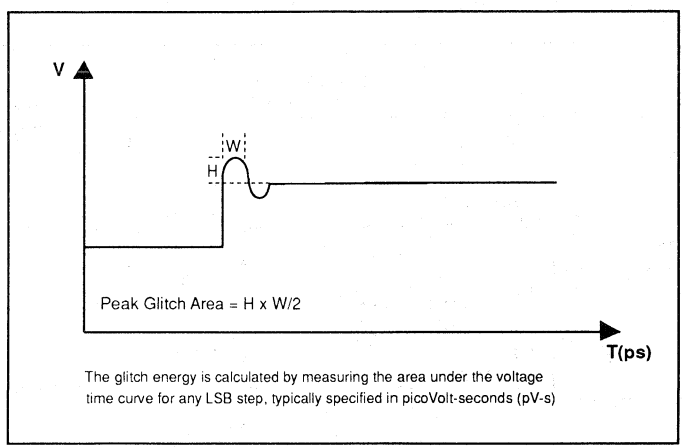


Fig.8 Glitch Energy

VP7615

COLOUR DIGITAL VIDEO CAMERA DECODER IC

The VP7615 iCamHost™ Processor chip can decode the signals from a variety of iVision™ compatible digital video cameras (such as Silicon Vision's iCam™) and process them for use in a host computer system. Digital cameras can offer real cost and performance gains in applications which require a digital video input, and iVision technology realises both these benefits. In a typical analog camera the digitised output from the CCD imager is normally encoded into an analog composite video signal which then has to be re-digitised at the input to the host system. By employing the iVision approach the output from the camera is maintained as a digital signal, but in a format which allows for a low cost 9-wire connection to the host. Eliminating the unnecessary conversion to an analog signal and back again not only saves cost, but also avoids any possible degradation of image quality. Other benefits include direct control of the camera from the host and the ability to power the camera from the host system so saving the cost of a separate power supply.

The VP7615 supports two software selectable CamPort™ interface ports, either of which can receive the digital video from an iVision™ compatible digital video camera. The output is a standard colour digital video signal, similar to standard composite analog-digital decoder chips such as the Philips SAA7110 and SAA7111. All iCamHost™ operating modes are controlled by the host PC via an I²C interface. Hardware I/O controls include output enable and I²C address offset.

NOTE: iCam™, CamPort™ and iCamHost™ are trademarks of Silicon Vision, Inc., Fremont, CA

ORDERING INFORMATION

VP7615 CG FP1N
(Note: Prior to full release to production device may be designated as VP7615 PR FP1N).

FEATURES

- Accommodates different camera configurations based on a variety of CCD imager resolutions
- Requires only a small, low-cost 9 pin mini-DIN to connect to camera
- Receives the image signal from the camera in digital form at a frame rate determined by the host
- Decodes all necessary synchronisation and clock signals from the digital data stream
- Programmable gamma correction curve in RGB colourspace
- Programmable colour-separation matrix
- Collects image status data within user-defined rectangular gated zone of CCD sensor
- Programmable horizontal and vertical aperture correction
- Pin-strap selectable output format in 16 bit YUV 4:2:2 or 8 bit CCIR 656 YUV 4:2:2
- Test pattern generator for SMPTE colourbars
- Bypass mode to output unprocessed 8 bit CCD pixel samples in the luminance channel
- Dual iCamPort™ camera input ports, software selectable
- Completely iVision™ Compatible
- Eight general purpose I/O pins for board level configuration control and/or status
- Programmable polarity for HSYNC, VSYNC, HACT & VACT control outputs
- Chip pinout is backwards compatible with VP7610

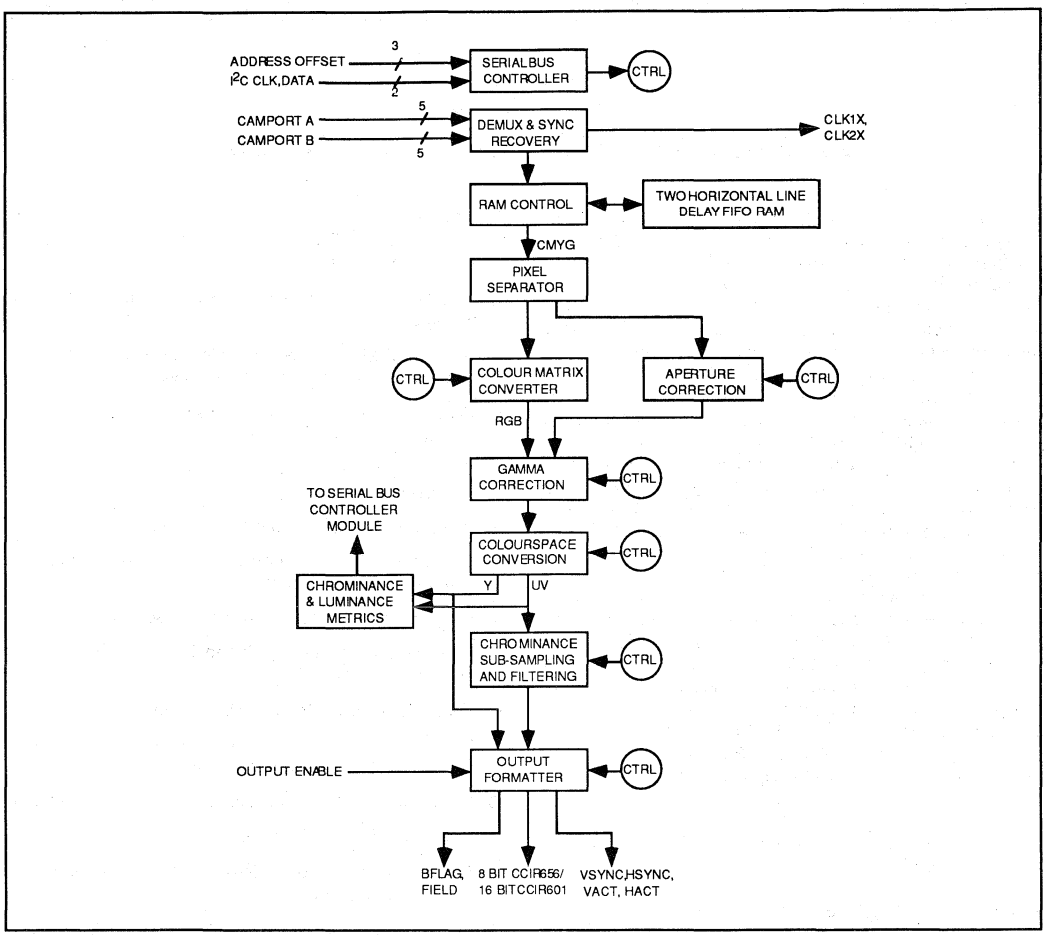


Fig.1 Functional Block Diagram

THEORY OF OPERATION

General Overview
The VP7615 iCamHost™ is a fully synchronous real-time pipeline pixel processor for converting digitized CCD photosite samples into co-sited, colour calibrated, gamma corrected and aperture corrected digital video in an industry-conventional format similar to analog video decoders. The VP7615 supports the full iVision™ Command Set for control of camera head functions such as frame rate, resolution, exposure and colour depth via the CamPort™ Interface. Access to all registers and functions is provided by an I^2C state machine.

Demux and sync recovery
The incoming CCD photosite bytes come in a single nibble at a time in a "bi-endian" fashion from one of two CamPort™s. These nibbles are clocked in via a separate pixel clock signal. The formatting signals such as start of active video, end of active video, and start of new frame are all encoded into the nibble stream. The output is an 8 bit byte of CCD sample for each pixel clock, as well as separate horizontal and vertical sync signals.

RAM control & 2H line delay FIFO RAM
Since the iCamHost™ assumes an interlaced scanning CCD with a CMYG colour mosaic format, the colour content is derived from different locations around where the output video pixel is desired. Specifically, the first line from the CCD contains "red-like" colour content, alternating with the following line containing "blue-like" colour content. The third line is real-time, and the first opportunity to output properly co-sited luminance and chrominance as though the colour pixels were superimposed upon themselves, all on the second line.

Pixel separator
Since the colourspace converter requires the 3 most recent lines of CCD data, this block handles the shuffling of either the 2 red and 1 blue line, or 2 blue and 1 red line of data.

Colour matrix converter
The input to this converter is derived from the relative sums and differences of the above 3 lines of sample data, and processes them through a programmable 3x3 matrix multiplier. The output is colour-separated and calibrated RGB samples.

Gamma corrector
Since CRT monitors have a non-linear RGB intensity response to input signal, gamma correction must be performed in RGB space as well to prevent cross-coupling errors between luminance and chrominance. This block is a programmable 16 line-segment curve generator to provide not only gamma correction, but any arbitrary contiguous curve of positive slope, with end points at any level to adjust contrast and range.

Colourspace converter
Since the output of the processor is to be YUV and not RGB, a fixed-coefficient 3x3 matrix converter is used.

Chrominance sub-sampling & filtering
Spatial sub-sampling and filtering is performed since the output sampling format must be reduced from 4:4:4 to 4:2:2 because most video systems do not require more chrominance data for video camera input.

Output formatter
Devices taking digital video input such as capture, graphics and compression chips usually require the YUV to be formatted either in CCIR601 16 bit mode (YU then YV) or CCIR656 8 bit mode(U then Y then V then Y). The output mode (8 vs 16 bit) CCIR601 is pin-strap selectable. Additional control register bits may be used to swap the luma and chroma data or to swap the order of U and V data to support the video input requirements of a variety of bus master or graphics chip video interfaces without external glue logic. The polarity of VSYNC, HSYNC, VACT and HACT is also programmable. An output enable input signal may be used when "bussing" the output with other video decoders. Other useful signals such as field and colour flags are also provided.

Aperture corrector
Since both the luminance and chrominance are derived from spatially spread pixels and the ideal output would be as though all the pixels were superimposed upon one another, a programmable vertical and horizontal aperture correction can be applied to either "soften" or "sharpen" the image.

Scene-sensing luminance and chrominance metrics
There are no hard-wired closed-loop control circuits in the processor. To achieve great flexibility in control over the behavior of the camera head and processor system, a user-defined region of interest is programmed which provides statistical information about the field of video only within that region. Peak luminance, total luminance, total red chrominance and total blue chrominance are provided and updated after each field.

Serial bus control
To provide read-write control over the registers within the processor, a standard I^2C state-machine is provided. Its address may be offset by 3 bits to preclude address conflicts.

PERFORMANCE

PARAMETER	MAXIMUM VALUE OR SPECIFICATION
CCD Resolution	Up to 768 pixels per line
Field Rate	Up to 60 fields per second
Video Sample Rate	30 MHz. max. input clock rate, 15MHz. max. output clock rate
Video Sample Quantisation	8 bit samples in 2 nibbles of 4 bits each
Control Signals	Standard I²C protocol
Configuration Inputs	I²C address offset, output enable
Gamma Correction	Programmable via 16 arbitrary connected line segments
Output Format	CCIR601 compliant 4:2:2 digital video, pixels per line=CCD pixels
Output Colourspace	YCrCb luminance & chrominance
Output Signals	16 bit digital video, H & V sync, 1X & 2X clock, field ID, chroma ID
Power Consumption	950mW

STATUS REGISTERS

FUNCTION	SIZE	DESCRIPTION
Gated Luminance Sum	32 bits	Sum of luminance values within gated zone
Gated Luminance Peak	8 bits	Value of peak luminance pixel(s) within gated zone
Gate Red Chrominance Sum	32 bits	Sum of red chrominance values within gated zone
Gated Blue Chrominance Sum	32 bits	Sum of blue chrominance values within gated zone

CONTROL REGISTERS

FUNCTION	SIZE	DESCRIPTION
Colour Calibration Matrix	78 bit	9x9 bit signed coefficients converting CMYG to RGB
Gating Zone Start Pixel	16 bits	8 bits for column # and for row #, in 4 pixel increments
Gating Zone End Pixel	16 bits	8 bits for column # and for row #, in 4 pixel increments
Gamma Correction	128 bit	Locus of 16 points of 8 bits each forms many curves
Horiz. Aperture Correction	4 bits	00H = 0%, 40H = +100%, 70H = +175%, F0H= -175%
Vert. Aperture Correction	4 bits	00H = 0%, 40H = + 50%, 70H = + 87%, F0H= - 87%
Processor bypass	2 bits	0=normal, 1=pass raw 8 bit samples to Y output pins
CamPort™ select	1 bit	0=port A, 1=port B
Test pattern generator	1 bits	0=live video, 1=colourbars

SIGNALS & PINOUT

Pin #	I/O	Name	Description
60	In*	CPCKA	Clock - This input receives the clock from the CamPort™ camera on port A.
54	In*	CPDA3	CamPort™ Data Bit 3 - This bus receives the data from the CamPort™ camera on port A.
55	In*	CPDA2	CamPort™ Data Bit 2 - Port A
56	In*	CPDA1	CamPort™ Data Bit 1 - Port A
59	In*	CPDA0	CamPort™ Data Bit 0 - Port A
88	In*	CPCKB	CamPort™ B Clock - This input receives the clock from the CamPort™ camera on port B.
84	In*	CPDB3	CamPort™ B Data Bit 3 - This bus receives the data from the CamPort™ camera on port B.
85	In*	CPDB2	CamPort™ B Data Bit 2
86	In*	CPDB1	CamPort™ B Data Bit 1
87	In*	CPDB0	CamPort™ B Data Bit 0
91	Out	CPSEL	CamPort™ Select Status - When this output is low, the data from CamPort™ A is being used, when this output is high, the data from CamPort™ B is being used. This pin is controlled by Bit 3 of the Configuration Register (sub-address = 0x00).
44	In	RSTN	Reset Not - When this Schmidtt trigger input is low, the chip is placed into a known state. When this input is high, the chip can operate.
11	Out	YY7	Luminance Out bit 7 - When CCSEL is low this bus carries the luminance data. When CCSEL is high this bus carries multiplexed luminance and chrominance data
10	Out	YY6	Luminance Out bit 6
9	Out	YY5	Luminance Out bit 5
6	Out	YY4	Luminance Out bit 4
5	Out	YY3	Luminance Out bit 3
4	Out	YY2	Luminance Out bit 2
3	Out	YY1	Luminance Out bit 1
2	Out	YY0	Luminance Out bit 0
23	Out	UV7	Chrominance Out bit 7 - When CCSEL is low this bus carries the chrominance data. When CCSEL is high this bus carries a constant value of 0x80 (128).
22	Out	UV6	Chrominance Out bit 6
21	Out	UV5	Chrominance Out bit 5
20	Out	UV4	Chrominance Out bit 4
17	Out	UV3	Chrominance Out bit 3
16	Out	UV2	Chrominance Out bit 2
15	Out	UV1	Chrominance Out bit 1
14	Out	UV0	Chrominance Out bit 0
24	Out	CLK2	Clock Out 2X - This clock runs at twice the pixel rate
27	Out	CLK1	Clock Out 1X - This clock runs at the pixel rate.
34	In	OUTEN	Output Enable - When this input is high, the signals YY[7..0], UV[7..0], HSYNC, VSYNC, CLK2, CLK1, HACT, VACT, FIELD and BFLAG are driven. When this input is low, these signals are high-impedance.

* CamPort inputs are TTL levels. All other inputs are CMOS. See Static Electrical Characteristics table.

12	Out	VSYNC	Vertical Sync - This signal goes active for 3 horizontal lines to mark the beginning of each field. In Odd fields, it starts and ends when HSYNC and HACT are low. In Even fields, it starts and ends when HSYNC and HACT are active. This signal's polarity is programmable, but defaults to active low on reset.
13	Out	HSYNC	Horizontal Sync - This signal goes active and returns inactive in the horizontal blanking interval to mark the beginning of each line. This signal's polarity is programmable, but defaults to active low on reset.
28	Out	HACT	Horizontal Active - This signal is active when there is valid video data on the luminance and chrominance busses. Data is valid only when this signal and VACT are active. HACT can be programmed to only go active on active lines (HACT = HACT AND VACT), but defaults at reset to active on all lines. This signal's polarity is also programmable, but defaults to active high on reset.
29	Out	VACT	Vertical Active - This signal is active when there is valid video data on the luminance and chrominance busses. Data is valid only when this signal and HACT are active. VACT can be programmed to only go active on active lines during active pixels (VACT = HACT AND VACT), but defaults at reset to active for entire lines only. This signal's polarity is also programmable, but defaults to active high on reset.
30	Out	FIELD	Field Flag - This signal indicates the field. When it is low, the field is odd. When it is high, the field is even.
31	Out	BFLAG	Blue Flag - This signal indicates when Blue chrominance data is on the chrominance bus.
35	In	CCSEL	CCIR 656 Select - When this input is high, the YY[7..0] bus carries multiplexed luminance and chrominance data in conformance with CCIR 656. When this signal is low, the YY[7..0] bus carries only luminance data.
36	In	RCLK	Register Clock - This input clocks the control circuitry in the chip and must be running in order to access the registers via the I²C bus. The frequency on this input should be between 10 and 20 MHz.
38	In	INVI	Inverter In - This CMOS Schmidt trigger input controls the INVO output. This inverter can be used to form an RC oscillator to drive the input RCLK. It is typically connected through a resistor to INVO and through a capacitor to GND. This oscillator has a period roughly equal to the time constant R*C.
37	Out	INVO	Inverter Out - This signal outputs the opposite level from that applied to INVI. If this inverter is used to form an RC oscillator, this pin would be connected to RCLK.
42	In	OSXI	Oscillator Crystal Input - The crystal oscillator is another way to produce a clock for the input RCLK. A crystal is connected between this input and OSXO.
41	Out	OSXO	Oscillator Crystal Output - A crystal is connected between this output and OSXI.
39	Out	OSCO	Oscillator Output - If the crystal oscillator is used to produce the register clock, this CMOS output drives the RCLK input.
45	In	IAD3	I²C Address Select Bit 3 - The IAD[3..1] inputs select the I²C address that the chip will respond to. The address is 0x60 + 8 * IAD3 + 4 * IAD2 + 2 * IAD1.
43	In	IAD2	I²C Address Select Bit 2
40	In	IAD1	I²C Address Select Bit 1
48	In	SDAI	Serial Data In - This input is connected to the I²C Data line. It may be connected through a filter to reduce noise susceptibility.
47	Out	SDAO	Serial Data Out - This open-drain output connects directly to the I²C Data line.
48	Out	SDMN	Serial Data Monitor - This output is low when the SDAO output is driving low. This output is high when the SDAO output is high impedance.
49	In	SCLI	Serial Clock In - This input is connected to the I²C Clock line. It may be connected through a filter to reduce noise susceptibility.

89	Out	SCLOA	Serial Clock Out Port A - This output drives the level on the SCLI input when the CamPort™ A is selected. When the CamPort™ B is selected this output is driven high. This is not an open-drain output.
90	Out	SCLOB	Serial Clock Out Port B - This output drives the level on the SCLI input when the CamPort™ B is selected. When the CamPort™ A is selected this output is driven high. This is not an open-drain output.
99	Out	GPIO7	General Purpose I/O Bit 7 - This bus represents eight general purpose I/O pins. Each bit may programmed to be an input or an ouput; on reset, all GPIO pins default to high impedance (tri-state) inputs.
98	Out	GPIO6	General Purpose I/O Bit 6
97	Out	GPIO5	General Purpose I/O Bit 5
96	Out	GPIO4	General Purpose I/O Bit 4
95	Out	GPIO3	General Purpose I/O Bit 3
94	Out	GPIO2	General Purpose I/O Bit 2
93	Out	GPIO1	General Purpose I/O Bit 1
92	Out	GPIO0	General Purpose I/O Bit 0
52	In	TST0	Test Pin - This pin should be tied low.
53	In	TST1	Test Pin - This pin should be tied low.
61	In	TST2	Test Pin - This pin should be tied low.
62	In	TST3	Test Pin - This pin should be tied low.
63	In	TST4	Test Pin - This pin should be tied low.
71	In	TSTOE	Test Output Enable - This pin should be tied high.
64, 65, 66, 67, 70, 72, 73, 74, 77, 78, 79, 80, 81,	Out	TOUT	Test Outputs - These pins should be unconnected.
1, 7, 19, 25, 32, 51, 57, 69, 75, 82,	In	GND	Power
8, 18, 26, 33, 50, 58, 68, 76, 83, 100	In	VDD	Power

REGISTER DESCRIPTIONS

The VP7615 iCamHost™ processor station address is strap-configurable to any even location between 0x60 and 0x6E inclusive. Since most iCam cameras currently built use the Station Address 0x68, it is recommended that the iCamHost™ be strapped to a different address. The register addresses shown below are the sub-addresses written to the iCamHost™ immediately after the Station Address. The 7 LSBs of the sub-address must match the specified address. The MSB of the sub-address controls the auto-increment feature of the iCamHost™. If the MSB of the sub-address is a '1', (sub-addresses 0x80 through 0xFF), the sub-address register in the iCamHost™ is incremented to the next address immediately after the data register is read or written. If the MSB of the sub-address is a '0', (sub-addresses 0x00 through 0x7F), the sub-address register in the iCamHost™ remains constant regardless of any reads or writes to the data register. All registers default to 0x00 following chip reset unless otherwise noted.

Address 0x00 Configuration Control Register **Read/Write**

7	6	5	4	3	2	1	0
0	0	0	0	Cfg3	Cfg2	Cfg1	Cfg0

Bits 7 - 4 Always read as '0'

Bit 3 Cfg3 - Camera Input Port Enable
'1' CamPort™ 'B' is source
'0' CamPort™ 'A' is source

Bit 2 Cfg2 - Colour Bar Enable
'1' Colour Bar Test Pattern Output
'0' Normal Video Output

Bit 1 Cfg1 - RGB to YUV Converter Bypass
'1' Green + BnR Pattern Output
'0' Normal YUV Output

Bit 0 Cfg0 - Separator Bypass
'1' Sum = CCD Data, Diff = 0
'0' Normal Separator Output

Address 0x01 RESERVED

Address 0x02 Peak Luma Filter Control Register **Read/Write**

7	6	5	4	3	2	1	0
0	0	0	0	0	PLF2	PLF1	PLF0

Bits 7 - 3 Always read as '0'

Bits 2 - 0 Peak Luma Filter Control
'000' - PLF K = 1, No Luma Filter
'001' - PLF K = 1/2, Fast Luma Filter
'010' - PLF K = 1/4, Med Fast Luma Filter
'011' - PLF K = 1/8, Med Slow Luma Filter
'1XX' - PLF K = 1/16, Slow Luma Filter

Address 0x03 RESERVED

Address 0x04 Horizontal Start Register **Read/Write**

7	6	5	4	3	2	1	0
HStrt7	HStrt6	HStrt5	HStrt4	HStrt3	HStrt2	HStrt1	HStrt0

Bits 7 - 0 Horizontal Start Register
Four times the value of this register is the
Horizontal starting pixel for the Metrics window.

Address 0x05 Horizontal Stop Register **Read/Write**

7	6	5	4	3	2	1	0
HStop7	HStop6	HStop5	HStop4	HStop3	HStop2	HStop1	HStop0

Bits 7 - 0 Horizontal Stop Register
Four times the value of this register is the Horizontal ending pixel for the Metrics window.

Address 0x06 Vertical Start Register **Read/Write**

7	6	5	4	3	2	1	0
VStrt7	VStrt6	VStrt5	VStrt4	VStrt3	VStrt2	VStrt1	VStrt0

Bits 7 - 0 Vertical Start Register
Four times the value of this register is the Vertical starting line (in the frame) for the Metrics window (two times in the field).

Address 0x07 Vertical Stop Register **Read/Write**

7	6	5	4	3	2	1	0
VStop7	VStop6	VStop5	VStop4	VStop3	VStop2	VStop1	VStop0

Bits 7 - 0 Vertical Stop Register
Four times the value of this register is the Vertical ending line (in the frame) for the Metrics window (two times in the field).

Address 0x08 Horizontal Aperture Control Register **Read/Write**

7	6	5	4	3	2	1	0
HApt7	HApt6	HApt5	HApt4	0	0	0	0

Bits 7 Horizontal Aperture Sign Bit
'1' Correction is negative (blurring)
'0' Correction is positive (sharpening)

Bits 6 - 4 Horizontal Aperture Control Value
'000' - No Aperture Correction
|
'111' - Maximum Aperture Correction

Bits 3 - 0 Always read as '0'

Address 0x09 Vertical Aperture Control Register **Read/Write**

7	6	5	4	3	2	1	0
VApt7	VApt6	VApt5	VApt4	0	0	0	0

Bits 7 Vertical Aperture Sign Bit
'1' Correction is negative (blurring)
'0' Correction is positive (sharpening)

Bits 6 - 4 Vertical Aperture Control Value
'000' - No Aperture Correction
|
'111' - Maximum Aperture Correction

Bits 3 - 0 Always read as '0'

Address 0x0A GPIO Output Control Register **Read/Write**

7	6	5	4	3	2	1	0
GPOE7	GPOE6	GPOE5	GPOE4	GPOE3	GPOE2	GPOE1	GPOE0

Bit 7 GPIO7 Output Enable
Bit 6 GPIO6 Output Enable
Bit 5 GPIO5 Output Enable
Bit 4 GPIO4 Output Enable
Bit 3 GPIO3 Output Enable
Bit 2 GPIO2 Output Enable
Bit 1 GPIO1 Output Enable
Bit 0 GPIO0 Output Enable

'0' = Corresponding GPIO pin is tristated/not driven.
'1' = Corresponding GPIO pin is driven to level of corresponding bit in GPIO Output Register.

Address 0x0B GPIO Output Register **Write Only**

7	6	5	4	3	2	1	0
GPO7	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1	GPO0

Bit 7 GPIO7 Output Level
Bit 6 GPIO6 Output Level
Bit 5 GPIO5 Output Level
Bit 4 GPIO4 Output Level
Bit 3 GPIO3 Output Level
Bit 2 GPIO2 Output Level
Bit 1 GPIO1 Output Level
Bit 0 GPIO0 Output Level

'0' = If corresponding GPIO Output Enable bit is '1', then drive the appropriate GPIO pin to '0'
'1' = If corresponding GPIO Output Enable bit is '1', then drive the appropriate GPIO pin to '1'
'X' = If the corresponding GPIO Output Enable bit it '0', then tri-state the appropriate GPIO pin.

Address 0x0B GPIO Input Register **Read Only**

7	6	5	4	3	2	1	0
GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0

Bits 7 - 0 GPIO Input Register
This register represents the level on the corresponding GPIO pins.

Address 0x0C Output Sense Control Register **Read/Write**

7	6	5	4	3	2	1	0
SWPYUV	SWPUV	VAG	HAG	VAS	HAS	VSS	HSS

Bit 7 SWPYUV - YY and UV Swap
- '0' = Normal: YY and UV are in proper positions
  CCIR601 output mode: YY data on YY bus; UV data on UV bus CCIR656 output mode: UYVY
- '1' = Swapped: YY and UV in each other's positions
  CCIR601 output mode: UV data on YY bus; YY data on UV bus CCIR656 output mode: YUYV .

Bit 6 SWPUV - UV Swap
- '0' = Normal: U and V are in position for CCIR601/656: U before V
- '1' = Swapped: U and V are swapped in time: V before U

Bit 5 VAG - VACT Gate
- '1' = Gated: VACT active gated by HACT
- '0' = Normal: VACT active during Active Lines

Bit 4 HAG - HACT Gate
- '1' = Gated: HACT active gated by VACT
- '0' = Normal: HACT active during Active Pixels

Bit 3 VAS - VACT Sense
- '1' = Active High: VACT = 1 during Active Lines
- '0' = Active Low: VACT = 0 during Active Lines

Bit 2 HAS - HACT Sense
- '1' = Active High: HACT = 1 during Active Pixels
- '0' = Active Low: HACT = 0 during Active Pixels

Bit 1 VSS - VSYNC Sense
- '1' = Active High: VSYNC = 1 during Vertical Sync
- '0' = Active Low: VSYNC = 0 during Vertical Sync

Bit 0 HSS - HSYNC Sense
- '1' = Active High: HSYNC = 1 during Horizontal Sync
- '0' = Active Low: HSYNC = 0 during Horizontal Sync

This register defaults on chip reset to 0x0C.

Address 0x0D VACT Control Register **Read/Write**

7	6	5	4	3	2	1	0
VAFIX	0	VFCnt5	VFCnt4	VFCnt3	VFCnt2	VFCnt1	VFCnt0

Bit 7 VAFIX - VACT Control
This bit provides backward compatibility for certain iCam cameras.
- '0' = Disabled: VACT controlled by camera timing
- '1' = Enabled: VACT is inactive during a fixed number of lines during Vertical Blanking. This only effects the end, and not the beginning, of Vertical Blanking.

Bit 6 Always read as '0'

Bits 5 - 0 VFCnt5 - VFCnt0
This field modifies the end of Vertical Blanking if VAFIX is '1' by setting the number of lines that VACT will be inactive during Vertical Blanking.

This register defaults on chip reset to 0x3F.

Address 0x0E Hardware Version Register **Read Only**

7	6	5	4	3	2	1	0
HVer7	HVer6	HVer5	HVer4	HVer3	HVer2	HVer1	HVer0

Bits 7 - 0 Hardware Version Register
0x10 - VP7600
0x11 - VP7610
0x12 - VP7615

Address 0x0F Timing Status Register **Read Only**

7	6	5	4	3	2	1	0
FCnt5	FCnt4	FCnt3	FCnt2	FCnt1	FCnt0	Fld	VBlk

Bits 7 - 2 Field Count
A number between 0 and 63 which increments at the beginning of every Vertical Blanking Interval

Bit 1 Field Bit
'1' Even Field - Digital Field 2
'0' Odd Field - Digital Field 1

Bit 0 Vertical Blanking
'1' Vertical Blanking Interval
'0' Vertical Active Interval

Address 0x10 Lower Byte Red Chroma Register **Read Only**
This register contains Bits 07 - 00 of the Sum of the Red Chrominance of the pixels within the Metrics window.

Address 0x11 Lower Middle Byte Red Chroma Register **Read Only**
This register contains Bits 15 - 08 of the Sum of the Red Chrominance of the pixels within the Metrics window.

Address 0x12 Upper Middle Byte Red Chroma Register **Read Only**
This register contains Bits 23 - 16 of the Sum of the Red Chrominance of the pixels within the Metrics window.

Address 0x13 Upper Byte Red Chroma Register **Read Only**
This register contains Bits 31 - 24 of the Sum of the Red Chrominance of the pixels within the Metrics window.

Address 0x14 Lower Byte Blue Chroma Register **Read Only**
This register contains Bits 07 - 00 of the Sum of the Blue Chrominance of the pixels within the Metrics window.

Address 0x15 Lower Middle Byte Blue Chroma Register **Read Only**
This register contains Bits 15 - 08 of the Sum of the Blue Chrominance of the pixels within the Metrics window.

Address 0x16 Upper Middle Byte Blue Chroma Register **Read Only**
This register contains Bits 23 - 16 of the Sum of the Blue Chrominance of the pixels within the Metrics window.

Address 0x17 Upper Byte Blue Chroma Register **Read Only**
This register contains Bits 31 - 24 of the Sum of the Blue Chrominance of the pixels within the Metrics window.

Address 0x18 Lower Byte Luminance Register **Read Only**
This register contains Bits 07 - 00 of the Sum of the Luminance of the pixels within the Metrics window.

Address 0x19 Lower Middle Byte Luminance Register **Read Only**
This register contains Bits 15 - 08 of the Sum of the Luminance of the pixels within the Metrics window.

Address 0x1A Upper Middle Byte Luminance Register **Read Only**
This register contains Bits 23 - 16 of the Sum of the Luminance of the pixels within the Metrics window.

Address 0x1B Upper Byte Luminance Register **Read Only**
This register contains Bits 31 - 24 of the Sum of the Luminance of the pixels within the Metrics window.

Address 0x1C Peak Luminance Register **Read Only**
This register contains the peak value of the filtered Luminance of the pixels within the Metrics window.

Address 0x20 Sum to Red Coefficient Register **Read/Write**
This register contains the magnitude of the Coefficient which determines the contribution to the Red signal from the Sum signal.

Address 0x21 AmB to Red Coefficient Register **Read/Write**
This register contains the magnitude of the Coefficient which determines the contribution to the Red signal from the AmB signal.

Address 0x22 CmD to Red Coefficient Register **Read/Write**
This register contains the magnitude of the Coefficient which determines the contribution to the Red signal from the CmD signal.

Address 0x23 Red Coefficients Sign Register **Read/Write**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	RCmD	RAmB

Bit 1 Sign for CmD to Red Coefficient
Bit 0 Sign for AmB to Red Coefficient
'1' Coefficient is negative
'0' Coefficient is positive

Address 0x24 Sum to Green Coefficient Register **Read/Write**

This register contains the magnitude of the Coefficient which determines the contribution to the Green signal from the Sum signal.

Address 0x25 AmB to Green Coefficient Register **Read/Write**

This register contains the magnitude of the Coefficient which determines the contribution to the Green signal from the AmB signal.

Address 0x26 CmD to Green Coefficient Register **Read/Write**

This register contains the magnitude of the Coefficient which determines the contribution to the Green signal from the CmD signal.

Address 0x27 Green Coefficients Sign Register **Read/Write**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	GCmD	GAmB

Bit 1 Sign for CmD to Green Coefficient
Bit 0 Sign for AmB to Green Coefficient
'1' Coefficient is negative
'0' Coefficient is positive

Address 0x28 Sum to Blue Coefficient Register **Read/Write**

This register contains the magnitude of the Coefficient which determines the contribution to the Blue signal from the Sum signal.

Address 0x29 AmB to Blue Coefficient Register **Read/Write**

This register contains the magnitude of the Coefficient which determines the contribution to the Blue signal from the AmB signal.

Address 0x2A CmD to Blue Coefficient Register **Read/Write**

This register contains the magnitude of the Coefficient which determines the contribution to the Blue signal from the CmD signal.

Address 0x2B Blue Coefficients Sign Register **Read/Write**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	BCmD	BAmB

Bit 1 Sign for CmD to Blue Coefficient
Bit 0 Sign for AmB to Blue Coefficient
'1' Coefficient is negative
'0' Coefficient is positive

Addresses 0x30 - 0x3F Gamma Values Write Register **Write**

The 16 values that are written to these registers determine the breakpoints in the Gamma correction circuit. The lower four bits of the address are ignored on writes, and the data values are pushed on to an internal shift register. The writes should start with the lowest value and end with the highest value. The last 16 values written generate the Gamma curve, so all 16 values must be written. It is recommended that all 16 writes occur to address 0x30 with auto-increment disabled.

All sixteen Gamma registers default on chip reset to 0x00.

Addresses 0x30 - 0x3F Gamma Values Read Register **Read**

The breakpoints in the Gamma correction circuit are read from these registers.

TIMING REQUIREMENTS

Name	Description	Value		Unit
		Min.	Max.	
fCPX	frequency CPCKA or CPCKB	0	30	MHz
tCPX	period CPCKA or CPCKB	33	-	ns
dcCPX	duty cycle CPCKA or CPCKB	40	60	%
tsuCPDX	setup time, CPDA [3..0] to CPCKA or CPDB [3..0] to CPCKB	8		ns
thCPDX	hold time, CPDA [3..0] to CPCKA or CPDB [3..0] to CPCKB	4		ns
fRCK	frequency RCLK	10	40	MHz
twRSTN	pulse width of RSTN	100		ns

TIMING CHARACTERISTICS

Name	Description	Value		Unit
		Min.	Max.	
tcqRCLK	RCLK to output (CPSEL, SDAO, SDMN)		20	ns
tcpCPX	rising edge of CPCKA or CPCKB to output (YY[7..0], UV[7..0], CLK1, VSYNC, HSYNC,VACT, HACT, BFLAG)		20	ns
tcqCK2f	falling edge of CLK2 to output (YY[7..0], UV[7..0], CLK1, VSYNC, HSYNC, VACT, HACT, BFLAG)	-2	5	ns
tcqCK2r	rising edge of CLK2 to output (YY[7..0], UV[7..0], CLK1,VSYNC, HSYNC, VACT, HACT, BFLAG)	(0.4*tCPX)-2	(0.6*tCPX)+5	ns
tcpCK1f	falling edge of CLK1 to output (YY[7..0], UV[7..0],VSYNC, HSYNC, VACT, HACT, BFLAG)	-3	3	ns
tcqCK1r	rising edge of CLK1 to output (YY[7..0], UV[7..0], VSYNC, HSYNC, VACT, HACT, BFLAG)	tCPX-3	tCPX+3	ns
tpdCK2	propagation delay from CPCKA or CPCKB to CK2		10	ns
tpdINV	propagation delay from INVI to INVO		10	ns
tpdSCL	propagation delay from SCLI to SCLOA or SCLOB		10	ns

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage VDD	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to VDD + 0.5V
Output voltage V_{OUT}	-0.5V to VDD + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HBM)	500V
Storage temperature T_S	-55°C to 150°C
Ambient temperature with power applied T_{AMB}	0°C to 70°C
Junction temperature	125°C
Package power dissipation	1000mW

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation for 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.

STATIC ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise stated)

T_{amb} = 0°C to +70°C V_{DD} = 5.0v ± 5%

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	$0.8V_{DD}$		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage (CMOS input)	V_{IHC}	$0.7V_{DD}$		-	V	
Input low voltage (CMOS input)	V_{ILC}			$0.2V_{DD}$	V	
Input high voltage (TTL input)	V_{IHT}	2.0		-	V	
Input low voltage (TTL input)	V_{ILT}			0.8	V	
Input leakage current	I_{IN}	-1		+1	µA	GND < V_{IN} < V_{DD}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-1		+1	µA	GND < V_{OUT} < V_{DD}
Output S/C current	I_{SC}	10		300	mA	V_{DD} = Max

Section 7

Arithmetic Building Block DSP

GEC PLESSEY
SEMICONDUCTORS

DS3705 - 2.3

PDSP1601/PDSP1601A

ALU AND BARREL SHIFTER

(Supersedes version in December 1993 Digital Video & Video Digital Signal Processing IC Handbook, HB3923-1)

The PDSP1601 is a high performance 16-bit arithmetic logic unit with an independent on-chip 16-bit barrel shifter. The PDSP1601A has two operating modes giving 20MHz or 10MHz register-to-register transfer rates.

The PDSP1601 supports Multicycle multiprecision operation. This allows a single device to operate at 20MHz for 16-bit fields, 10MHz for 32-bit fields and 5MHz for 64-bit fields. The PDSP1601 can also be cascaded to produce wider words at the 20MHz rate using the Carry Out and Carry In pins. The Barrel Shifter is also capable of extension, for example the PDSP1601 can used to select a 16-bit field from a 32-bit input in 100ns.

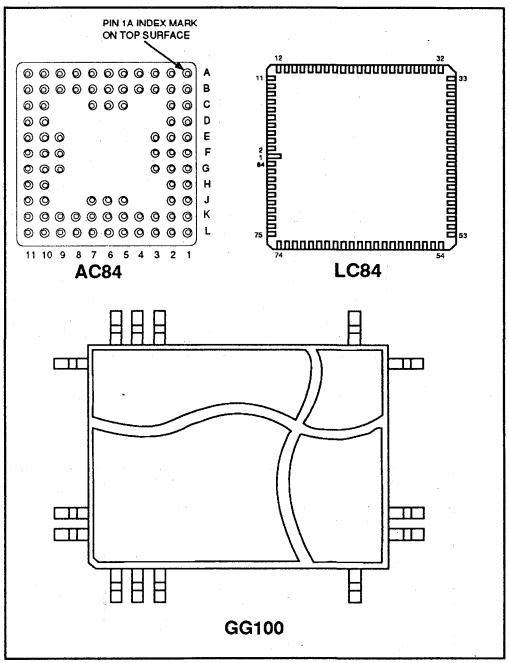


Fig.1 Pin connections - bottom view

FEATURES

- 16-bit, 32 instruction 20MHz ALU
- 16-bit, 20MHz Logical, Arithmetic or Barrel Shifter
- Independent ALU and Shifter Operation
- 4 x 16-bit On Chip Scratchpad Registers
- Multiprecision Operation; e.g. 200ns 64-bit Accumulate
- Three Port Structure with Three Internal Feedback Paths Eliminates I/O Bottlenecks
- Block Floating Point Support
- 300mW Maximum Power Dissipation
- 84-pin Pin Grid Array or 84 Contact LCC Packages or 100 pin Ceramic Quad Flat Pack

APPLICATIONS

- Digital Signal Processing
- Array Processing
- Graphics
- Database Addressing
- High Speed Arithmetic Processors

ASSOCIATED PRODUCTS

PDSP16112 Complex Multiplier
PDSP16116 16 x 16 Complex Multiplier
PDSP16318 Complex Accumulator
PDSP16330 Pythagoras Processor

PIN DESCRIPTION

LC pin	AC pin	Function	LC pin	AC pin	Function	LC pin	AC pin	Function	LC pin	AC pin	Function
1	C6	IA4	22	F3	GND	43	J6	IS0	64	F9	GND
2	A6	MSB	23	G3	MSA0	44	J7	IS1	65	F11	C8
3	A5	MSS	24	G1	MSA1	45	L7	IS2	66	E11	C9
4	B5	B15	25	G2	A15	46	K7	IS3	67	E10	C10
5	C5	B14	26	F1	A14	47	L6	SV0	68	E9	C11
6	A4	B13	27	H1	A13	48	L8	SV1	69	D11	C12
7	B4	B12	28	H2	A12	49	K8	SV2	70	D10	C13
8	A3	B11	29	J1	A11	50	L9	SV3	71	C11	C14
9	A2	B10	30	K1	A10	51	L10	$\overline{\text{SVOE}}$	72	B11	C15
10	B3	B9	31	J2	A9	52	K9	RS0	73	C10	$\overline{\text{OE}}$
11	A1	B8	32	L1	A8	53	L11	RS1	74	A11	BFP
12	B2	B7	33	K2	A7	54	K10	VCC	75	B10	VCC
13	C2	B6	34	K3	A6	55	J10	RS2	76	B9	CO
14	B1	B5	35	L2	A5	56	K11	C0	77	A10	RA0
15	C1	B4	36	L3	A4	57	J11	C1	78	A9	RA1
16	D2	B3	37	K4	A3	58	H10	C2	79	B8	RA2
17	D1	B2	38	L4	A2	59	H11	C3	80	A8	CI
18	E3	B1	39	J5	A1	60	F10	C4	81	B6	IA0
19	E2	B0	40	K5	A0	61	G10	C5	82	B7	IA1
20	E1	$\overline{\text{CEB}}$	41	L5	$\overline{\text{CEA}}$	62	G11	C6	83	A7	IA2
21	F1	CLK	42	K6	MSC	63	G9	C7	84	C7	IA3

GG	SIG	GG	SIG	GG	SIG	GG	SIG
1	N/C	26	N/C	51	N/C	76	N/C
2	N/C	27	N/C	52	N/C	77	N/C
3	N/C	28	N/C	53	N/C	78	N/C
4	N/C	29	N/C	54	N/C	79	N/C
5	VCC	30	B7	55	A7	80	VCC
6	C0	31	B6	56	A6	81	RS2
7	RA0	32	B5	57	A5	82	C0
8	RA1	33	B4	58	A4	83	C1
9	RA2	34	B3	59	A3	84	C2
10	CI	35	B2	60	A2	85	C3
11	IA0	36	B1	61	A1	86	C4
12	IA1	37	B0	62	A0	87	C5
13	IA2	38	CEB	63	CEA	88	C6
14	IA3	39	CLK	64	MSC	89	C7
15	IA4	40	GND	65	IS0	90	GND
16	MSB	41	MSA0	66	IS1	91	C8
17	MSS	42	MSA1	67	IS2	92	C9
18	B15	43	A15	68	IS3	93	C10
19	B14	44	A14	69	SV0	94	C11
20	B13	45	A13	70	SV1	95	C12
21	B12	46	A12	71	SV2	96	C13
22	B11	47	A11	72	SV3	97	C14
23	B10	48	A10	73	SVOE	98	C15
24	B9	49	A9	74	RS0	99	OE
25	B8	50	A8	75	RS1	100	BFP

N/C = not connected - leave open circuit

All GND and VDD pin must be used

PIN DESCRIPTIONS

Symbol	Pin No. (LC84 Package)	Description
MSB	2	**ALU B-input multiplexer select control.**[1] This input is latched internally on the rising edge of CLK.
MSS	3	**Shifter Input multiplexer select control.**[1] This input is latched internally on the rising edge of CLK.
B15 - B0	4 - 19	**B Port data input.** Data presented to this port is latched into the input register on the rising edge of CLK. B15 is the MSB.
$\overline{CEB}$	20	**Clock enable, B Port input register.** When low the clock to this register is enabled.
CLK	21	**Common clock to all internal registered elements.** All registers are loaded, and outputs change on the rising edge of CLK.
MSA0 - MSA1	23 - 24	**ALU A-input multiplexer select control.**[1] These inputs are latched internally on the rising edge of CLK.
A15 - A0	25 - 40	**A Port data input.** Data presented to this port is latched into the input register on the rising edge of CLK. A15 is the MSB.
$\overline{CEA}$	41	**Clock enable, A Port input register.** When low the clock to this register is enabled.
MSC	42	**C-Port multiplexer select control.**[1] This input is latched internally on the rising edge of CLK.
IS0 - IS3	43 - 46	**Instruction inputs to Barrel Shifter, IS3 = MSB.**[1] These inputs are latched internally on the rising edge of CLK.
SV0 - SV3	47 - 50	**Shift Value I/O Port.** This port is used as an input when shift values are supplied from external sources, and as an output when Normalise operations are invoked. The I/O functions are determined by the IS0 - IS3 instruction inputs, and by the $\overline{SVOE}$ control. The shift value is latched internally on the rising edge of CLK.
$\overline{SVOE}$	51	**SV Output enable.** When high the SV port can only operate as an input. When low the SV port can act as an input or as an output, according to the IS0 - IS3 instruction. This pin should be tied hihg or low, depending upon the application.
RS0, RS1 RS2	52 - 53 55	**Instruction inputs to Barrel Shifter registers.**[1] These inputs are latched internally on the rising edge of CLK.
C0 - C15	56 - 63 65 - 72	**C Port data output.** Data output on this port is selected by the C output multiplexer. C15 is the MSB.
$\overline{OE}$	73	**Output enable.** The C Port outputs are in high impedance condition when this control is high.
BFP	74	**Block Floating Point Flag** from ALU, active high.
CO	76	**Carry out** from MSB of ALU.
RA0 - RA2	77 - 79	**Instruction inputs to ALU registers.**[1] These inputs are latched internally on the rising edge of CLK.
CI	80	**Carry in** to LSB of ALU.
IA0 - IA3 IA4	81 - 84 1	**Instruction inputs to ALU.**[1] IA4 = MSB. These inputs are latched internally on the rising edge of CLK.
Vcc	54 & 75	**+5V supply:** Both Vcc pins must be connected.
GND	22 & 64	**0V supply:** Both GND pins must be connected.

NOTES

1. All instructions are executed in the cycle commencing with the rising edge of the CLK which latches the inputs.

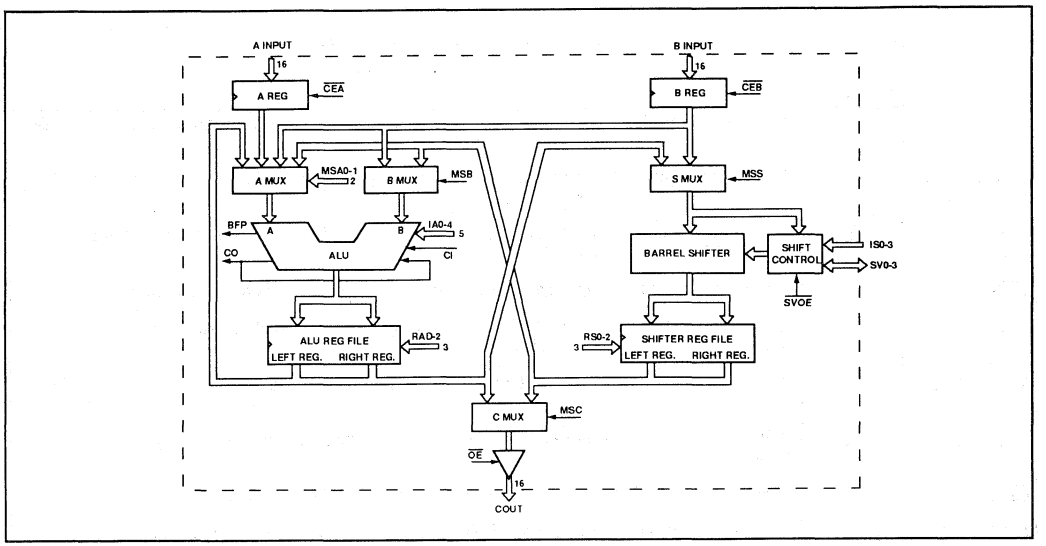


Fig.2 PDSP1601 block diagram

FUNCTIONAL DESCRIPTION

The PDSP1601 contains four main blocks: the ALU, the Barrel Shifter and the two Register Files.

The ALU

The ALU supports 32 instructions as detailed in Table 1.

The inputs to the ALU are selected by the A and B MUXs. Data will fall through from the selected register through the A or B input MUXs and the ALU to the ALU output register file in 50ns for the PDSP1601A (100ns for the PDSP1601).

The ALU instructions are latched, such that the instruction will not start executing until the rising edge of CLK latches the instruction into the device.

The ALU accepts a carry in from the CI input and supplies a carry out to the CO output. Additionally, at the end of each cycle, the carry out from the ALU is loaded into an internal 1 bit register, so that it is available as an input to the ALU on the next cycle. In the manner, multicycle, multiprecision operations are supported. (See MULTICYCLE CASCADE OPERATIONS).

BFP Flag

The ALU has a user programmable BFP flag. This flag may be programmed to become active at any one of four conditions. Two of these conditions are intended to support Block Floating Point operations, in that they provide flags indicating that the ALU result is within a factor of two or four of overflowing the 16 bit number range. For multiprecision operations the flag is only valid whilst the most significant 16 bit byte is being processed. In this manner the BFP flag may be used over any extended word width.

The remaining two conditions detect either an overflow condition or a zero result. For the overflow condition to be active the ALU result must have overflowed into the 16th (sign) bit, (this flag is only valid whilst the most significant 16 bit byte is being processed). The zero condition is active if the result from the ALU is equal to zero. For multiprecision operations the zero flag must be active for all of the 16 bit bytes of an extended word.

The BFP flag is programmed by executing on of the four SBFXX instructions (see Table 1). During the execution of any of these four instructions, the output of the ALU is forced to zero.

Multicycle/Cascade Operation

The ALU arithmetic instructions contain two or three options for each arithemtic operation.

The ALU is designed to operate with two's complement arithmetic, requiring a one to be added to the LSB for all subtract operations. The instructions set includes instructions that will force a one into the LSB, e.g. MIAX1, AMBX1, BMAX1 (see Table 1).

These instructions are used for the least significant 16 bit byte of any subtract operation.

The user has an option of cascading multiple devices, or multicycling a single device to extend the arithmetic precision. Should the user cascade multiple devices, then the cascade arithmetic instructions using the external CI input should be employed for all but the least significant 16 bit byte, e.g. MIACI, APBCI, BMACI (see Table 1).

Should the user multicycle a single device, then the Multicycle Arithmetic instructions, using the internally registered CO bit should be employed for all but the least significant 16 bit byte, e.g. MIACO, APBCO, AMBCO, BMACO (see Table 1).

Table 1 ALU instructions

1a. ARITHMETIC INSTRUCTIONS

Inst	IA4-AI0	Mnemonic	Operation	Function	Mode
00	00000	CLRXX	RESET	CLEAR ALL REGISTERS	--------
01	00001	MIAX1	MINUS A	NA Plus 1	LSBYTE
02	00010	MIACI	MINUS A	NA Plus CI	CASCADE
03	00011	MIACO	MINUS A	NA Plus CO	MULTICYCLE
04	00100	A2SGN	A/2	A/2 Sign Extend	MSBYTE
05	00101	A2RAL	A/2	A/2 with RAL LSB	MULTICYCLE
06	00110	A2RAR	A/2	A/2 with RAR LSB	MULTICYCLE
07	00111	A2RSX	A/2	A/2 with RSX LSB	MULTICYCLE
08	01000	APBCI	A PLUS B	A Plus B Plus CI	CASCADE
09	01001	APBCO	A PLUS B	A Plus B Plus CO	MULTICYCLE
0A	01010	AMBX1	A MINUS B	A Plus NB Plus 1	LSBYTE
0B	01011	AMBCI	A MINUS B	A Plus NB Plus CI	CASCADE
0C	01100	AMBCO	A MINUS B	A Plus NB Plus CO	MULTICYCLE
0D	01101	BMAX1	B MINUS A	NA Plus B Plus 1	LSBYTE
0E	01110	BMACI	B MINUS A	NA Plus B Plus CI	CASCADE
0F	01111	BMACO	B MINUS A	NA Plus B Plus CO	MULTICYCLE

1b. LOGICAL INSTRUCTIONS

Inst	IA4-AI0	Mnemonic	Operation	Function
10	10000	ANXAB	A AND B	A. B
11	10001	ANANB	A AND NB	A. NB
12	10010	ANNAB	NA AND B	NA. B
13	10011	ORXAB	A OR B	A + B
14	10100	ORNAB	NA OR B	NA + B
15	10101	XORAB	A XOR B	A XOR B
16	10110	PASXA	PASS A	A
17	10111	PASNA	INVERT A	NA

1c. CONTROL INSTRUCTIONS

Inst	IA4-AI0	Mnemonic	Operation
18	11000	SBFOV	Set BFP Flag to OVR, Force ALU output to zero
19	11001	SBFU1	Set BFP Flag to UND 1 Force ALU output to zero
1A	11010	SBFU2	Set BFP Flag to UND 2 Force ALU output to zero
1B	11011	SBFZE	Set BFP Flag to ZERO Force ALU output to zero
1C	11100	OPONE	Output 0001 Hex
1D	11101	OPBYT	Output 00FF Hex
1E	11110	OPNIB	Output 000F Hex
1F	11111	OPALT	Output 5555 Hex

KEY

A = A input to ALU
B = B input to ALU
CI = External Carry in to ALU
CO = Internally Registered Carry out from ALU
RAL = ALU Register (Left)
RAR = ALU Register (Right)
RSX = Shifter Register (Left or Right)

MNEMONICS

CLRXX	Clear All Registers to zero		
MIAXX	Minus A,	XX	= Carry in to LSB
A2XXX	A Divided by 2,	XXX	= Source of MSB
APBXX	A Plus B,	XX	= Carry in to LSB
AMBXX	A Minus B,	XX	= Carry in to LSB
BMAXX	B Minus A,	XX	= Carry in to LSB
ANX-Y	AND	X	= Operand 1, Y = Operand 2
ORX-Y	OR	X	= Operand 1, Y = Operand 2
XORXY	Exclusive OR	X	= Operand 1, Y = Operand 2
PASXX	Pass	XX	= Operand
SBFXX	Set BFP Flag	XX	= Function
OPXXX	Output Constant	XXX	

Divide by Two

The ALU has four (A2SGN, A2RAL, A2RAR, A2RSX) instructions used for right shifting (dividing by two) extended precision words. These words, (up to 64 bits) may be stored in the two on-chip register files. When the least significant 16 bit word is shifted, the vacant MSB must be filled with the LSB from the next most significant 16 bit byte. This is achieved via the A2RAL, A2RAR or A2RSX instructions which indicate the source of the new MSB (see ALU INSTRUCTION SET).

When the most significant 16 bit byte is right shifted, the MSB must be filled with a duplicate of the original MSB so as to maintain the correct sign (Sign Extension). This operation is achieved via the A2SGN instruction (see Table 1).

Constants

The ALU has four instructions (OPONE, OPBYT, OPNIB, OPALT) that force a constant value onto the ALU output. These values are primarily intended to be used as masks, or the seeds for mask generation, for example, the OPONE instruction will set a single bit in the least significant position. This bit may be rotated any where in the 16 bit field by the Barrel Shifter, allowing the AND function of the ALU to perform bit-pick operations on input data.

CLR

The ALU instruction CLRXX is used as a Master Reset for the entire device. This instruction has the effect of:

1. Clearing ALU and Barrel Shifter register files to zero.
2. Clearing A and B port input registers to zero.
3. Clearing the R1 and R2 shift control registers to zero.
4. Clearing the internally registered CO bit to zero.
5. Programming the BFP flag to detect *overflow* conditions.

The Barrel Shifter

The Barrel Shifter supports 16 instructions as detailed in Table 2. The input to the Barrel Shifter is selected by the S MUX. Data will fall through from the selected register, through the S MUX and the Barrel Shifter to the shifter output register file in 50ns for the PDSP1601A (100ns for the PDSP1601).

The Barrel Shifter instructions are latched, such that the instructions will not start executing until the rising edge of CLK latches the instruction into the device.

The Barrel Shifter is capable of Logical Arithmetic or Barrel Shifts in either direction.

A. Logical shifts discard bits that exit the 16 bit field and fill spaces with zeros.
B. Arithmetic shifts discard bits that exit the 16 bit field and fill spaces with duplicates of the original MSB.
C. Barrel Shifts rotate the 16 bit fields such that bits tha exit the 16 bit field to the left or right reappear in the vacant spaces on the right or left.

The amount of shift applied is encoded onto the 4 bit Barrel Shifter input as illustrated in Table 3. The type of shift and the amount are determined by the shift control block. The shift control block (see Fig.3) accepts and decodes the four bit ISO-3 instruction. The shift control block contains a priority encoder and two user programmable 4 bit registers R1 and R2.

There are four possible sources of shift value that can be passed onto the Barrel Shifter, there are:

1. The Priority Encoder
2. The SV input
3. The R1 register
4. The R2 register

Inst	IS3-IS0	Mnemonic	Operation	I/O
0	0000	LSRSV	Logical Shift Right by SV	I
1	0001	LSLSV	Logical Shift Left by SV	I
2	0010	BSRSV	Barrel Shift Right by SV	I
3	0011	BSLSV	Barrel Shift Left by SV	I
4	0100	LSRR1	Logical Shift Right by R1	X
5	0101	LSLR1	Logical Shift Left by R1	X
6	0110	LSRR2	Logical Shift Right by R2	X
7	0111	LSLR2	Logical Shift Left by R2	X
8	1000	LR1SV	Load Register 1 From SV	I
9	1001	LR2SV	Load Register 2 From SV	I
A	1010	ASRSV	Arithmetic Shift Right by SV	I
B	1011	ASRR1	Arithmetic Shift Right by R1	X
C	1100	ASRR2	Arithmetic Shift Right by R2	X
D	1101	NRMXX	Normalise Output PE	O
E	1110	NRMR1	Normalise Output PE, Load R1	O
F	1111	NRMR2	Normalise Output PE, Load R2	O

Table 2 Barrel shifter instructions

KEY

SV = Shift Value
R1 = Register 1
R2 = Register 2
PE = Priority Encoder Output
I => SV Port operates as an Input
O => SV Port operates as an Output
X => SV Port in a High Impedance State

MNEMONICS

LSXYY Logical Shift, X = Direction YY = Source of Shift Value
BSXYY Barrel Shift, X = Direction YY = Source of Shift Value
ASXYY Arithmetic Shift, X = Direction YY = Source of Shift Value
LXXYY Load XX = Target YY = Source
NRMYY Normalise by PE, Output PE value on SV Port, Load YY Reg

6

SV3	SV2	SV1	SV0	Shift
0	0	0	0	No shift
0	0	0	1	1 place
0	0	1	0	2 places
0	0	1	1	3 places
0	1	0	0	4 places
0	1	0	1	5 places
0	1	1	0	6 places
0	1	1	1	7 places
1	0	0	0	8 places
1	0	0	1	9 places
1	0	1	0	10 places
1	0	1	1	11 places
1	1	0	0	12 places
1	1	0	1	13 places
1	1	1	0	14 places
1	1	1	1	15 places

Table 3 Barrel shifter codes

Priority Encoder

If the priority encoder is selected as the source of the shift value (instructions:- NRMXX, NRMR1, MRMRZ), then within one 100ns cycle or two 50ns cycles for the PDSP1601A (one 200ns or two 100ns cycles for the PDSP1601), the shift circuitry will:

(1) Priority encode the 16 bit input to the Barrel Shifter and place the 4 bit value in either of the R1 or R2 registers and output the value on the SV port (if enabled by $\overline{\text{SVOE}}$).

(2) Shift the 16 bit input by the amount indicated by the Priority Encoder such that the output from the Barrel Shifter is a normalised value.

SV Input

If the SV port is selected as the source of the shift value, then the input to the Barrel Shifter is shifted by the value stored in the internal SV register.

$\overline{\text{SVOE}}$

The SV port acts as an input or an output depending upon the IS0-3 instruction. If the user does not wish to use the normalise instructions, then the SV port mat be forced to be input only by typing $\overline{\text{SVOE}}$ control high. In this mode the SV port may be considered an extension of the instruction inputs.

R1 and R2 Registers

The R1 and R2 registers may be loaded from the Priority Encoder (NRMR1 and NRMR2) or from the SV input (LR1SV, LR2SV).

Whilst the latter two instructions are executing, the Barrel Shifter will pass its input to the output unshifted.

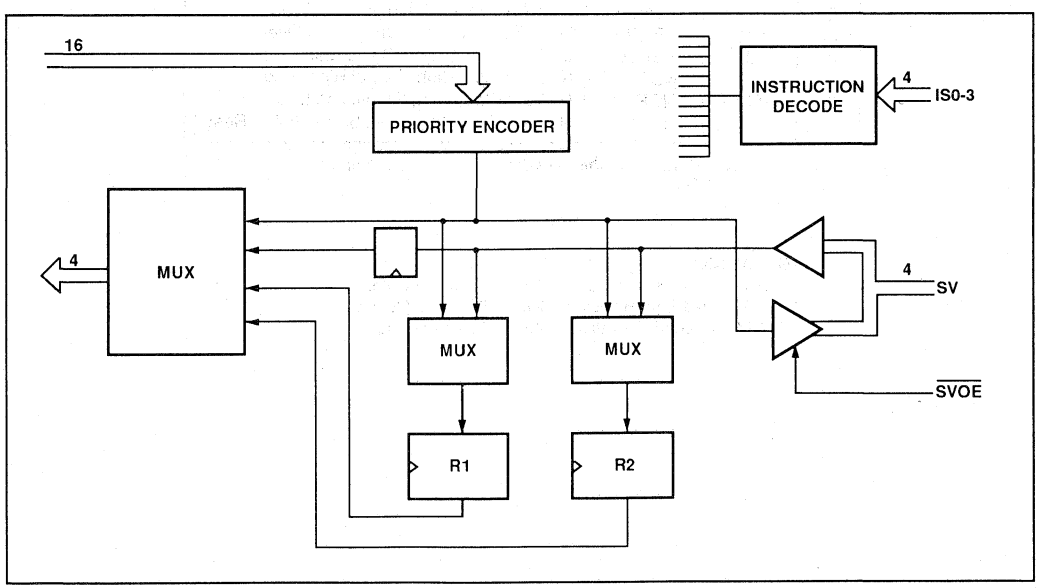


Fig.3 Shift control block

The Register Files

There are two on-chip register files (ALU and Shifter), each containing two 16 bit registers and each supporting 8 instructions (see Table 4). The instructions for the ALU register file and the Barrel Shifter Register file are the same.

The Inputs to the register files come from either the ALU or the Barrel Shifter, and are loaded into the Register files on the rising edge of CLK.

The register file instructions are latched such that the instruction will not start executing until the rising edge of the CLK latches the instruction into the device.

The register file instructions (see Table 4) allow input data to be loaded into either, neither or both of the registers. Data is loaded at the end of the cycle in which the instruction is executing.

The register file instructions allow the output to be sourced from either of the two registers, the selected output will be valid during the cycle in which the instruction is executing.

ALU REGISTER INSTRUCTIONS			
Inst	**RA2-RA0**	**Mnemonic**	**Operation**
0	000	LLRRR	Load Left Reg Output Right Reg
1	001	LRRLR	Load Right Reg Output Left Reg
2	010	LLRLR	Load Left Register, Output Left Reg
3	011	LRRRR	Load Right Register, Output Right Reg
4	100	LBRLR	Load Both Registers, Output Left Reg
5	101	NOPRR	No Load Operation, Output Right Reg
6	110	NOPLR	No Load Operation, Output Left Reg
7	111	NOPPS	No Load Operation, Pass ALU Result
SHIFTER REGISTER INSTRUCTIONS			
Inst	**RA2-RA0**	**Mnemonic**	**Operation**
0	000	LLRRR	Load Left Reg Output Right Reg
1	001	LRRLR	Load Right Reg Output Left Reg
2	010	LLRLR	Load Left Register, Output Left Reg
3	011	LRRRR	Load Right Register, Output Right Reg
4	100	LBRLR	Load Both Registers, Output Left Reg
5	101	NOPRR	No Load Operation, Output Right Reg
6	110	NOPLR	No Load Operation, Output Left Reg
7	111	NOPPS	No Load Operation, Pass Barrel Shifter Result

Table 4 ALU and shift register instructions mnemonics

MNEMONICS

LXXYY Load XX = Target, YY = Source of Output
LBOXX Load Both Registers, XX = Source of Output
NOPXX No Load Operation, XX = Source of Output

Multiplexers

There are four user selectable on-chip multiplexers (A-MUX, B-MUX, S-MUX and C-MUX).

These four multiplexers support instructions as tabulated in Table 5.

The MUX instructions are latched such that the instruction will not start executing until the rising edge of CLK latches the instruction onto the device.

		MSA1	MSA0	Output
A-MUX	MARAX	0	0	ALU REGISTER FILE OUPUT
	MAAPR	0	1	A-PORT INPUT
	MABPR	1	0	B-PORT INPUT
	MARSX	1	1	SHIFTER REGISTER FILE OUTPUT

	MSB	Output
B-MUX	0	B-PORT INPUT
	1	SHIFTER REGISTER FILE OUTPUT

	MSS	Output
S-MUX	0	B-PORT INPUT
	1	SHIFTER REGISTER FILE OUTPUT

	MSC	Output
C-MUX	0	ALU REGISTER FILE OUTPUT
	1	SHIFTER REGISTER FILE OUTPUT

Table 5

INSTRUCTION SET

ALU Arithmetic Instructions

Mnemonic	Op Code	Function
CLRXX	<00>	On the rising edge of CLK at the end of the cycle in which this instruction is executing, the A Port, B Port, ALU, Barrel Shifter, and Shift Control Registers will be loaded with zeros. The internal registered CO will also be set to zero, and the BFP flag will be set to activate on overflow conditions.
MIAX1	<01>	The A input to the ALU is inverted and a one is added to the LSB.
MIAC1	<02>	The A input to the ALU is inverted and the CI input is added to the LSB.
MIACO	<03>	The A input to the ALU is inverted and the CO output from the ALU on the previous cycle is added to the LSB.
A2SGN	<04>	The A input to the ALU is right shifted one bit position. The LSB is discarded, and the vacant MSB is filled by duplicating the original MSB (Sign Extension).
A2RAL	<05>	The A input to the ALU is right shifted one bit position. The LSB is discarded, and the vacant MSB is filled with the LSB from the ALU register.
A2RAR	<06>	The A input to the ALU is right shifted one bit position. The LSB is discarded, and the vacant MSB is filled with the LSB from the ALU register.
A2RSX	<07>	The A input to the ALU is right shifted one bit position. The LSB is discarded, and the vacant MSB is filled with the LSB from the B input to the ALU.
APBCI	<08>	The A input to the ALU is added to the B input, and the CI input is added to the LSB.
APBCO	<09>	The A input to the ALU is added to the B input, and the CO out from the ALU on the previous cycle is added to the LSB.
AMBX1	<0A>	The A input to the ALU is added to the inverted B input, and a one is added to the LSB.
AMBCI	<0B>	The A input to the ALU is added to the inverted B input, and the CI input is added to the LSB.
AMBCO	<0C>	The A input to the ALU is added to the inverted B input, and the CO out from the ALU on the previous cycle is added to the LSB.
BMAX1	<0D>	The inverted A input to the ALU is added to the B input, and a one is added to the LSB.
BMAC1	<0E>	The inverted A input to the ALU is added to the B input, and the CI input is added to the LSB.
BMACO	<0F>	The inverted A input to the ALU is added to the B input, and the CO out from the ALU on the previous cycle is added to the LSB.

ALU Logical Instructions

Mnemonic	Op Code	Function
ANXAB	<10>	The A input to the ALU is logically 'ANDed' with the B input.
ANANB	<11>	The A input to the ALU is logically 'ANDed' with the inverse of the B input.
ANNAB	<12>	The inverse of the A input to the ALU is logically 'ANDed' with the B input.
ORXAB	<13>	The A input to the ALU is logically 'ORed' with the B input.
ORNAB	<14>	The inverse A input to the ALU is logically 'ORed' with the B input.
XORAB	<15>	The A input to the ALU is logically Exclusive-ORed with the B input.
PASXA	<16>	The A input to the ALU is passed to the output.
PASNA	<17>	The inverse of the A input to the ALU is passed to the output.

ALU Control Instructions

Mnemonic	Op Code	Function
SBFOV	<18>	The BFP flag is programmed to activate when an ALU operation causes an overflow of the 16 bit number range. This flag is logically the exclusive-or of the carry into and out of the MSB of the ALU. For the most significant Byte this flag indicates that the result of an arithmetic two's complement operation has overflowed into the sign bit. The output of the ALU is forced to zero for the duration of this instruction.
SBFU1	<19>	The BFP flag is programmed to activate when an ALU operation comes within a factor of two of causing an overflow of the 16 bit number range. For the most significant Byte this flag indicates that the result of an arithmetic two's complement operation is within a factor of two of overflowing into the sign bit. The output of the ALU is forced to zero for the duration of this instruction.
SBFU2	<1A>	The BFP flag is programmed to activate when an ALU operation comes within a factor of four of causing an overflow of the 16 bit number range. For the most significant Byte this flag indicates that the result of an arithmetic two's complement operation is within a factor of four of overflowing into the sign bit. The output of the ALU is forced to zero for the duration of this instruction.
SBFZE	<1B>	The BFP flag is programmed to activate when an ALU operation causes a result of zero. The output of the ALU is forced to zero for the duration of this instruction. During the execution of this instruction the BFP flag will become active.
OPONE	<1C>	The ALU will output the binary value 0000000000000001, the MSB on the left.
OPBYT	<1D>	The ALU will output the binary value 0000000011111111, the MSB on the left.
OPNIB	<1E>	The ALU will output the binary value 0000000000001111, the MSB on the left.
OPALT	<1F>	The ALU will output the binary value 0101010101010101, the MSB on the left.

Barrel Shifter Instructions

Mnemonic	Op Code	Function
LSRSV	<0>	The 16 bit input to the Barrel Shifter is right shifted by the number of places indicated by the magnitude of the four bit number present in the SV register. The LSBs are dicarded, and the vacant MSBs are filled with zeros.
LSLSV	<1>	The 16 bit input to the Barrel Shifter is left shifted by the number of places indicated by the magnitude of the four bit number present in the SV register. The LSBs are dicarded, and the vacant MSBs are filled with zeros.
BSRSV	<2>	The 16 bit input to the Barrel Shifter is rotated to the right by the number of places indicated by the magnitude of the four bit number present in the SV register. The LSBs that exit the 16 bit field to the right, reappear in the vacant MSBs on the left.
BSLSV	<3>	The 16 bit input to the Barrel Shifter is rotated to the left by the number of places indicated by the magnitude of the four bit number present in the SV register. The LSBs that exit the 16 bit field to the right, reappear in the vacant MSBs on the right.
LSRR1	<4>	The 16 bit input to the Barrel Shifter is right shifted by the number of places indicated by the magnitude of the four bit number resident within the R1 register. The LSBs are discarded, and the vacant MSBs are filled with zeros.
LSLR1	<5>	The 16 bit input to the Barrel Shifter is left shifted by the number of places indicated by the magnitude of the four bit number resident within the R1 register. The LSBs are discarded, and the vacant LSBs are filled with zeros.
LSRR2	<6>	The 16 bit input to the Barrel Shifter is right shifted by the number of places indicated by the magnitude of the four bit number resident within the R2 register. The LSBs are discarded, and the vacant MSBs are filled with zeros.
LSLR2	<7>	The 16 bit input to the Barrel Shifter is left shifted by the number of places indicated by the magnitude of the four bit number resident within the R2 register. The LSBs are discarded, and the vacant LSBs are filled with zeros.

Mnemonic	Op Code	Function
LR1SV	<8>	On the rising edge of CLK at the end of the cycle in which this instruction is executing, the R1 register will be loaded with the data present on the SV port. The input to the Barrel Shifter will be passed onto the output unshifted.
LR2SV	<9>	On the rising edge of CLK at the end of the cycle in which this instruction is executing, the R2 register will be loaded with the data present on the SV port. The input to the Barrel Shifter will be passed onto the output unshifted.
ASRSV	<A>	The 16 bit input to the Barrel Shifter is right shifted by the number of places indicated by the magnitude of the four bit number present in the SV register. The LSBs are discarded, and the vacant MSBs are filled with duplicates of the original MSB. (Sign Extension).
ASRR1	<B>	The 16 bit input to the Barrel Shifter is right shifted by the number of places indicated by the magnitude of the four bit number resident within the R1 register. The LSBs are discarded, and the vacant MSBs are filled with duplicates of the original MSB. (Sign Extension).
ASRR2	<C>	The 16 bit input to the Barrel Shifter is right shifted by the number of places indicated by the magnitude of the four bit number resident within the R2 register. The LSBs are discarded, and the vacant MSBs are filled with duplicates of the original MSB. (Sign Extension).
NRMXX	<D>	The 16 bit input to the Barrel Shifter is left shifted by the number of places indicated by the magnitude of the four bit number output from the Priority Encoder. This value is also output on the SV port (provided $\overline{SVOE}$ is low). The effect of this operation is to left shift the input by the necessary amount (max 15 places) to result in the MSB and the next most significant bit being different. This has the effect of eliminating unnecessary Sign Bits, and hence Normalising the input data. The MSBs shifted out to the left are discarded, and the vacant LSBs on the right are filled with zeros.
NRMR1	<E>	The 16 bit input to the Barrel Shifter is left shifted by the number of places indicated by the magnitude of the four bit number output from the Priority Encoder. This value is also loaded into the R1 register at the end of the cycle, and is output on the SV port (provided $\overline{SVOE}$ is low). The effect of this operation is to left shift the input by the necessary amount (max 15 places) to result in the MSB and the next most significant bit being different. This has the effect of eliminating unnecessary Sign Bits, and hence Normalising the input data. The MSBs shifted out to the left are discarded, and the vacant LSBs on the right are filled with zeros.
NRMR2	<F>	The 16 bit input to the Barrel Shifter is left shifted by the number of places indicated by the magnitude of the four bit number output from the Priority Encoder. This value is also loaded into the R2 register at the end of the cycle, and is output on the SV port (provided $\overline{SVOE}$ is low). The effect of this operation is to left shift the input by the necessary amount (max 15 places) to result in the MSB and the next most significant bit being different. This has the effect of eliminating unnecessary Sign Bits, and hence Normalising the input data. The MSBs shifted out to the left are discarded, and the vacant LSBs on the right are filled with zeros.

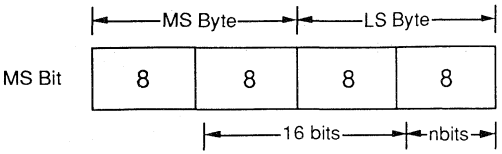
Barrel Shifter or ALU Register Instructions

Mnemonic	Op Code	Function
LLRRR	<0>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the contents of the Right register will appear on the output. On the rising edge of CLK at the end of the cycle, and the data on the register inputs will be loaded into the Left Register.
LRRLR	<1>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the contents of the Left register will appear on the output. On the rising edge of CLK at the end of the cycle, the data on the register inputs will be loaded into the Right Register.
LLRLR	<2>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the contents of the Left register will appear on the output. On the rising edge of CLK at the end of the cycle, the data on the register inputs will be loaded into the Left Register.
LRRRR	<3>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the contents of the Right register will appear on the output. On the rising edge of CLK at the end of the cycle, the data on the register inputs will be loaded into the Right Register.
LBRLR	<4>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the contents of the Left register will appear on the output. On the rising edge of CLK at the end of the cycle, and the data on the register inputs will be loaded into both Left and Right Register.
NOPRR	<5>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the contents of the Right register will appear on the output. On the rising edge of CLK at the end of the cycle no load operation will occur, the register contents will remain unchanged.
NOPLR	<6>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the contents of the Left register will appear on the output. On the rising edge of CLK at the end of the cycle no load operation will occur, the register contents will remain unchanged.
NOPPS	<7>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the input to the registers will appear on the output. On the rising edge of CLK at the end of the cycle no load operation will occur, the register contents will remain unchanged.

TYPICAL APPLICATION

Select a 16 bit field from each word in a block of 32 bit words with a 10MHz throughput.

The 16 bit field indicated is to be selected from each 32 bit word.



The 32 bit words are fed into the B port of the PDSP1601 in two cycles, MS byte first.

The PDSP1601 shift control is initiated by programming the R1 and R2 registers with n and 16-n respectively.

The shift operation is implemented in three steps:-

(1) The MS byte is logically left shifted (16-n) places, the MSBs being discarded and the LSB spaces being filled with zeros. This shifted data is loaded into the shifter register file left register.

(2) The LS byte is logically right shifted, n-places, the LSBs being discarded and the MSBs being filled with zeros. This shifted data is loaded into the shifter register file left register.

During this cycle the previous contents of this register are passed through the ALU to the ALU register file left register.

(3) While the MS byte of the next 32 bit word is shifted in the Barrel Shifter, the two previous results, resident within the left registers of the ALU and Shifter Register files are 'ORed' by the ALU, the result being the desired 16 bit field is loaded into the ALU register file right register ready to be output on the next cycle.

The instructions from initialisation are given in Table 6.

CLK	CEB	MSA	MSB	MSS	MSC	IA	IS	SV	RA	RS	Comment
1/	1	MARSX	1	0	0	CLRXX	X	X	NOPLR	NOPLR	Clear
2/	1	MARSX	1	0	0	PASXA	LR1SV	n	NOPLR	NOPLR	Load R1 with n
3/	0	MARSX	1	0	0	PASXA	LR2SV	(16-n)	NOPLR	NOPLR	Load R2 with (16-n)
4/	0	MARSX	1	0	0	PASXA	LSLR2	X	NOPLR	LLRLR	Shift 1st MS byte
5/	0	MARSX	1	0	0	PASXA	LSRR1	X	LLRRR	LLRLR	Shift 1st LS byte
6/	0	MARAX	1	0	0	ORXAB	LSLR2	X	LRRLR	LLRLR	OR 1st bytes and shift 2nd MS byte
7/	0	MARSX	1	0	0	PASXA	LSRR1	X	LLRRR	LLRLR	Shift 2nd LS byte and output first result
8/	0	MARAX	1	0	0	ORXAB	LSLR2	X	LRRLR	LLRLR	Shift 3rd LS byte

Repeat instruction pair 5/ and 6/ until all 16 bit fields have been selected.

Table 6

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage Vcc	-0.5V to 7.0V
Input voltage V_{IN}	-0.9 to Vcc + 0.9V
Output voltage V_{OUT}	-0.9 to Vcc + 0.9V
Clamp diode current per pin Ik (see note 2)	±18mA
Static discharge voltage (HMB)	500V
Storage temperature T_S	-65°C to +150°C
Ambient temperature with power applied T_{amb}	
Military	-40°C to +125°C
Industrial	-40°C to +85°C
Package power dissipation PTOT	
AC	1000mw
LC	1000mw

NOTES

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.

THERMAL CHARACTERISTICS

Package type	Θ_{JC} °C/W	Θ_{JA} °C/W
AC	12	36
LC	12	35

ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise stated)

T_{AMB} (Commercial) = 0°C to +70°C, V_{CC} = 5.0V±5%, Ground = 0V
T_{AMB} (Industrial) = -40°C to +85°C, V_{CC} = 5.0V±10%, Ground = 0V
T_{AMB} (Military) = -55°C to +125°C, V_{CC} = 5.0V±10%, Ground = 0V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4			V	I_{OH} = 8mA
Output low voltage	V_{OL}			0.4	V	I_{OL} = -8mA
Input high voltage	V_{IH}	3.5			V	
Input low voltage	V_{IL}			0.5	V	
Input leakage current	I_{IL}	-10		+10	µA	GND < V_{IN} < V_{CC}
Vcc current	I_{CC}			60	mA	T_{amb} = -40°C to +85°C
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{CC}
Output S/C current	I_{SC}	12		80	mA	V_{CC} = Max
Input capacitance	C_{IN}		5		pF	

Switching Characteristics

Characteristic	Value				Units	Conditions
	PDSP1601		PDSP1601/A			
	Min.	Max.	Min.	Max.		
CLK rising edge to C-PORT	5	40	5	25	ns	2 x LSTTL + 20pF
CLK rising edge to CO	5	100	5	50	ns	1 x LSTTL + 5pF
CLK rising edge to BFP	5	100	5	50	ns	1 x LSTTL + 5pF
Setup $\overline{CEA}$ or $\overline{CEB}$ to CLK rising edge	30		15		ns	
Hold $\overline{CEA}$ or $\overline{CEB}$ after CLK rising edge		0		0	ns	
Setup A or B port inputs to CLK rising edge	40		20		ns	
Hold A or B port inputs after CLK rising edge		0		0	ns	
Setup MSA0-1, MSB, MSS, MSC, RA2-0, RS0-2, IA0-4, IS0-3, to CLK rising edge	40		20		ns	
Hold RS0-2, IA0-4 after CLK rising edge		0		0	ns	
Hold IS0-3 after CLK rising edge		3		3	ns	
Hold MSA0-1, MSB, MSS, MSC, RA0-2 after CLK rising edge		0		0	ns	
Setup SV to CLK rising edge	40		20		ns	Input mode
Hold SV after CLK rising edge		3		3	ns	Input mode
CLK rising edge to SV	5	100	5	50	ns	20pF load, SV O P mode
$\overline{OE}$ ⎍⎾C-PORT⏌⎿ Z		40		25	ns	2 x LSTTL + 20pF
$\overline{OE}$ ⎍⎾C-PORT⎍⎾ Z		40		25	ns	2 x LSTTL + 20pF
$\overline{OE}$ ⏌⎿C-PORT Z⎍⎾		40		25	ns	2 x LSTTL + 20pF
$\overline{OE}$ ⏌⎿C-PORT Z⏌⎿		40		25	ns	2 x LSTTL + 20pF
Clock period (ALU & Barrel Shifter, serial mode)	200		100		ns	
Clock period (ALU & Barrel Shifter, parallel mode)	100		50		ns	
Clock high time	40		20		ns	
Clock low time	40		20		ns	

NOTES
1. LSTTL is equivalent to I_{OH} at 20µA I_{OL} of -0.4mA
2. Current is defined as negative into the device.

ORDERING INFORMATION

PDSP1601 AO AC	10MHz Military - PGA package
PDSP1601 MC GGCR	10MHz MIL883 Screened - QFP package
PDSP1601A BO AC	20MHz Industrial - PGA package

GEC PLESSEY
SEMICONDUCTORS

DS3706 - 2.3

PDSP16112/PDSP16112A

16 x 12 BIT COMPLEX MULTIPLIER

(Supersedes version in December 1993 Digital Video & Video Digital Signal Processing IC Handbook, HB3923-1)

The PDSP16112/PDSP16112A will multiply a complex (16 + 16) bit word by a complex (12 + 12) bit coefficient word and produce a complex (17 + 17) bit rounded product. The input data format is two's complement. The device consists of four 16 x 12 multiplier sections based on Booth's '2 bits at a time' algorithm and is pipelined to achieve a 20MHz (PDSP16112A) or 10MHz (PDSP16112) throughput.

FEATURES

- 20MHz Complex Number (16 + 16) x (12 + 12) Multiplication
- Pipeline Architecture
- Power Dissipation only 500mW
- TTL Compatible Inputs
- 120 pin PGA or QFP packages

APPLICATIONS

- Digital Filtering
- Fast Fourier Transforms
- Radar and Sonar Processing
- Instrumentation
- Automation
- Image Processing

ASSOCIATED PRODUCTS

PDSP1601 Arithmetic Logic Unit
PDSP16318 40MHz Address Generator
PDSP16330 Pythagoras Processor

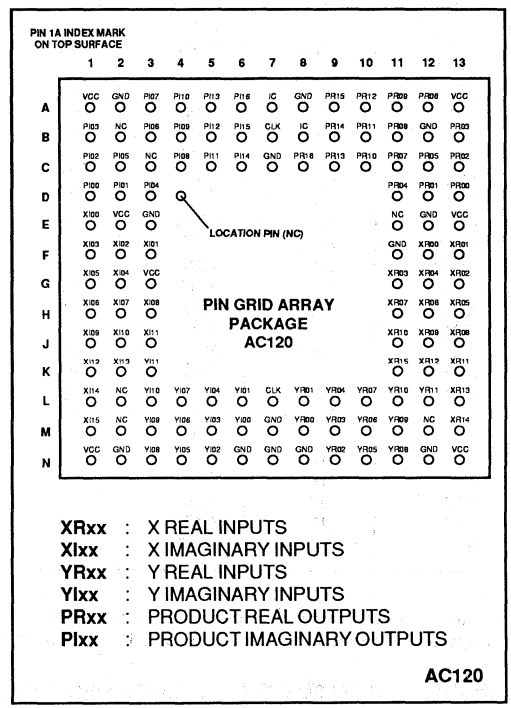


Fig.1 Pin connections - top view (AC120 - PGA)

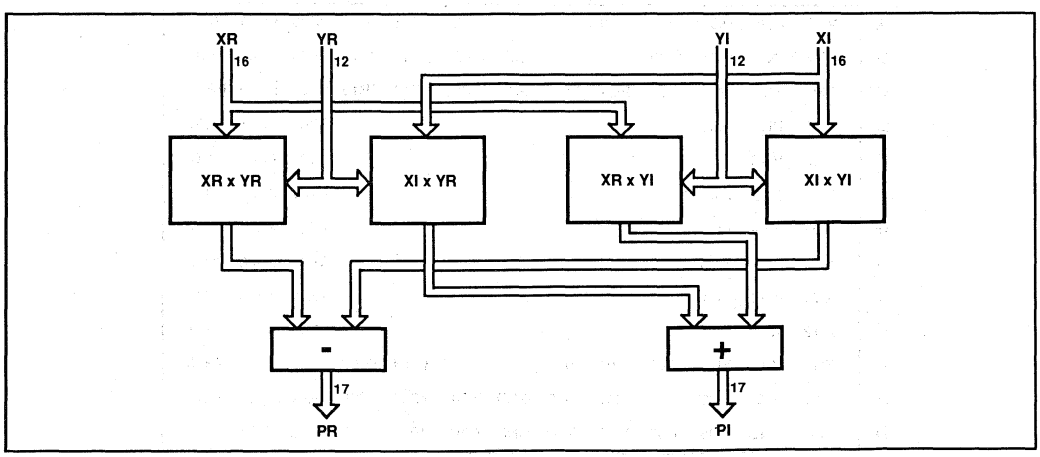


Fig. 2 Multiplier block diagram

PIN OUT - FUNCTION TO PIN (PGA Package - AC120)

Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.
PR00	D13	PR09	A11	PI00	D1	PI09	B4
PR01	D12	PR10	C10	PI01	D2	PI10	A4
PR02	C13	PR11	B10	PI02	C1	PI11	C5
PR03	B13	PR12	A10	PI03	B1	PI12	B5
PR04	D11	PR13	C9	PI04	D3	PI13	A5
PR05	C12	PR14	B9	PI05	C2	PI14	C6
PR06	A12	PR15	A9	PI06	B3	PI15	B6
PR07	C11	PR16	C8	PI07	A3	PI16	A6
PR08	B11	CLK	L7	PI08	C4	CLK	B7
XR00	F12	XI00	E1	YR00	M8	YI00	M6
XR01	F13	XI01	F3	YR01	L8	YI01	L6
XR02	G13	XI02	F2	YR02	N9	YI02	N5
XR03	G11	XI03	F1	YR03	M9	YI03	M5
XR04	G12	XI04	G2	YR04	L9	YI04	L5
XR05	H13	XI05	G1	YR05	N10	YI05	N4
XR06	H12	XI06	H1	YR06	M10	YI06	M4
XR07	H11	XI07	H2	YR07	L10	YI07	L4
XR08	J13	XI08	H3	YR08	N11	YI08	N3
XR09	J12	XI09	J1	YR09	M11	YI09	M3
XR10	J11	XI10	J2	YR10	L11	YI10	L3
XR11	K13	XI11	J3	YR11	L12	YI11	K3
XR12	K12	XI12	K1	NC	B2	NC	M12
XR13	L13	XI13	K2	NC	L2	NC	M2
XR14	M13	XI14	L1	VCC	A1	NC	E11
XR15	K11	XI15	M1	VCC	G3	NC	C3
GND	N12	GND	C7	VCC	E2	GND	N8
GND	N7	GND	A2	VCC	A13	GND	N6
GND	M7	GND	E12	VCC	E13	GND	F11
GND	N2	GND	E3	VCC	N1	IC	B8
GND	A8	GND	B12	VCC	N13	IC	A7

NOTE
IC = Internally connected - do not connect to these pins.
All inputs are internally connected to Vcc by 10k (nominal) resistors.

PIN OUT - PIN TO FUNCTION (PGA Package - AC120)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VCC	GND	PI07	PI10	PI13	PI16	IC	GND	PR15	PR12	PR09	PR06	VCC
B	PI03	NC	PI06	PI09	PI12	PI15	CLK	IC	PR14	PR11	PR08	GND	PR03
C	PI02	PI05	NC	PI08	PI11	PI14	GND	PR16	PR13	PR10	PR07	PR05	PR02
D	PI00	PI01	PI04								PR04	PR01	PR00
E	XI00	VCC	GND								NC	GND	VCC
F	XI03	XI02	XI01								GND	XR00	XR01
G	XI05	XI04	VCC								XR03	XR04	XR02
H	XI06	XI07	XI08								XR07	XR06	XR05
J	XI09	XI10	XI11								XR10	XR09	XR08
K	XI12	XI13	YI11								XR15	XR12	XR11
L	XI14	NC	YI10	YI07	YI04	YI01	CLK	YR01	YR04	YR07	YR10	YR11	XR13
M	XI15	NC	YI09	YI06	YI03	YI00	GND	YR00	YR03	YR06	YR09	NC	XR14
N	VCC	GND	YI08	YI05	YI02	GND	GND	GND	YR02	YR05	YR08	GND	VCC

PIN OUT - PIN TO FUNCTION (PGA Package - AC120)

GG	SIG	GG	SIG	GG	SIG	GG	SIG
84	PR00	95	PR09	8	PI00	115	PI09
85	PR01	96	PR10	7	PI01	114	PI10
86	PR02	97	PR11	6	PI02	113	PI11
87	PR03	98	PR12	5	PI03	112	PI12
88	PR04	99	PR13	4	PI04	111	PI13
89	PR05	100	PR14	3	PI05	110	PI14
92	PR06	101	PR15	118	PI06	109	PI15
93	PR07	102	PR16	117	PI07	108	PI16
94	PR08	46	CLK	116	PI08	105	CLK
79	XR00	11	XI00	49	YR00	43	YI00
78	XR01	12	XI01	50	YR01	42	YI01
77	XR02	13	XI02	51	YR02	41	YI02
76	XR03	14	XI03	52	YR03	40	YI03
75	XR04	15	XI04	53	YR04	39	YI04
74	XR05	17	XI05	54	YR05	38	YI05
73	XR06	18	XI06	55	YR06	37	YI06
72	XR07	19	XI07	56	YR07	36	YI07
71	XR08	20	XI08	57	YR08	35	YI08
70	XR09	21	XI09	58	YR09	34	YI09
69	XR10	22	XI10	59	YR10	33	YI10
68	XR11	23	XI11	63	YR11	28	YI11
67	XR12	24	XI12	1	N/C	29	N/C
66	XR13	25	XI13	16	N/C	31	N/C
65	XR14	26	XI14	2	VCC	61	N/C
64	XR15	27	XI15	10	VCC	83	N/C
9	GND	45	GND	30	VCC	44	GND
32	GND	47	GND	62	VCC	48	GND
60	GND	104	GND	81	VCC	80	GND
82	GND	106	GND	90	VCC	103	I/C
91	GND	120	GND	119	N/C	107	I/C

N/C = Not connected - leave open circuit
I/C = Internally connected - leave open circuit

All GND and VDD pins must be used

PIN DESCRIPTION

XR00 - XR15	X Real Inputs : Two's Complement Format XR15 = MSB (Sign) XR00 = LSB For Fractional Arithmetic the Weighting of XR15 = 1 i.e. -1 ≤XR<1	PR00 - PR16	P Real Inputs : Two's Complement Format PR16 = MSB (Sign) PR00 = LSB For Fractional Arithmetic the Weighting of PR16 = 2 i.e. -2 ≤PR<2
XI00 - XI15	X Imag Inputs : Two's Complement Format XI15 = MSB (Sign) XI00 = LSB For Fractional Arithmetic the Weighting of XI15 = 1 i.e. -1 ≤XI<1	PI00 - PI16	P Imag Outputs : Two's Complement Format PI16 = MSB (Sign) PI00 = LSB For Fractional Arithmetic the Weighting of PI16 = 2 i.e. -2 ≤PI<2
YR00 - YR11	Y Real Inputs : Two's Complement Format YR11 = MSB (Sign) YR00 = LSB For Fractional Arithmetic the Weighting of YR11 = 1 i.e. -1 ≤YR<1	CLK pin B7 and Pin L7	Common Clock to all on chip registers, both pins must be connected
		VCC GND	All VCC and GND pins must be connected
YI00 - YI11	Y Imag Inputs : Two's Complement Format YI11 = MSB (Sign) YI00 = LSB For Fractional Arithmetic the Weighting of YI11 = 1 i.e. -1 ≤YI<1	IC	Internally connected - do not use

FUNCTIONAL DESCRIPTION

The PDSP16112 Complex Multiplier contains four pipeline 16 x 12 Array Multipliers, a 17-bit adder and a 17-bit subtractor.

The multipliers accept data from the XR, XI, YR, and YI inputs and perform the four multiplies necessary to implement a Complex Multiply Operation.

$$(XR \times YR,\ XR \times YI,\ XI \times YR,\ XI \times YI).$$

The 28-bit results from these operations are rounded to the most significant 16-bits before being passed to the adder and subtractor. The subtractor calculates

$$(XR \times YR) - (XI \times YI)$$

to form a 17-bit result representing the real result of the complex multiplication. The adder calculates

$$(XR \times YI) + (XI \times YR)$$

to form a 17-bit result that represents the imaginary result of the complex multiplication. These real and imaginary results are passed to the PR and PI outputs respectively.

The add and subtract operations may (depending upon the data) cause the multiplier results to grow by one bit hence requiring 17-bit outputs to represent the results. The PDSP16112 is designed to operate with two's complement arithmetic, hence if the Fractional two's complement format is used the outputs will lie in the range

$$-2 \leq P < 2$$

for inputs in the range

$$-1 \leq X \text{ or } Y < 1$$

If the output magnitude lies in the range

$$-1 \leq P < 1,$$

then the 17th (MSB) bit of the outputs will duplicate the 16th (Sign) bit of the output.

In common with other Array multipliers, the operation

$$-1 \times -1$$

will yield an incorrect result for fractional two's complement formats, and hence should be avoided.

Both X and Y inputs are registered as are the PR and PI outputs. On the rising edge of CLK data present on the XR, XI, YR and YI inputs is clocked into the input registers. At the same time a new result is clocked into the output registers and made available on the PR and PI output ports.

Pipelined Operation

The internal Multiply and Add operations are divided into stages by six internal pipeline registers giving a total latency through the device of eight clock cycles. This means that the result from data loaded into the device on the first clock cycle appears at the outputs during the seventh clock cycle, and may be loaded into another device on the eigth clock cycle.

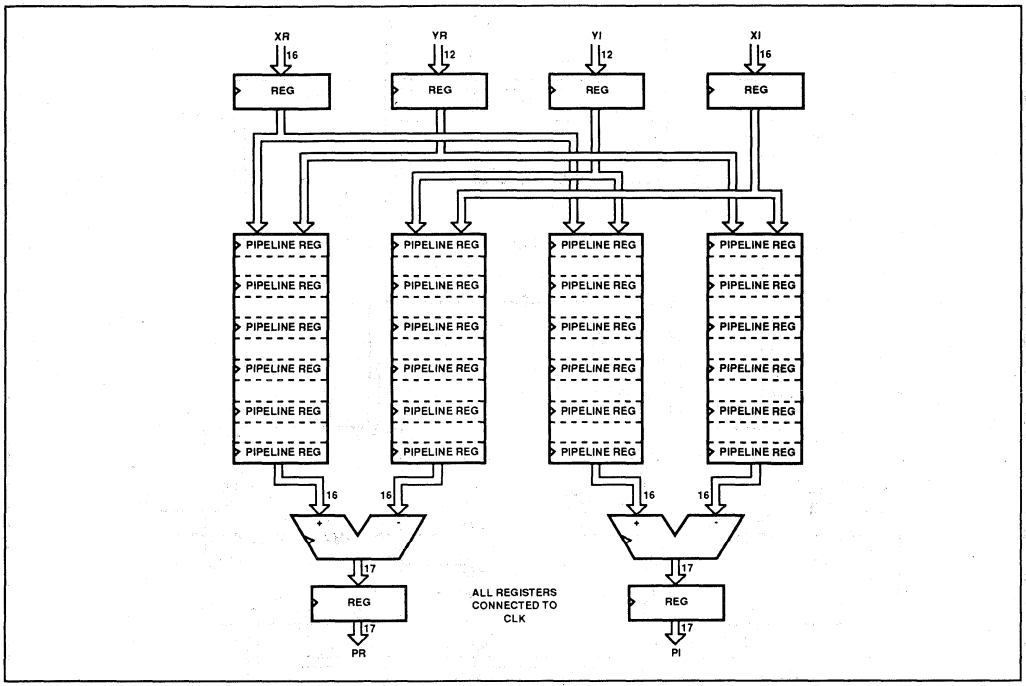


Fig.3 Pipeline multiplier structure

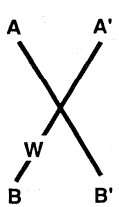
TYPICAL APPLICATION

The PDSP16112A may be configured as the main arithmetic element in the FFT Butterfly calculation. A single PDSP16112A together with two PDSP16318As will produce an arithmetic processor capable of executing a new Radix 2 DIT Butterfly every 50ns using 16-bit data and 12-bit coefficients. The PDSP16318A provides flags that monitor the magnitude of the output data, together with on chip shift circuits.

A single Butterfly processor of this type will allow the following FFT benchmarks.

1024 point complex radix 2 transform in 256µsecs
512 point complex radix 2 transform in 115µsecs
256 point complex radix 2 transform in 51µsecs

The arithmetic operation required to realise a radix 2 decimation in time algorithm is as follows.



$$A' = A + (B \times W)$$

$$B' = A - (B \times W)$$

Where A and B are the data inputs, A' and B' are the data outputs, and W is the coefficient. A,B,A',B' and W are all complex numbers i.e. they all have real and imaginary components. The Butterfly therefore requires one complex multiply and two complex adds to execute, which is equivalent to four real multiplies and six real adds.

Fig.4 illustrates the interconnection of the PDSP16112A with the two PDSP16318A Complex Accumulators. The PDSP16112A performs the complex multiply operation at the full 20MHz rate to provide the real and imaginary components of the (B x W) to the two ALUs. The PDSP16318A is capable of 16-bit operations at 20MHz and has on chip register storage and Shifter. In every 20MHz cycle each PDSP16318A performs two arithmetic operations to calculate the real or imaginary parts of A + (B x W) and A - (B x W). One of the PDSP16318As calculates the real parts and the other calculates the imaginary parts.

For greater throughput one chip-set mat be allocated to each column of the FFT. For example, a 1K complex FFT could be calculated by 10 chip-sets every 26µs.

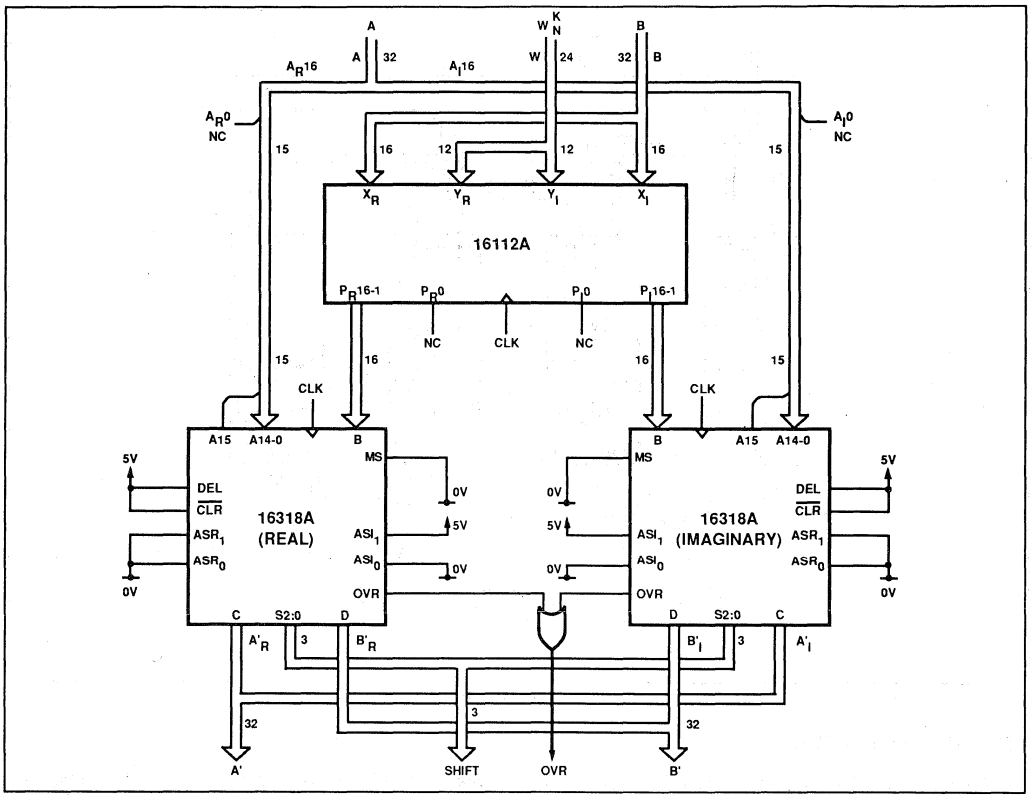


Fig.4 Radix 2 DIT butterfly processor

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} (Industrial) =-40°C to +85°C, Vcc = 5.0V ± 10%, GND = 0V

T_{amb} (Military) =-55°C to +125°C, Vcc = 5.0V ± 10%, GND = 0V

T_{amb} (Commercial) = 0°C to +70°C, Vcc = 5.0V ± 5%, GND = 0V

Static Characteristics

Characteristics	Symbol	Value						Units	Conditions
		PDSP16112			PDSP16112A				
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4			2.4			V	I_{OH} = 4mA
Output low voltage	V_{OL}			0.6			0.6	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.8			2.8			V	
Input low voltage	V_{IL}			0.8			0.8	V	
Input leakage current *	I_{IL}	-1.2		+0.01	-1.2		+0.01	mA	GND ≤ V_{IN} ≤ V_{CC}
Output short circuit current	I_{OS}	30		200	40		200	mA	V_{CC} = max
Input capacitance	C_I		10			10		pF	

* All inputs have a nominal 10K pull resistor to Vcc.

AC Characteristics

Characteristic	Symbol	Value Industrial						Value Military		Units	Conditions
		PDSP16112			PDSP16112A						
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.		
Vcc current	Icc			90			170		90	mA	Vcc = max Outputs unloaded f_{CLK} = max
Max. CLK frequency	fCLK	10			20			10		MHz	
Min. CLK frequency				DC			DC		DC		
Input setup time	tSU			30			20		30	ns	
Input hold time	tih			5			5		5	ns	
CLK to output delay	td	5		50	5		30	5	50	ns	
CLK Mark/Space ratio		40		60	40		60	40	60	%	
Drive capability		2 x LSTTL +20pF									

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage Vcc	-0.5V to 7.0V
Input voltage VIN	-0.5V to Vcc +0.5V
Output voltage VOUT	-0.5V to Vcc +0.5V
Clamp diode current per Ik (see Note 2)	±18mA
Static discharge voltage	500V
Storage temperature range Ts	-65°C to +150°C
Junction temperature	150°C
Ambient temperature with power applied Tamb	
Commercial	0°C to +70°C
Industrial	-44°C to +85°C
Military	-55°C to +125°C
Package power dissipation PTOT	1000mW

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Package Type	θJC °C/W	θJA °C/W
AC	12	35

ORDERING INFORMATION

Industrial (-40°C to +85°C)

PDSP16112A B0 AC (20MHz - PGA)
PDSP16112A B0 GG (20MHz - QFP)

Military (-55°C to +125°C)

PDSP16112 A0 AC (10MHz - PGA)
PDSP16112A A0 AC (20MHz - PGA)
PDSP16112A A0 GG (20MHz - QFP)

Call for availability on High Reliability parts and MIL-883C screening.

PDSP16116/A

16 BY 16 BIT COMPLEX MULTIPLIER

(Supersedes version October 1995 verison, DS3707 - 3.0)

The PDSP16116A will multiply two complex (16 + 16) bit words every 50ns and can be configured to output the complete complex (32 + 32) bit result within a single cycle. The data format is fractional two's complement.

The PDSP16116/A contains four 16 x 16 Array Multipliers, two 32 bit Adder/Subtractors and all the control logic required to support Block Floating Point Arithmetic as used in FFT applications. In combination with a PDSP16318, the PDSP16116A forms a two chip 10MHz Complex Multiplier Accumulator with 20 bit accumulator registers and output shifters. The PDSP16116 in combination with two PDSP16318s and two PDSP1601s forms a complete 10MHz Radix 2 DIT FFT Butterfly solution which fully supports Block Floating Point Arithmetic. The PDSP16116/A has an extremely high throughput that is suited to recursive algorithms as all calculations are performed with a single pipeline delay (two cycle fall-through).

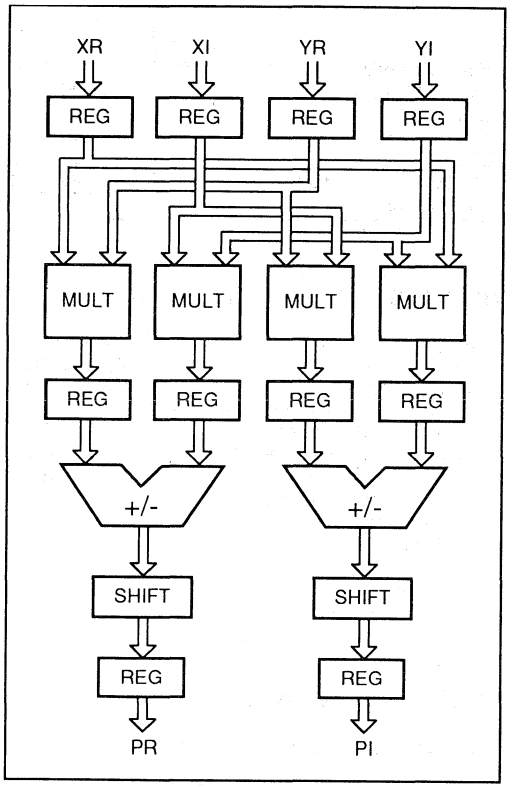


Fig.1 Simplified Block Diagram

FEATURES

- Complex Number (16 + 16) X (16 + 16) Multiplication
- Full 32 bit Result
- 20MHz Clock Rate
- Block Floating Point FFT Butterfly Support
- -1 times -1 Trap
- Two's Complement Fractional Arithmetic
- TTL Compatible I/O
- Complex Conjugation
- 2 Cycle Fall Through
- 144 pin PGA or QFP packages

APPLICATION

- Fast Fourier Transforms
- Digital Filtering
- Radar and Sonar Processing
- Instrumentation
- Image Processing

ASSOCIATED PRODUCTS

PDSP16318/A	Complex Accumulator
PDSP16112/A	(16 + 16) X (12 + 12) Complex Multiplier
PDSP16330/A	Pythagoras Processor
PDSP1601/A	ALU and Barrel Shifter
PDSP16350	Precision Digital Modulator
PDSP16256	Programmable FIR Filter
PDSP16510	Single Chip FFT Processor

The PDSP16116 has a number of features tailored for System applications.

-1 x -1 Trap

In multiply operations utilising Twos Complement Fractional notation, the -1 x -1 operation forms an invalid result as +1 is not representable in the fractional number range. The PDSP16116/A eliminates this problem by trapping the -1 x -1 operation and forcing the Multiplier result to become the most positive representable number.

Complex Conjugation

Many algorithms utilising complex arithmetic require conjugation of complex data stream. This operation has traditionally required an adiditional ALU to multiply the imaginary component by -1. The PDSP16116 eliminates the requirement for the extra ALU by offering on chip complex conjugation of either of the two incoming complex data words with no loss in throughput.

Easy Interfacing

As with all PDSP family members the PDSP16116 has registered I/O for data and control. Data inputs have independent clock enables and data outputs have independent three state output enables.

Signal	Type	Description	Normal mode Configuration
XR15:0	INPUT	16 bit input for real x data	
XI15:0	INPUT	16 bit input for imag x data	
YR15:0	INPUT	16 bit input for reaal y data	
YI15:0	INPUT	16 bit input for imag y data	
PR15:0	OUTPUT	16 bit output for real p data	
PI15:0	OUTPUT	16 bit output for img p data	
CLK	INPUT	Clock, new data is loaded on rising edge of CLK	
CEX	INPUT	Clock, enable X-port input register	
CEY	INPUT	Clock, enable Y-port input register	
CONX	INPUT	Conjugate X data	
CONY	INPUT	Conjugate Y data	
ROUND	INPUT	Rounds the real & imag results	
MBFP	INPUT	Mode select (BFP/Normal)	Tie Low
SOBFP	INPUT	Start of BFP operations **	Tie Low
EOPSS	INPUT	End of pass **	Tie Low
AR15:13	INPUT	3 MSB's from real part of A-word **	Tie Low
AI15:13	INPUT	3 MSB's from imag part of A-word **	Tie Low
WTA1:0	INPUT	Word tag from A-word	Tie Low
WTB1:0	INPUT	Word tag from B-word / shift control *	
WTOUT1:0	OUTPUT	Word tag output **	
SFTA1:0	OUTPUT	Shift control for A-word / overflow flag *	
SFTR2:0	OUTPUT	Shift control for accumulator resul **	
GWR4:0	OUTPUT	Global weighting register contents **	
OSEL1:0	INPUT	Selects the desired output configuration	
OER, OEI	INPUT	Output enables	
VDD	POWER	+5V Supply All supply pins	
GND	POWER	0V Supply must be connected	

* Indicates pin performs different functions in BFP / Normal modes.
** Indicates pin is used only in BFP mode

Table.1 Signal Descriptions

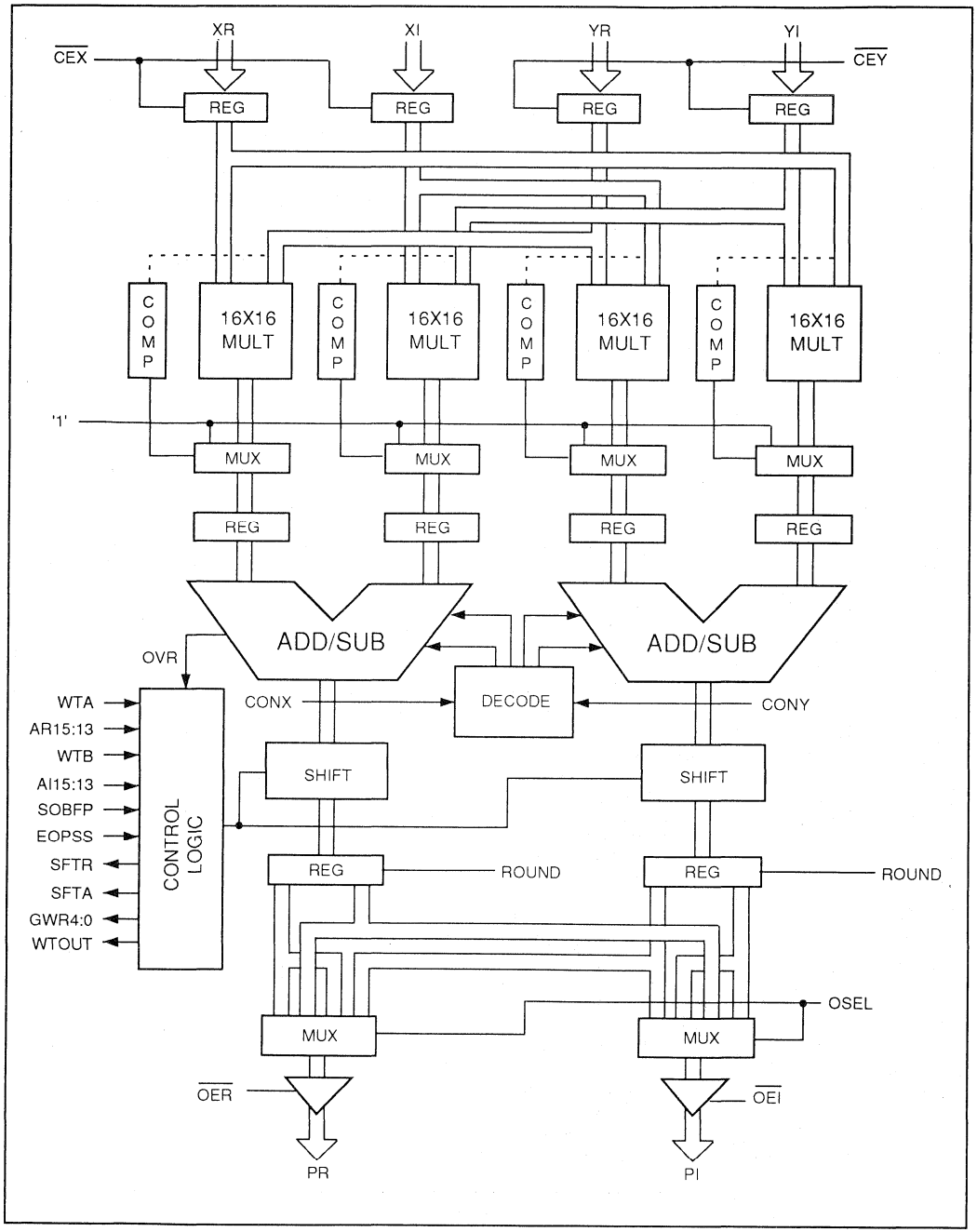


Fig.2 Block Diagram

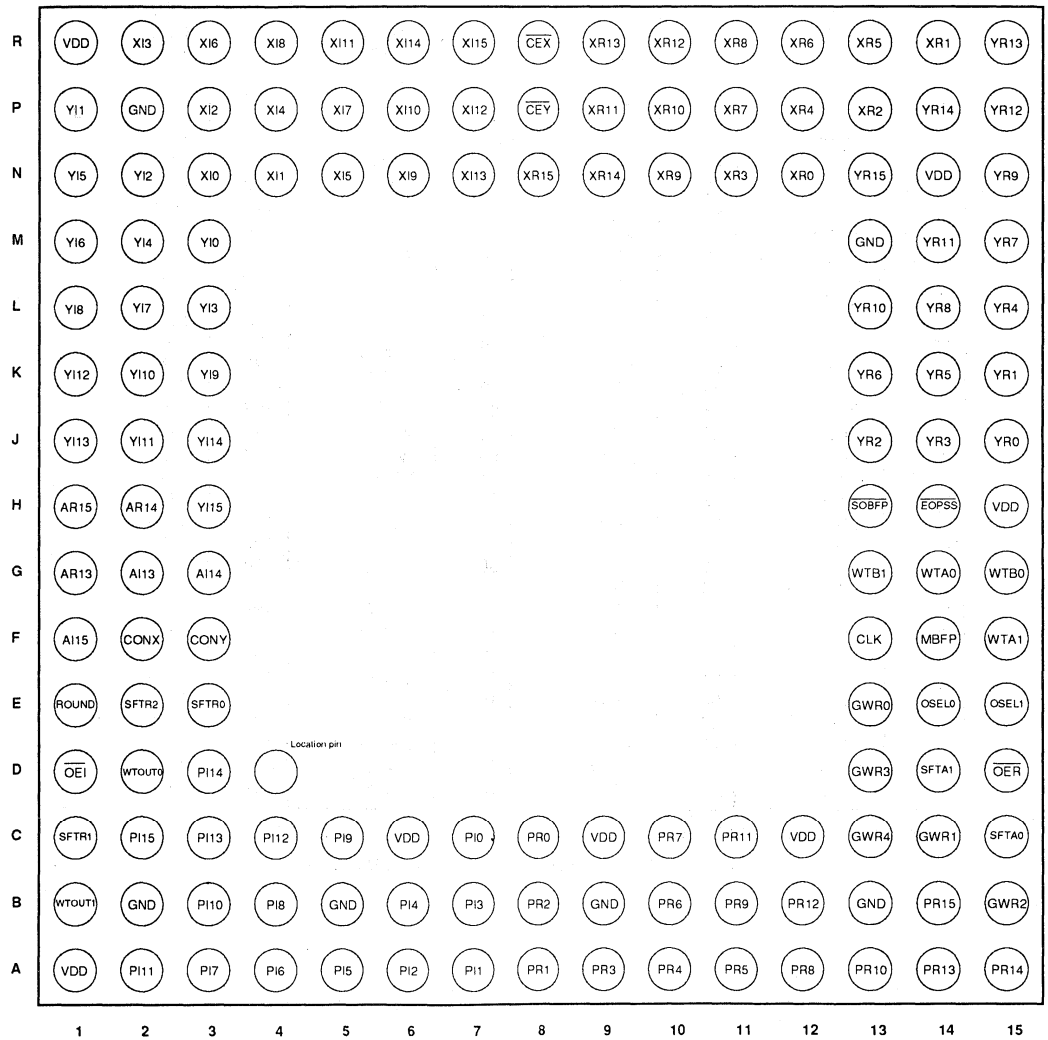


Fig.3 Pin Allocation Diagram (Bottom View)
144 pin PGA - AC144

GG	SIG	GG	SIG	GG	SIG	GG	SIG
1	PI14	37	XI1	73	GND	109	VDD
2	PI15	38	XI2	74	VDD	110	GND
3	WTOUT1	39	XI3	75	YR12	111	PR13
4	WTOUT0	40	XI4	76	YR11	112	PR12
5	SFTR0	41	XI5	77	YR10	113	PR11
6	SFTR1	42	XI6	78	YR9	114	PR10
7	SFTR2	43	XI7	79	YR8	115	PR9
8	$\overline{\text{OEI}}$	44	XI8	80	YR7	116	PR8
9	CONX	45	XI9	81	YR6	117	PR7
10	CONY	46	XI10	82	YR5	118	PR6
11	ROUND	47	XI11	83	YR4	119	PR5
12	AI13	48	XI12	84	YR3	120	GND
13	AI14	49	XI13	85	YR2	121	VDD
14	AI15	50	XI14	86	YR1	122	PR4
15	AR13	51	XI15	87	YR0	123	PR3
16	AR14	52	$\overline{\text{CEY}}$	88	$\overline{\text{EOPSS}}$	124	PR2
17	AR15	53	$\overline{\text{CEX}}$	89	VDD	125	PR1
18	YI15	54	XR15	90	$\overline{\text{SOBFP}}$	126	PR0
19	YI14	55	XR14	91	$\overline{\text{WTB1}}$	127	PI0
20	YI13	56	XR13	92	WTB0	128	PI1
21	YI12	57	XR12	93	WTA1	129	PI2
22	YI11	58	XR11	94	WTA0	130	PI3
23	YI10	59	XR10	95	MBFP	131	PI4
24	YI9	60	XR9	96	CLK	132	VDD
25	YI8	61	XR8	97	OSEL1	133	PI5
26	YI7	62	XR7	98	OSEL0	134	GND
27	YI6	63	XR6	99	$\overline{\text{OER}}$	135	PI6
28	YI5	64	XR5	100	$\overline{\text{SFTA0}}$	136	PI7
29	YI4	65	XR4	101	SFTA1	137	PI8
30	YI3	66	XR3	102	GWR0	138	PI9
31	YI2	67	XR2	103	GWR1	139	PI10
32	YI1	68	XR1	104	GWR2	140	PI11
33	YI0	69	XR0	105	GWR3	141	PI12
34	XI0	70	YR15	106	GWR4	142	PI13
35	GND	71	YR14	107	PR15	143	GND
36	VDD	72	YR13	108	PR14	144	VDD

All GND and VDD pins must be used.

Fig.3A Pin Allocation Diagram - 144 pin ceramic QFP - GG144

NORMAL MODE OPERATION

When the MBFP mode select input is held low the 'Normal' mode of operation is selected. This mode supports all Complex Multiply operations that do not require Block Floating Point arithmetic.

Multiplier Stage

Complex two's complement fractional data is loaded into the X and Y input registers via the X and Y Ports on the rising edge of CLK. The Real and Imaginary components of the fractional data are each assumed to have the following format

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WEIGHTING	S	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Where S = sign bit which has an effective weighting -2^0

The value of the 16 bit two's complement word is

Value = $(-1xS)+(bit14x2^{-1})+(bit13x2^{-2})+(bit12x2^{-3})$. . .

The X & Y port registers are individually enabled by the CEX & CEY signals respectvely. If the registers are required to be permanently enabled, then these signals may be tied to ground. On each clock cycle the contents of the input registers are passed to the four multipliers to start a new Complex Multiply operation. Each Complex Multiply operation requires four partial products (Xr x Yr), (Xr x Yi), (Xi x Yr), (Xi x Yi), all of which are calculated in parallel by the four 16 x 16 Multipliers. Only one clock cycle is required to complete the multiply stage before the Mutliplier results are loaded into the Multiplier output registers for passing on to the Adder/Subtractors in the next cycle. Each multiplier produces a 31 bit result with the duplicate sign bit eliminated. The format of the output data from the Multipliers is

BIT NUMBER	30	29	28	27	26	25	24	...	7	6	5	4	3	2	1	0
WEIGHTING	S	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	...	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

The effective weighting of the sign bit is -2^0

Result Correction

Due to the nature of the fraction twos complement representation it is possible to represent -1 exactly but not 1. With conventional multipliers this causes a problem when -1 is multiplied by -1 as the multiplier produces an incorrect result. The PDSP16116 includes a trap to ensure that the most positive number (value = 1.2^{-30}), (hex = 7FFFFFFF) is subsituted for the incorrect result. The multiplier result is therefore always a (correct) fractional value.

Complex Conjugation

Either the X or Y input data may be complex conjugated by asserting the CONX or CONY signals respectively. Asserting either of these signals has the effect of inverting (multiplying by -1) the imaginary component of the respective input. Table 3 shows the effect of CONX and CONY on the X and Y inputs.

FUNCTION	OPERATION	CONX	CONY
X x Y	(XR+XI)x(YR+YI)	low	low
X x Conj Y	(XR+XI)x(YR-YI)	high	low
Conj X x Y	(XR-XI)x(YR+YI)	low	high
Invalid	Invalid	high	high

Table 3 Conjugate Functions

Adder / Subtractor Stage

The 31 bit Real and Imaginary results from the Multipliers are passed to two 32 bit Adder/Subtractors. The Adder calculates the imaginary result ((Xr x Yi) + (Xi x Yr)) and the Subtractor calculates the Real result ((Xr x Yr) = (Xi x Yi)). Each Adder/Subtractor produces a 32 bit result with the following format.

BIT NUMBER	31	30	29	28	27	26	...	8	7	6	5	4	3	2	1	0
WEIGHTING	S	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	...	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

The effective weighting of the sign bit is -2^1

Rounding

The ROUND control when asserted rounds the most significant 16 bits of the full 32 bit result from the shifter. If the ROUND signal is active (High), then bit 16 is set to a one, rounding the most significant 16 bits of the shifted result. (The least siginificant 16 bits are unaffected). Inserting a one ensures that the rounding error is never greater than 1LSB, and that no DC bias is introduced as a result of the rounding processes.

The format of the Rounded result is;

BIT NUMBER	31	30	29	28	27	...	18	17	16	15	14	13	...	2	1	0
WEIGHTING	S	2^{0}	2^{-1}	2^{-2}	2^{-3}	...	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	...	2^{-28}	2^{-29}	2^{-30}
	ROUNDED VALUE													LSB's		

The effective weighting of the sign is -2^1

Shifter

Each of the two Adder/Subtractors are followed by Shifters controlled via the WTB control input. These shifters can each apply two different shifts, however the same shift is applied to both real and imaginary components. The two shift options are:

i) WTB1:0 = 11 Shift complex product one place to the left.

The effective weighting of the sign bit is -2^0

ii) WTB1:0 = 00, 01 or 10 Shift complex product three place to the right. The effective weighting of the sign bit is -2^4.

Overflow

If the left shift option is selected and the Adder/Subtractor contain a 32 bit word, then an invalid result will be passed to the output. An invalid output arising from this combination of events will be flagged by the SFTA0 flag output. The SFTA0 Flag will go high if either the real or imaginary reslut is invalid.

Output Select

The output from the Shifters is passed to the Output Select Mux, which is controlled via the OSEL inputs. These inputs are not registered and hence allow the output combination to be changed within each cycle. The full complex 64 bit result from the multiplier may therefore be output within a single cycle. The OSEL control selects four different output combinations as as summarised in Table 4.

OSEL1	OSEL0	PR	PI
0	0	MSR	MSI
0	1	LSR	LSI
1	0	MSR	LSR
1	1	MSI	LSI

Table 3 Output Selection

(Where MSR and LSR are the most and least siginificant 16 bit words of the Real Shifter output, MSI and LSI are the most and least significant 16 bit words of the imaginary Shifter output).

The output select options allow two different modes for extracting the full 32 bit result from the PDSP16116. The first mode treats the two 16 bit outputs as real and imaginary ports allowing the real and imaginary results to be output in two halves on the real and imaginary output ports. The second mode treats the two 16 bit outputs as one 32 bit output and allows the real and imaginary results to be output as 32 bit words.

PIN DESCRIPTIONS

XR, XI, YR, YI

Data inputs 16 bits: Data is loaded into the input registers from these ports on the rising edge of CLK. The data format is Twos Complement Fractional, where the MSB (sign bit) is bit 15. In normal mode the weighting of the MSB is -20 ie -1.

PR, PI

Data outputs 16 bits: Data is clocked into the output registers and passed to the PR and PI outputs on the rising edge of CLK. The data format is Twos Complement Fractional. The field of the internal result selected for output via PR and PI is controlled by signals OSEL1:0 (see Table 4).

CLK

Common Clock to all internal register.

CEX, CEY

Clock enables for X and Y input ports: When low these inputs enable the CLK signal to the X or Y input registers allowing new data to be clocked into the Multiplier.

CONX, CONY

If either of these inputs are high on the rising edge of CLK, then the data in the associated input has its imaginary component inverted (multiplied by -1), see Table 3. CONX and CONY affect data input on the same clock rising edge.

ROUND

The ROUND control is used to round the most siginficant 16 bits of the output register. The rounding operation takes place one cycle after the ROUND input is taken high. The ROUND input is not latched and is intended to be tied high or low depending upon the application.

MBFP

Mode select: When high, Block Floating Point (BFP) mode is selected. This allows the device to maintain the dynamic range of the data using a series of word tags. This is especially useful in FFT appllications. When low, the chip operates in normal mode for more general applications. This pin is intended to be tied high or low, depending on application.

SOBFP (BFP MODE ONLY)

Start of BFP: This input should be held low for the first cycle of the first pass of the BFP calculations (see Fig.7). It serves to reset the internal registers associated with BFP control. When operating in normal mode this input should be tied low.

EOPSS (BFP MODE ONLY)

End of pass: This input should be held low for the last cycle of each pass and for the lay time between passes. It instructs the control logic to update the value of the global weighting register and prepare the BFP circuitry for the next pass. When operating in normal mode this input should be tied low.

AR15:13 (BFP MODE ONLY)

Three Msbs of the real part of the A-word : These are used in the FFT butterfly application to deteremine the magnitude of the real part of the A-word and, hence, to determine if there will be any chage of word growth in the PDSP16318 Complex Accumulator. When operating in normal mode, these inputs are not used and may be tied low.

AI15:13 (BFP MODE ONLY)

Three Msbs of the imaginary part of the A-word : used in the same fashion as AR.

SFTR2:0 (BFP MODE ONLY)

Accumulator result shift control. These pins should be linked directly to the S2:0 pins on the PDSP16318 Complex Accumulator. They control the accumulator's barrel shifter (see Table 5). The purpose of this shift is to minimise sign extension in the multiplier or accumulator ALU's. When operating in normal mode, these output are superfluous.

SFTR2:0	FUNCTION
0 0 0	Reserved
0 0 1	Reserved
0 1 0	Reserved
0 1 1	Shift right by one
1 0 0	No shift
1 0 1	Shift left by one
1 1 0	Shift left by two
1 1 1	Reserved

Table 5 Auccumulator Shifts (BFP mode)

GWR4:0 (BFP MODE ONLY)

Contents of the global weighting register: This stores the weighting of the largest word present with respect to the weighting of the original input words. Hence, if the contents of the GWR are 00010, this indicates that the largest word currently being processed has its binary point two bits to the right of the original data at the start of the BFP calculations. The contents of this register are updated at the end of each pass, according to the largest value of WTOUT occuring during that pass. (i.e. If WTOUT = 11, then GWR will be increased by 2). The GWR is presented in two's complement format. These outputs are superfluous in normal mode.

WTOUT1:0 (BFP MODE ONLY)

Word tag output. This tag records the weighting of the output words from the current cycle relative to the current global weighting register (see Table 6). It should be stored along with the A' and B' words as it will form the input word tags, WTA and WTB, for each complex word during the next pass. These outputs are superfluous in normal mode.

WTOUT1:0	Weighting of the output relative to the current global weighting register
0 0	One less
0 1	The same
1 0	One more
1 1	Two more

Table 6 Word Tag Weightings

WTA1:0 (BFP MODE ONLY)

Word tag from the A-word. This word records the weighting of the A-word relative to the global weighting register on the previous pass. Although the A-word inself is not processed in the PDSP16116, this information is required by the control logic for the radix-2 butterfly FFT application. These inputs should be tied low in normal mode.

WTB1:0 (BFP & NORMAL MODES)

In BFP mode, this is the word tag from the B-word. This is operated in the same manner as WTA but for the B-word. The value of the word tags are used to ensure that the binary weighting of the A word and the product of the complex multiplier are the same at the inputs to the complex accumulator. Depending on which word is the larger, the weighting adjustment is performed using either the internal shifter or an external shifter controlled by SFTA. The word tags are also used to maintain the weighting of the final result to within plus two and minus one binary points relative to the new GWR. (On the first pass all word tags will be ignored).

In normal mode, these inputs perform a different function. They directly control the internal shifter at the output port as shown in Table 7.

WTB1:0	FUNCTION
11	shift complex product one place to the left
00, 01, 10	shift complex product three places to the right

Table 7 Normal Mode Shift Control

SFTA1:0 (BFP & NORMAL MODES)

In BFP mode, these signals act as as the A-word shift control. They allow shifting from one to four places to the right, see Table 8. Depending on the relative weightings of the A-words and the complex product, the A-word may have to be shifted to the right to ensure compatible weightings at the inputs to the PDSP16318 complex accumulator. (The two words must have the same weighting if they are to be added).

In normal mode, SFTA0 performs a different a different function. If WTB1:0 is set to implement a left shift, then overflow will occur if the data is fully 32 bits wide. This pin is used to flag such an overflow. SFTA1 is not used in normal mode.

WTB1:0	FUNCTION
0 0	Shift A-word 1 places to the right
0 1	Shift A-word 2 places to the right
1 0	Shift A-word 3 places to the right
1 1	Shift A-word 4 places to the right

Table 8 External A-word shift control

OSEL1:0

The outputs from the device are selected by the OSEL0 & OSEL1 instruction bits. These controls allow selection of the output combination during the current cycle. (They are not registered). These are four possible output configurations that allow either complex outputs of the most or least significant bytes, or real or imaginary outputs of the full 32 bit word (see Table 4). OSEL0 and OSEL1 should both be tied low when in BFP mode.

BFP MODE FFT APPLICATION

The PDSP16116 may be used as the main arithmetic unit of the butterfly processor which will allow the following FFT benchmarks:

1024 point complex radix-2 transform in 517us
512 point complex radix-2 transform in 235us
256 point complex radix-2 transform in 106us

In addition, with pin MBFP tied high, the BFP circuitry within the PDSP16116 can be used to adaptively rescale data throughout the course of the FFT so as to give high-resolution results.

The BFP system on the PDSP16116 can be used with any variation of the Radix-2 Decimation-In-Time FFT - e.g. the Constant Geometry algorithm, the In-Place algorithm etc. An N-point Radix-2 DIT FFT is split into log (N) passes. Each pass consists of N/2 'butterflies', each performing the operation:

$A' = A + B.W$
$B' = A - B.W$

Where W is the complex coefficient and A & B are the complex data.

Fig.4 illustrates how a single PDSP16116 may be combined with two PDSP1601's and two PDSP16318's to form a complete BFP butterfly processor. The PDSP16318's are used to perform the complex addition and subtraction of the butterfly operation, while the PDSP1601's are used to match the data path of the A-word to the pipelining and shifting operations within the PDSP16116.

For more information on the theory and construction of this butterfly processor, refer to application note AN59.

BFP MODE OPERATION

The BFP mode on the PDSP16116 is intended for use in the FFT application described above. i.e. it is intended to prevent data degredation during the course of an FFT calculation. The operation of the PDSP16116 based BFP butterfly processor (see Fig.4) is described below.

The Block Floating Point System

A block floating point system is essentially an ordinary integer arithmetic system with some clever logic bolted on. The object of the extra logic is to lend the system some of the enormous dynamic range afforded by a true floating point system without suffering the corresponding loss in performance.

The initial data used by the FFT should all have the same binary arithmetic weighting. i.e. the binary point should occupy the same position in every data word, as is normal in integer arithmetic. However, during the course of the FFT, a variety of weightings are used in the data words to increase the dynamic range available. This situation is similar to that within a true floating point system, though the range of numbers representable is more limited. In the BFP system used in the PDSP16116, there are, within any one pass of the FFT, four possible positions of the binary point wihin the integer words. To record the position of its binary point, each word has a 2-bit word tag associated with it. By way of example, in a particular pass we may have the following four positions of binary point avaiable, each denoted by a certain value of word tag:

XX.XXXXXXXXXXX	word tag = 00
XXX.XXXXXXXXXX	word tag = 01
XXXX.XXXXXXXXX	word tag = 10
XXXXX.XXXXXXXX	word tag = 11

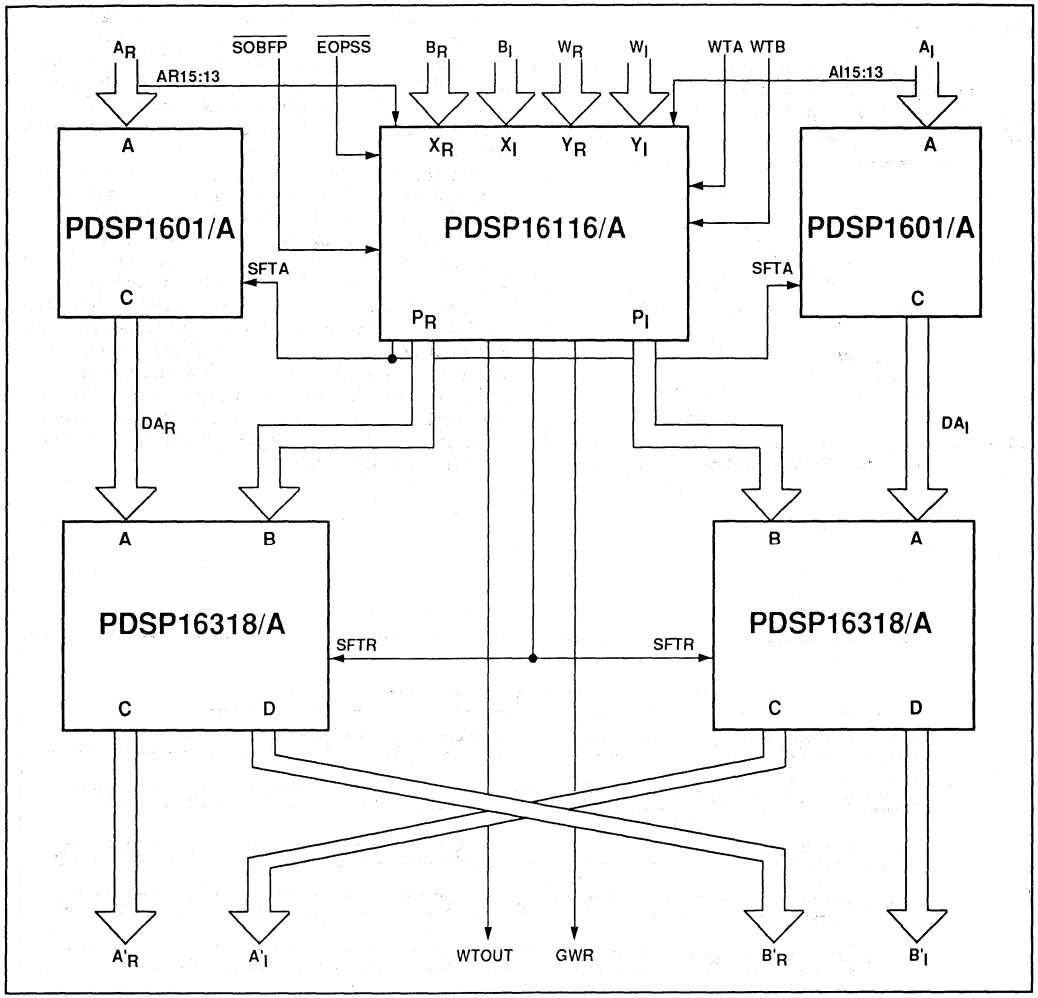


Fig.4 FFT Butterfly Processor

At the end of each constituent pass of the FFT, the positions of the binary point supported may change to reflect the trend of data increase or decreases in magnitude. Hence, in the pass following that of the above example, the four positions of binary point supported may be change to:

XX.XXXXXXXXXX	word tag = 00
XXX.XXXXXXXXX	word tag = 01
XXXX.XXXXXXXX	word tag = 10
XXXXX.XXXXXXX	word tag = 11

This variation in the range of binary points supported from pass to pass (i.e. the movement of the binary point relative to its position in the original data) is recorded in the GWR.

Thus we can determine the position of the binary point relative to its initial position by modifying the value of GWR by WTOUT for a given word as shown in Table 6.
As an example, if GWR=01001 and WTOUT=10 then the binary point has moved 10 places to the right of its original position.

The butterfly operation

The butterfly operation is the arithmetic operation which is repeated many times to produce an FFT. The PDSP16116A based butterfly processor performs this operation in a low power high accuracy chip set.

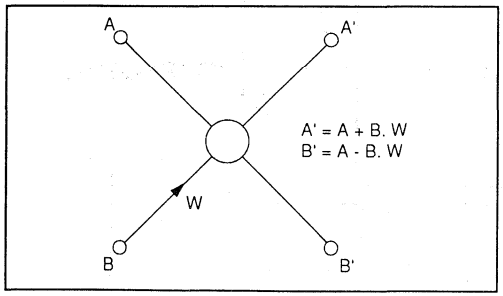


Fig.5 Butterfly Operation

A new butterfly operation is commenced each cycle, requiring a new set of data for , B, W, WTA and WTB. Five cycles later, the corresponding results A' and B' are produced along with their associated WTOUT. In between, the signals SFTA and SFTR are produced and acted upon by the shifters in the PDSP1601/A and PDSP16318/A. The timing of the data and control signals is shown in Fig.6.

The results (A' and B') of each butterfly calculation in a pass must be stored away to be used later as the input data (A and B) in the next pass. Each result must be stored together with its associated word tag, WTOUT. Although WTOUT is common to both A' and B', it must be stored separately with each word as the words are used on different cycles during the next pass. At the inputs, the word tag associated with the A word is known as WTA and the word tag associated with the B word is known as WTB. Hence, the WTOUTs from one pass will become the WTAs and WTBs for the following pass. It should be noted that the first pass is unique in that word tags need not be input into the butterfly as all data initially has the same weighting. Hence, during the first pass alone, the inputs WTA and WTB are ignored.

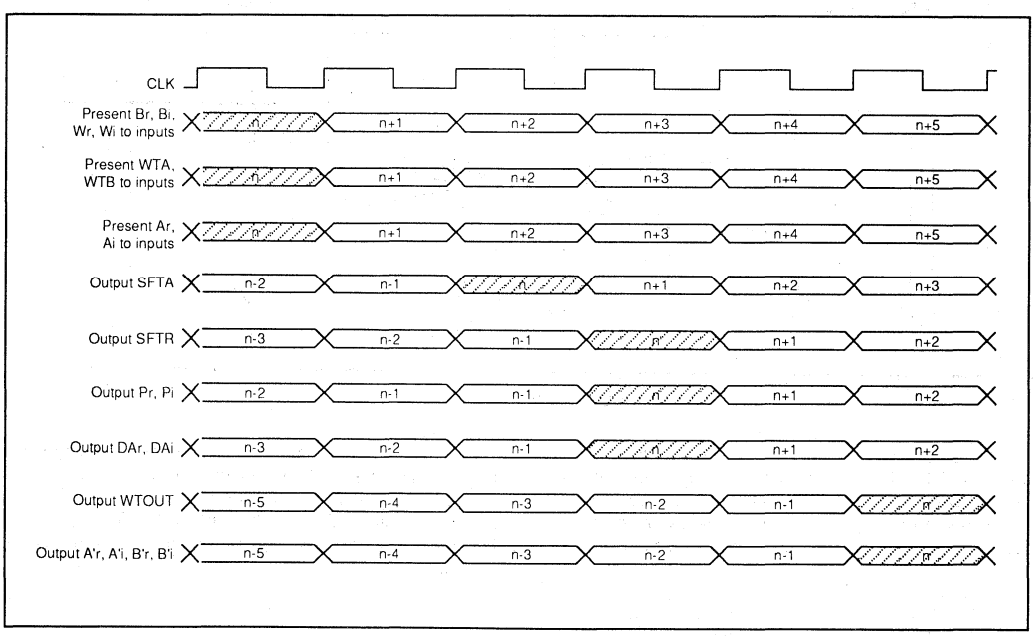


Fig.6 Butterfly Data and Control Signals

Control of the FFT

To enable the block floating point hardware to keep track of the data, the following signals are provided :

SOBFP - start of the FFT

EOPSS - end of current pass

These inform the PDSP16116/A when an FFT is starting and when each pass is complete. Fig.7 shows how these signals should be used and a commentary is provided below.

To commence the FFT, the signal EOPSS should be set high (where it will remain for the duration of the pass). SOBFP should be pulled low during the initial cycle when the first data words A and B are presented to the inputs of the butterfly processor. The following cycle SOBFP must be pulled high where it should remain for the duration of the FFT. New data is presented to the processor each successive cycle until the end of the first pass of the FFT. On the last cycle of the pass, the signal EOPSS should be pulled low and remain low for a minimum of five cycles *, the time required to clear the pipeline of the butterfly processor so that all the results from one pass are obtained before commencing the following pass. On the initial cycle of each new pass, the signal EOPSS should be pulled high and it should remain high until the final cycle of that pass, when it is pulled low again.

* Should a longer pause be required between passes - to arrange the data for the next pass, for example, then EOPSS may be kept low as long as necessary - the next pass cannot commence until it is brought high again.

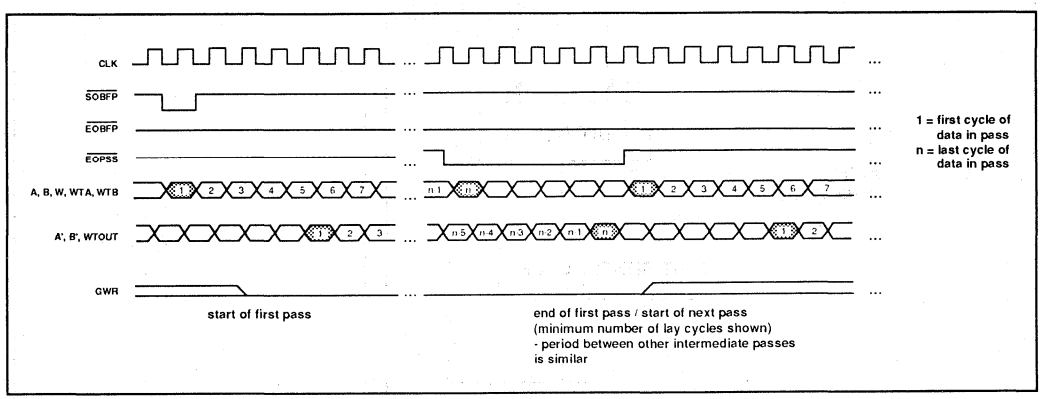


Fig.7 Use of the BFP Control Signals

FFT Output Normalisation

When an FFT system outputs a series of FFT results for display, storage or transmission, it is essential that all results are compatible, i.e. with the binary point in the same position. However, in order to preserve the dynamic range of the data in the FFT calculation, the PDSP1601/A employs a range of different weightings. Therefore, data must be re-formatted at the end of the FFT to be pre-determined common weighting. This can be done by comparing the exponent of given data word with the pre-determined unversial exponent and then shifting the data word by the difference. The PDSP1601/A, with its multifunction 16 bit barrel shifter, is ideally suited to this task.

What value should the Unversal Exponent take? Well, according to theory, the largest possible data result from an FFT is N times the largest input data. This means that the binary point can move a maximum of log2(N) places to the right. Hence, if we choose the Unverisal Exponent to be log2(N) this should give us sufficient range to represent all data points faithfully.

In practice, data output may never approach the theoretical maximum. Hence, it may be worthwhile to try various Unverisal Exponents and choose the one best suited to the particular application.

Data is output from the butterfly processor with a two-part exponent: the 5-bit GWR applicable to all data words from a given FFT and a 2-bit WTOUT associated with each individual data word. To find the complete exponent for a given word, the GWR for that FFT must be modified by its WTOUT as shown in Table 6. The result is the number of places the binary point has shifted to the right during the course of the FFT.

This value must be compared with the Unversial Exponent to determine the shift required. This is done by subtracting it from the Unversial Exponent. The number of places to be shifted is equal to the difference between the two exponents. The shift can be implemented in a PDSP1601/A. The shift value is fed into the SV port.

As FFT data consists of real and imaginary parts, either two PDSP1601As must be used (controlled by the same logic) or a single PDSP1601/A could be used handling real and imaginary data on alternate cycles (using the same instructions for both cycles).

An example of an output normalisation circuit is shown in Fig.8. Only 4 bit data paths are used in calculating the shift. This means that we must be able to trap very small values negative of GWR and force a 15 bit right shift in such cases.

N.B.

It is easier to simply add the word tag to the exponent for the purpose of determing the shift required, instead of modifying it according to Table.6. To compensate for this, the Universal Exponent may be increased by one.

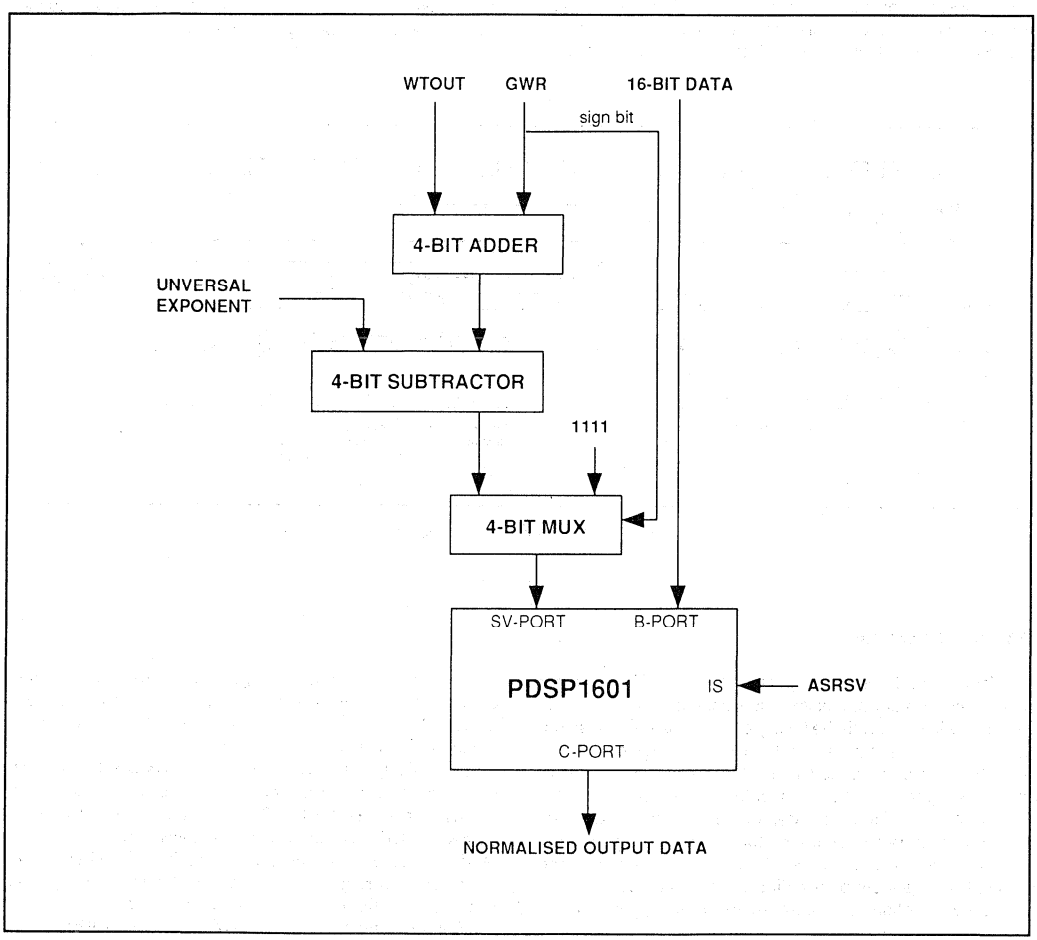


Fig.8 Output Normalisation Circuitry

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage V_{CC}	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to V_{CC} +0.5V
Output voltage V_{OUT}	-0.5V to V_{CC} +0.5V
Clamp diode current per I_K (see note 2)	18mA
Static discharge voltage (HBM)	500V
Storage temperature range T_S	-65°C to +150°C
Ambient temperature with power applied T_{AMB}	
Military	-55°C to +125°C
Industrial	-40°C to +85°C
Junction temperature	150°C
Package power dissipation	1000mW
Thermal resistances	
Junction to case θ_{JC}	12°C/W
Junction to case θ_{JA}	29°C/W

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceedeed, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Operating conditions (unless otherwise stated):
Industrial: T_{AMB} = -40°C to +85°C, V_{CC} = 5.0V ± 10%, GND = 0V
Military: T_{AMB} = -55°C to +125°C, V_{CC} = 5.0V ± 10%, GND = 0V

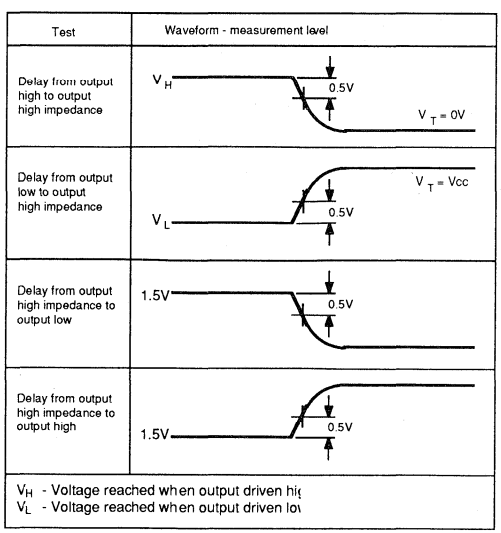
Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Min.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 8mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -8mA
Input high voltage	V_{IH}	3.0		-	V	CLK input only
Input high voltage	V_{IH}	2.2		-	V	All other inputs
Input low voltage	V_{IL}	-		0.8	V	GND <V_{IN}<V_{CC}
Input leakage current	I_{IN}	-10		+10	µA	
Input capacitance	C_{IN}		10		pF	GND <V_{IN}<V_{CC}
Output leakage current	I_{OZ}	-50		+50	µA	V_{CC} = Max
Output S/C current	I_{OS}	10		300	mA	

Switching Characteristics

Characteristic	PDSP16116		PDSP16116A		Units	Conditions
	Min.	Max.	Min.	Max.		
CLK rising edge to P-PORTS	5	45	5	23	ns	2 x LSTTL + 20pF
CLK rising edge to WTOUT1:0	5	30	5	20	ns	2 x LSTTL + 20pF
CLK rising edge to GWR4:0	5	30	5	20	ns	2 x LSTTL + 20pF
CLK rising edge to SFTA1:0	5	60	5	30	ns	2 x LSTTL + 20pF
CLK rising edge to SFTR2:0	5	50	5	28	ns	2 x LSTTL + 20pF
Setup CEX or CEY to CLK rising edge	11	-	8	-	ns	
Hold CEX or CEY to CLK rising edge	-	0	-	0	ns	
Setup X or Y port inputs to CLK rising edge	11	-	8	-	ns	
Hold X or Y port inputs to CLK rising edge	-	2	-	0	ns	
Setup WTA1:0, WTB1:0, SOBFP or EOPSS inputs to CLK rising edge	14	-	8	-	ns	
Hold WTA1:0, WTB1:0, SOBFP or EOPSS inputs to CLK rising edge	-	0	-	0	ns	
Setup CONX or CONY inputs to CLK rising edge	14	-	8	-	ns	
Hold CONX or CONY inputs to CLK rising edge	-	0	-	0	ns	
Setup AR15:13 or AI15:13 to CLK rising edge	14	-	-	-	ns	
Hold AR15:13 or AI15:13 to CLK rising edge	-	0	-	0	ns	
OPSEL to valid P-PORTS	-	35	-	20	ns	2 x LSTTL + 20pF
OER or OEI rising PR-PORT or PI-PORT high to Z	-	35	-	25	ns	see Fig.9
OER or OEI rising PR-PORT or PI-PORT low to Z	-	45	-	25	ns	see Fig.9
OER or OEI falling PR-PORT or PI-PORT Z to high	-	22	-	18	ns	see Fig.9
OER or OEI falling PR-PORT or PI-PORT Z to low	-	24	-	18	ns	see Fig.9
Clock period	100	-	50	-	ns	
Clock high time	30	-	12	-	ns	
Clock low time	20	-	12	-	ns	
Vcc Current (CMOS input levels)	-	60	-	80	mA	see Note 4
Vcc Current (TTL input levels)	-	100	-	130	mA	see Note 4

NOTE 4 :- V_{CC} = Max Outputs unloaded, clock freq = Max



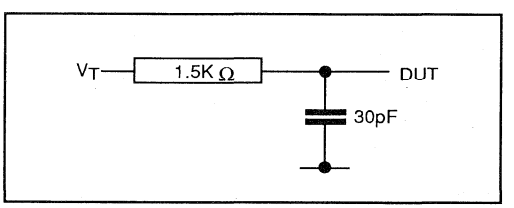


Fig.9 Three state delay measurement load

ORDERING INFORMATION

PDSP16116 MC GGDR	**10MHz**	**MIL-883 screened**
PDSP16116A B0 AC	**20MHz**	**Industrial**
PDSP16116A A0 AC	**20MHz**	**Military**
PDSP16116A B0 GG	**20MHz**	**Industrial**
PDSP16116A A0 GG	**20MHz**	**Military**
PDSP16116A MC GGDR	**20MHz**	**MIL-883 screened**
PDSP16116B B0 AC	**25MHz**	**Industrial**

PDSP16318/PDSP16318A

COMPLEX ACCUMULATOR

(Supersedes version in December 1993 Digital Video & Video Digital Signal Processing IC Handbook, HB3923-1)

The PDSP16318 contains two independent 20-bit Adder/ Subtractors combined with accumulator registers and shift structures. The four port architecture permits full 20MHz throughout in FFT and filter applications.

Two PDSP16318As combined with a single PDSP16112A Complex Multiplier provide a complete arithmetic solution for a Radix 2 DIT FFT Butterfly. A new complex Butterfly result can be generated every 50ns allowing 1K complex FFTs to be executed in 256µs.

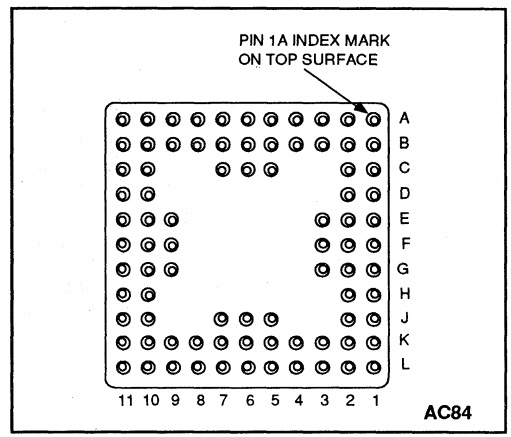


Fig.1 Pin connections - bottom view (AC84 - PGA)

FEATURES

- Full 20MHz Throughout in FFT Applications
- Four Independent 16-bit I/O Ports
- 20-bit Addition or Accumulation
- Fully Compatible with PDSP16112 Complex Multiplier
- On Chip Shift Structures for Result Scaling
- Overflow Detection
- Independent Three-State Outputs and Clock Enables for 2 Port 20MHz Operation
- 1.4 micron CMOS
- 500mW Maximum Power Dissipation
- 84 Pin PGA or QFP packages

APPLICATIONS

- High speed Complex FFT or DFTs
- Complex Finite Impulse Response (FIR) Filtering
- Complex Conjugation
- Complex Correlation/Convolution

ASSOCIATED PRODUCTS

PDSP16112 16 x 12 Complex Multiplier
PDSP16116 16 x 16 Complex Multiplier
PDSP1601 ALU and Barrel Shifter
PDSP16330 Pythagoras Processor

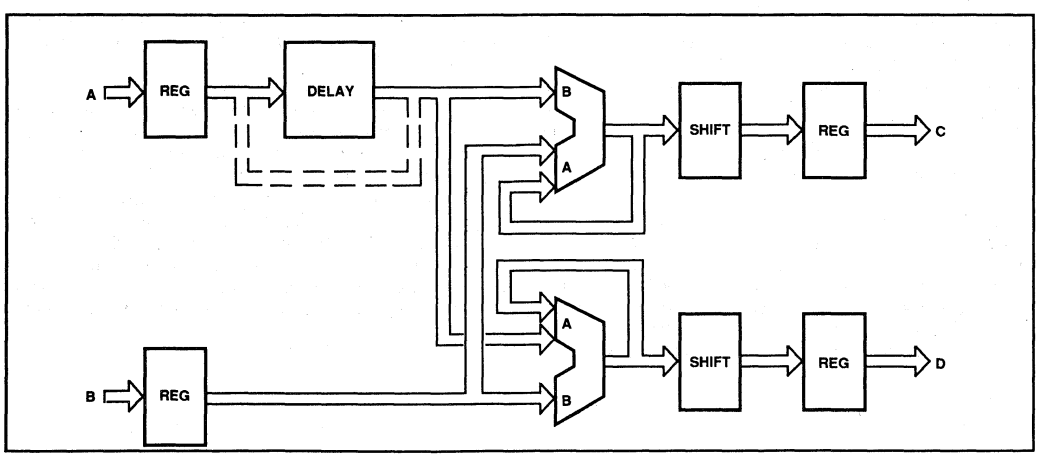


Fig. 2 PDSP16318 simplified block diagram

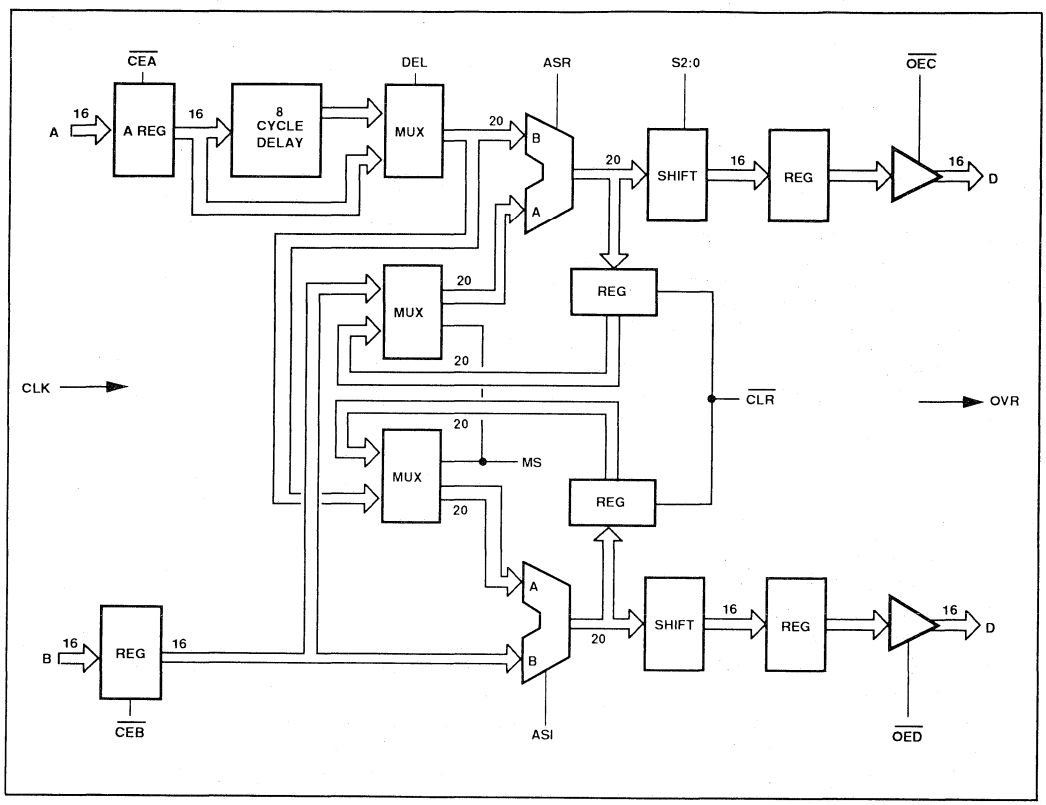


Fig. 3 Block diagram

FUNCTIONAL DESCRIPTION

The PDSP16318 is a Dual 20-bit Adder/Subtractor configured to support Complex Arithmetic. The device may be used with each of the adders allocated to real or imaginary data (e.g. Complex Conjugation), the entire device allocated to Real or Imaginary Data (e.g. Radix 2 Butterflys) or each of the adders configured as accumulators and allocated to real or imaginary data (Complex Filters). Each of these modes ensures that a full 20MHz throughput is maintained through both adders, the first and last mode illustrating true Complex operation, where both real and imaginary data is handled by the single device.

Both Adder/Subtractors may be controlled independently via the ASR and ASI inputs. These controls permit A + B, A - B, B - A or pass A operations, where the A input to the Adder is derived from the input multiplexer. The $\overline{CLR}$ control line allows the clearing of both accumulator registers. The two multiplexers may be controlled via the MS inputs, to select either new input data, or fed-back data from the accumulator registers. The PDSP16318 contains an 8-cycle deskew register selected via the DEL control. This deskew register is used in FFT applications to ensure correct phasing of data that has not passed through the PDSP16112 Complex Multiplier.

The 16-bit outputs from the PDSP16318 are derived from the 20-bit result generated by the Adders. The three bit S2:0 input selects eight different shifted output formats ranging from the most significant 16 bits of the 20-bit data, to the least significant 13 bits of the 20-bit data. In this mode the 14th, 15th and 16th bits of the output are set to zero. The shift selected is applied to both adder outputs, and determines the function of the OVR flag. The OVR flag becomes active when either of the two adders produces a result that has more significant digits than the MSB of the 16-bit output from the device. In this manner all cases when invalid data appears on the output are flagged.

Symbol	Type	Description
A15:0	Input	**Data** presented to this input is loaded into the input register on the rising edge of CLK. A15 is the MSB.
B15:0	Input	**Data** presented to this input is loaded into the input register on the rising edge of CLK. B15 is the MSB and has the same weighting as A15.
C15:0	Output	New **data** appears on this output after the rising edge of CLK. C15 is the MSB.
D15:0	Output	New **data** appears on this output after the rising edge of CLK. C15 is the MSB.
CLK	Input	**Common Clock** to all internal registers
$\overline{CEA}$	Input	**Clock enable:** when low the clock to the A input register is enabled.
$\overline{CEB}$	Input	**Clock enable:** when low the clock to the B input register is enabled.
$\overline{OEC}$	Input	**Output enable:** Asynchronous 3-state output control: The C outputs are in a high impedance state when this input is high.
$\overline{OED}$	Input	**Output enable:** Asynchronous 3-state output control: The D outputs are in a high impedance state when this input is high.
OVR	Output	**Overflow flag:** This flag will go high in any cycle during which either the output data overflows the number range selected or either of the adder results overflow. A new OVR appears after the rising edge of the CLK.
ASR1:0	Input	**Add/subtract Real:** Control input for the 'Real' adder. This input is latched by the rising edge of clock.
ASI1:0	Input	**Add/subtract Imag:** Control input for the 'Imag' adder. This input is latched by the rising edge of clock.
$\overline{CLR}$	Input	**Accumulator Clear:** Common accumulator clear for both Adder/Subtractor units. This input is latched by the rising edge of CLK.
MS	Input	**Mux select:** Control input for both adder multiplexers. This input is latched by the rising edge of CLK. When high the feedback path is selected.
S2:0	Input	**Scaling control:** This input selects the 16-bit field from the 20-bit adder result that is routed to the outputs. This input is latched by the rising edge of CLK.
DEL	Input	**Delay Control:** This input selects the delayed input to the real adder for operations involving the PDSP16112. This input is latched by the rising edge of CLK.
VCC	Power	**+5V supply:** Both Vcc pins must be connected.
GND	Ground	**0V supply:** Both GND pins must be connected.

GG pin	AC pin	Function	GG pin	AC pin	Function	GG pin	AC pin	Function	GG pin	AC pin	Function
77	B2	D7	6	K2	C7	31	K10	A1	56	B10	B10
82	C2	D8	7	K3	C6	32	J10	A2	57	B9	B9
83	B1	D9	8	L2	C5	33	K11	A3	58	A10	B8
84	C1	D10	9	L3	C4	34	J11	A4	59	A9	B7
85	D2	GND	10	K4	C3	35	H10	A5	60	B8	B6
86	D1	VCC	11	L4	C2	36	H11	A6	61	A8	B5
87	E3	D11	12	J5	C1	37	F10	A7	62	B6	B4
88	E2	D12	13	K5	C0	38	G10	A8	63	B7	B3
89	E1	D13	14	L5	$\overline{OED}$	39	G11	A9	64	A7	B2
90	F2	D14	15	K6	$\overline{OEC}$	40	G9	A10	65	C7	B1
91	F3	D15	16	J6	S2	41	F9	A11	66	C6	B0
92	G3	C15	17	J7	S1	42	F11	A12	67	A6	$\overline{CLK}$
93	G1	C14	18	L7	S0	43	E11	A13	68	A5	$\overline{CEB}$
94	G2	C13	19	K7	MS	44	E10	A14	69	B5	OVR
95	F1	C12	20	L6	ASI1	45	E9	A15	70	C5	D0
96	H1	VCC	21	L8	ASI0	46	D11	$\overline{CEA}$	71	A4	D1
97	H2	GND	22	K8	DEL	47	D10	B15	72	B4	D2
98	J1	C11	23	L9	$\overline{CLR}$	48	C11	B14	73	A3	D3
99	K1	C10	24	L10	ASR1	49	B11	B13	74	A2	D4
100	J2	C9	25	K9	ASR0	50	C10	B12	75	B3	D5
5	L1	C8	26	L11	A0	51	A11	B11	76	A1	D6

Device Pinout for ceramic 84 - pin PGA (AC84) and ceramic QFP (GG100)

ASR or ASI ASX1	ASX0	ALU Function
0	0	A + B
0	1	A
1	0	A - B
1	1	B - A

DEL	Delay Mux Control
0	A port input
1	Delayed A port input

MS	Real and Imag' Mux Control
0	B port input/Del mux output
1	C accumulator/D accumualtor

S2:0			Adder result																		
S2	S1	S0	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
0	0	1		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
0	1	0			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0	1	1				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	0	0					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1						15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1	1	0							15	14	13	12	11	10	9	8	7	6	5	4	3	2
1	1	1								15	14	13	12	11	10	9	8	7	6	5	4	3

NOTE

This table shows the portion of the adder result passed to the D15:0 and C15:0 outputs. Where fewer than 16 adder bits are selected the output data is padded with zeros.

ABSOLUTE MAXIMUM RATINGS (Note 1)

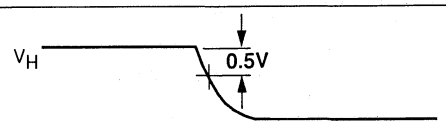
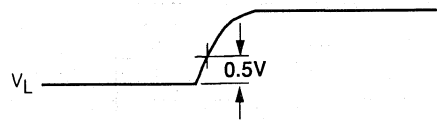
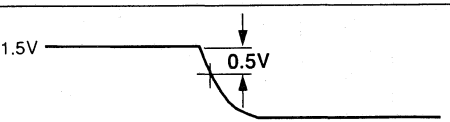
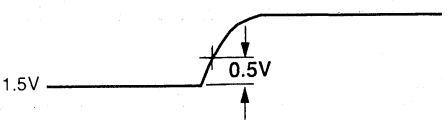
Supply voltage V_{CC}	-0.5V to 7.0V
Input voltage V_{IN}	-0.9V to V_{CC} +0.9V
Output voltage V_{OUT}	-0.9V to V_{CC} +0.9V
Clamp diode current per pin I_K (see Note 2)	18mA
Static discharge voltage (HMB) V_{STAT}	500V
Storage temperature range Ts	-65°C to +150°C
Ambient temperature with power applied T_{amb}	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Junction temperature	150°C
Package power dissipation P_{TOT}	1000mW

NOTES

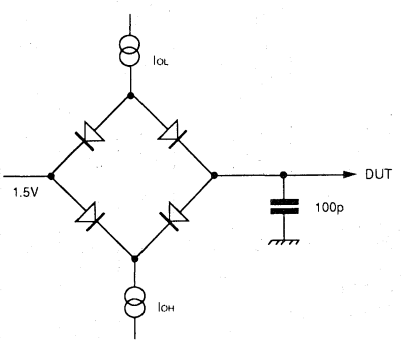
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Package Type	θ_{JC} °C/W	θ_{JA} °C/W
LC	12	35
AC	12	36

Test	Waveform - measurement level
Delay from output high to output high impedance	
Delay from output low to output high impedance	
Delay from output high impedance to Output low	
Delay from output high impedance to Output high	

NOTES
1. V_H - Voltage reached when output driven high
2. V_L - Voltage reached when output driven low



ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} (Commercial) = 0°C to +70°C, V_{CC} = 5.0V ± 5%, GND = 0V

T_{amb} (Industrial) =-40°C to +85°C, V_{CC} = 5.0V ± 10%, GND = 0V

T_{amb} (Military) =-55°C to +125°C, V_{CC} = 5.0V ± 10%, GND = 0V

STATIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 3.2mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL}=-3.2mA
Input high voltage	V_{IH}	3.5		-	V	
Input low voltage	V_{IL}	-		0.5	V	
Input leakage current	I_{IL}	-10		+10	µA	GND ≤ V_{IN}≤V_{CC}
Output leakage current	I_{oz}	-50	-	+50	µA	GND ≤V_{OUT} ≤ V_{CC}
Output SC current	I_{OS}	20	-	200	mA	V_{cc} = Max
Input capacitance	C_{IN}	-	9	-	pF	

SWITCHING CHARACTERISTICS

Characteristic	Value Industrial + Commercial				Value Military		Units	Conditions
	PDSP16318		PDSP16318A		PDSP16318			
	Min.	Max.	Min.	Max.	Min.	Max.		
Clock period	100	-	50	-	100	-	ns	
Clock High Time	20	-	15	-	20	-	ns	
Clock Low Time	20	-	15	-	20	-	ns	
A15:0, B15:0 setup to clock rising edge	8	-	5	-	8	-	ns	
A15:0, B15:0 hold after clock rising edge	2	-	2	-	2	-	ns	
MS, S2:0, ASI setup to clock rising edge	10	-	10	-	10	-	ns	
DEL, ASR, $\overline{CLR}$ setup to clock rising edge	8	-	5	-	8	-	ns	
DEL, ASR, $\overline{CLR}$, MS, S2:0, ASI hold after clock rising edge	2	-	2	-	2	-	ns	
$\overline{CEA}$, $\overline{CEB}$ setup to clock falling edge	2	-	2	-	2	-	ns	
$\overline{CEA}$, $\overline{CEB}$ hold after clock rising edge	8	-	8	-	8	-	ns	
Clock rising edge to OVR, C15:0, D15:0	5	40	5	30	5	40	ns	2 x LSTTL + 20pF
$\overline{OEC}$/$\overline{OED}$ low to C15:0/D15:0 high data valid	-	40	-	30	-	40	ns	2 x LSTTL + 20pF
$\overline{OEC}$/$\overline{OED}$ low to C15:0/D15:0 low data valid	-	40	-	30	-	40	ns	2 x LSTTL + 20pF
$\overline{OEC}$/$\overline{OED}$ high to C15:0/D15:0 high impedance	-	40	-	30	-	40	ns	2 x LSTTL + 20pF
Vcc current	-	70	-	110	-	70	mA	V_{CC} = max, TTL input levels Outputs unloaded, f_{CLK} = max
Vcc current	-	30	-	60	-	30	mA	V_{CC} = max, CMOS input levels Outputs unloaded, f_{CLK} = max

NOTES

1. LSTTL is equivalent to I_{OH} = 20 microamps, I_{OL} = -0.4mA
2. Current is defined as negative into the device
3. CMOS input levels are defined as:
   V_{IL} = 0.5
   V_{IH} = V_{DD} - 0.5

ORDERING INFORMATION

Industrial (-40°C to +85°C)

PDSP16318A/B0/AC	(20MHz	- PGA)
PDSP16318A/B0/GG	(20MHz	- QFP)

Military (-55°C to +125°C)

PDSP16318A/A0/AC	(20MHz	- PGA)
PDSP16318A/MC/GGCR	(20MHz	- QFP MIL883C Screened)

Section 8
Function Specific DSP

GEC PLESSEY
SEMICONDUCTORS

PDSP16256 / A

PROGRAMMABLE FIR FILTER

(Supersedes October 1995 version, DS3709 - 3.0)

The PDSP16256 contains sixteen multiplier - accumulators, which can be multi cycled to provide from 16 to 128 stages of digital filtering. It accepts 16 bit data and coefficients, and accumulates results upto 32 bits.

In 16 tap mode the device samples data at the 25MHz system clock rate. If a lower sample rate is acceptable then the number of stages can be increased in powers of two upto a maximum of 128. Each time the number of stages is doubled, the sample clock rate must be halved with respect to the system clock. With 128 stages the sample clock is therefore one eighth of the system clock.

In all speed modes devices can be cascaded to provide filters of any length, only limited by the possibility of accumulator overflow. The 32 bit results are passed between cascaded devices without any intermediate scaling and subsequent loss of precision.

The device can be configured as either, one long filter, or two separate filters with half the number of taps in each. Both networks can have independent inputs and outputs.

Both single and cascaded devices can be operated in decimate by two mode. The output rate is then half the input rate, but twice the number of stages are possible at a given sample rate. A single device with a 20MHz clock would then, for example, provide a 128 stage low pass filter, with a 5MHz input rate and 2.5MHz output rate.

Coefficients are stored internally and can be down loaded from a host system or an EPROM. The latter requires no additional support, and is used in stand alone applications. A full set of coefficients is then automatically loaded at power on, or at the request of the system. A single EPROM can be used to provide coefficients for upto 16 devices.

FEATURES

- Sixteen MACs in a single device
- Basic mode is 16 tap filter with 25MHz sample rates
- 16 bit data and 32 bit accumulators
- Programmable to give up to 128 taps with sampling rates proportionally reducing to 3.13MHz
- Can be configured as one long filter or two half length filters
- Decimate by two option will double the filter length
- Coefficients supplied from a host system or a local EPROM
- Advanced 144 PGA package with integral ground and supply planes

APPLICATIONS

- High Performance Digital Filters
- Pulse Compression for Radar & Sonar
- Matrix Multiplication
- Correlation

ASSOCIATED PRODUCTS

PDSP16350 I/Q Splitter / NCO

PDSP16510 FFT Processor

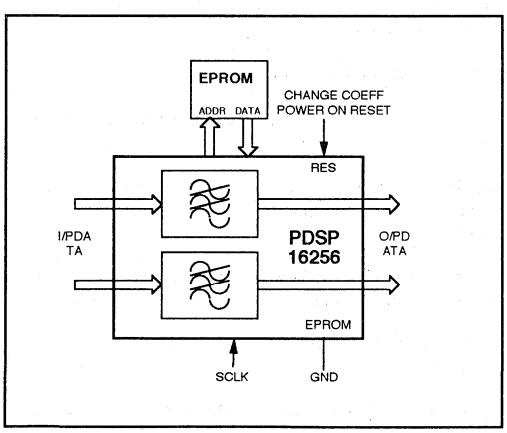


Fig. 1 Dual Filter

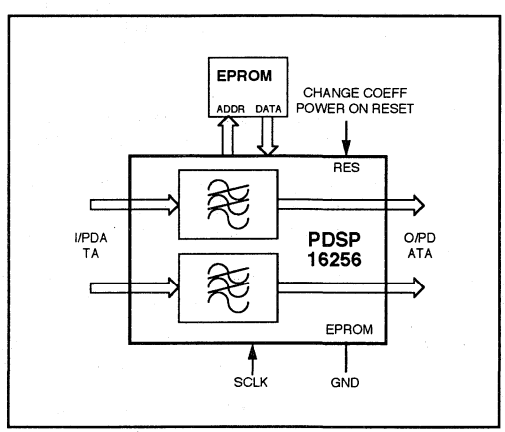


Fig. 2 Typical System Application

SIGNAL	DESCRIPTION
DA15:0	16 bit data input bus to Network A.
DB15:0	Delayed data output bus in the single filter mode. Connected to the data input bus of the next device in a cascaded chain. Input to Network B in the dual filter modes.
X31:0	Expansion input bus in the single filter mode. Connected to the previous filter output in a cascaded chain. The inputs are not used on a single device system or on the Termination device in a cascaded chain. The output from Network B in the dual modes.
F31:0	In single filter mode this bus holds the main device output. In dual mode it holds the output from Network A.
FEN	Filter enable. The first high present on an SCLK rising edge defines the first data sample. The signal must stay active whilst valid data is being received.
DFEN	Delayed filter enable. This output is connected to the Filter Enable input of the next device in a cascaded chain, when moving towards the termination device. It is used to coordinate the control logic within each device.
SWAP	Selects either the upper or lower set of coefficients for Bank Swap. A low selects the lower bank, a high the upper bank.
FRUN	When high this signal allows continuous filter operations to occur without the need for the initial FEN edge. If the device is not a single or interface device then this pin must be tied low.
$\overline{\text{DCLR}}$	A low on this signal on the SCLK rising edge will clear all the internal accumulators. DCLR need only remain low for a single cycle, signal BUSY will indicate when the internal clearing is complete. After a clear the device must be re-synchronised to the data stream using FEN. It is recommended the FEN is taken low at the same time as clear. FEN may then be taken high to synchronise the data stream once BUSY has returned low.
C15:0	16 bit coefficient input bus. In the Byte mode of operation, C15:8 have alternative uses as explained in the text.
A7:0	Coefficient address bus. In the EPROM mode A7:0 are address outputs for an EPROM. In the remote host mode they are inputs from the host. A7 is not used when coefficients are loaded as 16 bit words.
CCS	This pin is similar in operation to A7:0 and provides a higher order address bit. When low the coefficients are loaded, when high the control register is loaded.
$\overline{\text{WEN}}$	In the remote mode this pin is an input which when low enables the load operation. In the EPROM mode it is an output which provides the write enable for other slave devices.
$\overline{\text{CS}}$	This pin is always an input and must also be low for the internal write operation to occur.
$\overline{\text{BYTE}}$	When this pin is tied low, coefficients are loaded as two bytes. When the pin is high they are loaded as 16 bit words. In the EPROM mode this pin is ignored.
$\overline{\text{EPROM}}$	When this pin is tied low coefficients are loaded as bytes from an external EPROM. The device outputs an address on A7:0. When the pin is high coefficients must be loaded from a remote master. They can then be transferred individually rather than as a complete set.
SCLK	The main system clock, all operations are synchronous with this clock. The clock rate must be either 1, 2, 4, or 8 times the required data sampling rate. The factor used depends on the required filter length.
CLKOP	This output when used to enable SCLK can provide a data sampling clock. It has the effect of dividing the SCLK rate by 1, 2, 4 or 8 depending on the filter mode selected.
$\overline{\text{OEN}}$	Tri-state enable for the F bus. When high the outputs will be high impedance. OEN is registered onto the device and does not therefore take effect until the first SCLK rising edge

SIGNAL	DESCRIPTION
BUSY	A high on this signal indicates that the device is completing internal operations and is not yet able to accept new data. The signal is used during automatic EPROM loading, reset and accumulator clearing.
$\overline{RES}$	When this pin is low the control logic and accumulators are reset. In the EPROM mode it will initiate a load sequence when it goes high.

NOTE unused busses (e.g. X31:0 when the device is configured in single or termination mode) can be set to any value. They should however be maintained at a valid logic level to avoid an increase in power consumption.

To ensure correct input voltage thresholds are maintained all the VDD and GND pins must be connected to adequate power and ground planes.

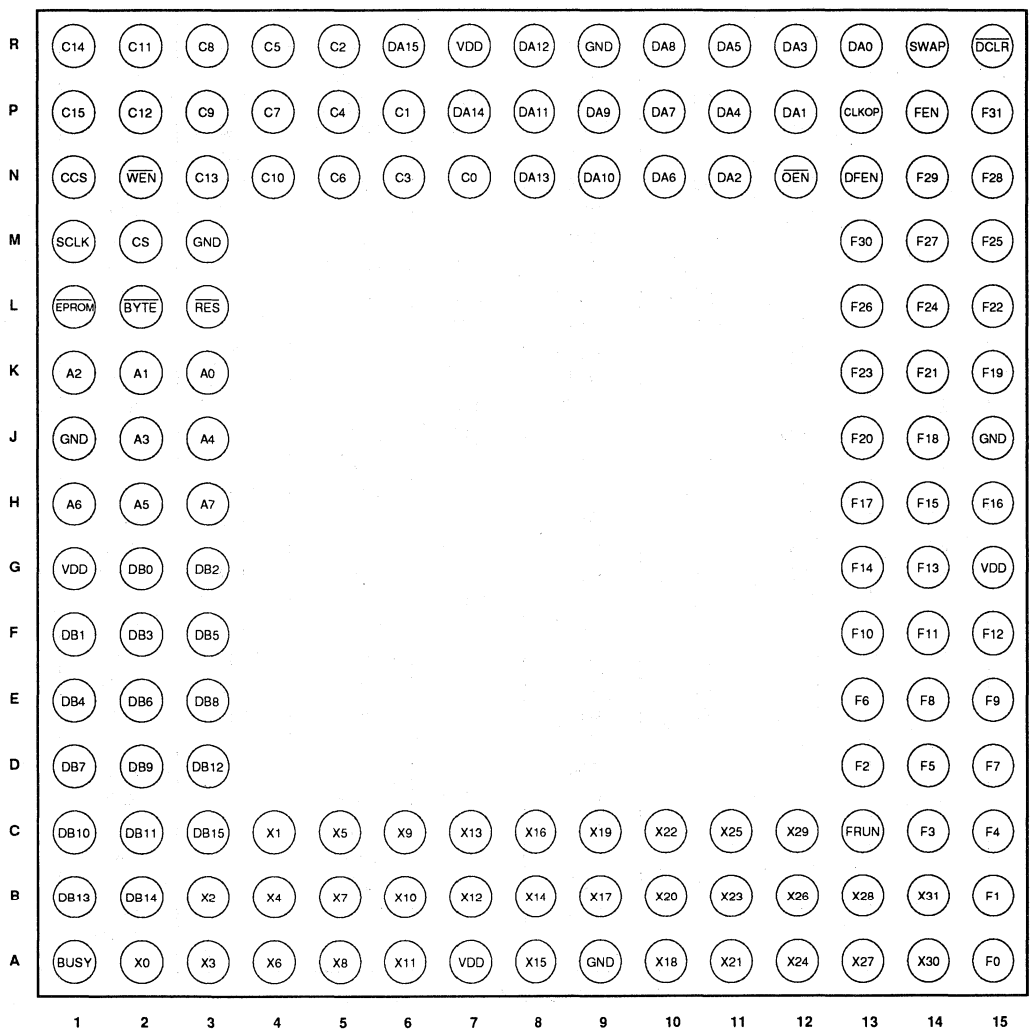


Fig. 3A Device Pinout - Bottom view (144 pin PGA - AC144)

GC	SIG	GC	SIG	GC	SIG	GC	SIG
1	F0	44	SWAP	87	C15	130	GND
2	F1	45	GND	88	GND	131	BUSY
3	F2	46	OEN	89	GND	132	X0
4	F3	47	CLKOP	90	WEN	133	VDD
5	VDD	48	VDD	91	CCS	134	X1
6	F4	49	DA0	92	CS	135	X2
7	F5	50	DA1	93	VDD	136	X3
8	GND	51	DA2	94	RES	137	X4
9	F6	52	DA3	95	SCLK	138	X5
10	F7	53	DA4	96	GND	139	X6
11	F8	54	DA5	97	VDD	140	GND
12	F9	55	GND	98	BYTE	141	X7
13	F10	56	DA6	99	EPROM	142	X8
14	F11	57	DA7	100	A0	143	VDD
15	F12	58	DA8	101	A1	144	X9
16	GND	59	DA9	102	A2	145	X10
17	F13	60	VDD	103	A3	146	X11
18	F14	61	DA10	104	A4	147	X12
19	F15	62	DA11	105	VDD	148	X13
20	VDD	63	DA12	106	A5	149	X14
21	F16	64	DA13	107	A6	150	GND
22	F17	65	DA14	108	GND	151	X15
23	F18	66	DA15	109	A7	152	X16
24	F19	67	GND	110	DB0	153	X17
25	VDD	68	C0	111	DB1	154	X18
26	F20	69	C1	112	DB2	155	X19
27	F21	70	C2	113	GND	156	X20
28	GND	71	C3	114	DB3	157	X21
29	F22	72	C4	115	DB4	158	X22
30	F23	73	C5	116	DB5	159	GND
31	F24	74	VDD	117	DB6	160	X23
32	F25	75	C6	118	DB7	161	X24
33	F26	76	C7	119	VDD	162	X25
34	F27	77	C8	120	DB8	163	VDD
35	F28	78	C9	121	DB9	164	X26
36	GND	79	C10	122	DB10	165	X27
37	F29	80	GND	123	DB11	166	X28
38	F30	81	C11	124	DB12	167	X29
39	F31	82	C12	125	DB13	168	X30
40	VDD	83	C13	126	DB14	169	GND
41	FEN	84	VDD	127	GND	170	X31
42	DFEN	85	GND	128	DB15	171	VDD
43	DCLR	86	C14	129	VDD	172	FRUN

Fig. 3B Device Pinout (172 pin QFP - GC172)

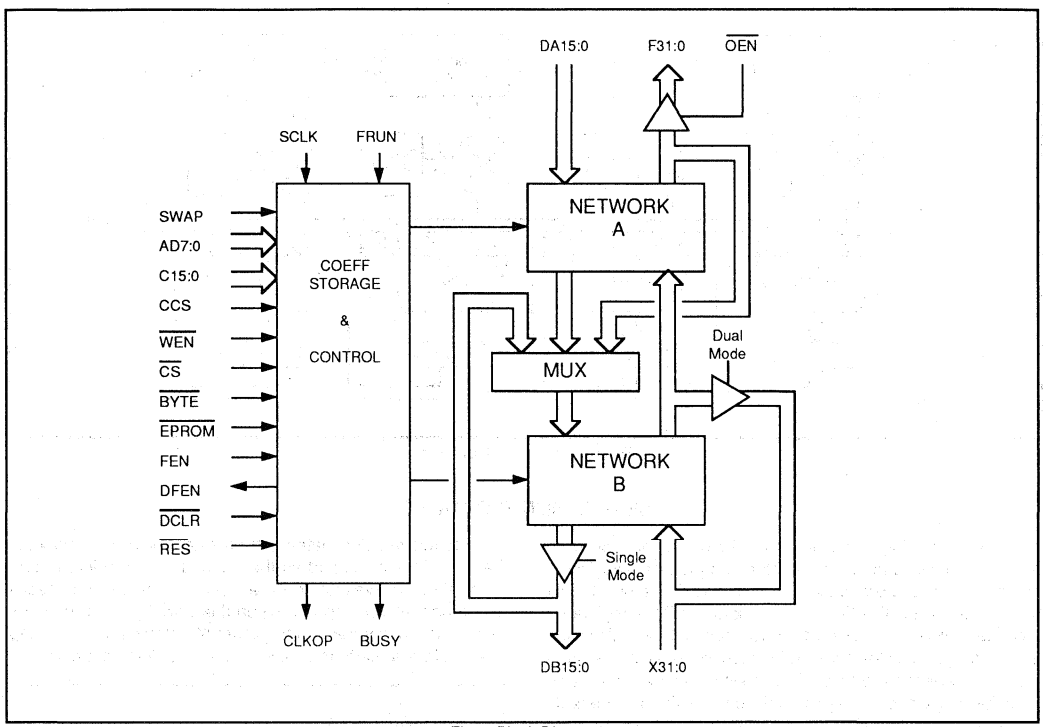


Fig. 4 Block Diagram

OPERATIONAL OVERVIEW

The PDSP16256 is an application specific FIR filter for use in high performance digital signal processing systems. Sampling rates can be upto 25MHz The device provides the filter function without any software development, and the options are simply selected by loading a control register. The device can be user configured as either a single filter, or as two separate filters. The latter can provide two independent filters for the in-phase and quadrature channels after IQ splitting, or can provide two filters in cascade for greater stop band rejection.

The device operates from a system clock, with rates up to 25MHz. This clock must be 1, 2, 4, or 8 times the required sampling frequency, with the higher multiplication rates producing longer filter networks at the expense of lower sampling rates. Devices can be connected in cascade to produce longer filter lengths. This can be accomplished without the need for any additional external data delays, and all the single device options remain available.

Continuous inputs are accepted, and continuous results produced after the internal pipeline delay. Connection can be made directly to an A/D converter. The filter operation can be synchronised to a Filter Enable signal whose active going edge marks the first data sample. The internal multiplier - accumulator array can be cleared with a dedicated input. This is necessary if erroneous results obtained during the normal data 'flush through' are not permissible.

Coefficients can be loaded from a host system using a conventional peripheral interface and separate data bus. Alternatively, they can be loaded as a complete set from a byte wide EPROM. The device produces addresses for the EPROM and a BUSY output indicates that the transfer is occurring. Up to sixteen devices can have their coefficients supplied from a single EPROM. These devices need not necessarily be part of the same filter network.

Each of the filter networks shown in Fig. 4 contains eight systolic multiplier accumulator stages, an example with four stages is shown in Fig. 5. Input data flows through the delay lines and is presented for multiplication with the required coefficient. This is added to either the last result from this accumulator or the result from the previous accumulator. The filter results progress along the adders at the data sample rate. If the sample rate equals SCLK divided by four, for example, then the accumulated result is passed onto the next stage every forth cycle. The structure described is highly efficient when used to calculate filtered results from continuous input data.

A comprehensive digital filter design program is available for PC compatible machines. This will optimise the filter coefficients for the filter type required and number of taps available at the selected sample rate within the PDSP16256 device. An EPROM file can be automatically generated in Motorola S-record format.

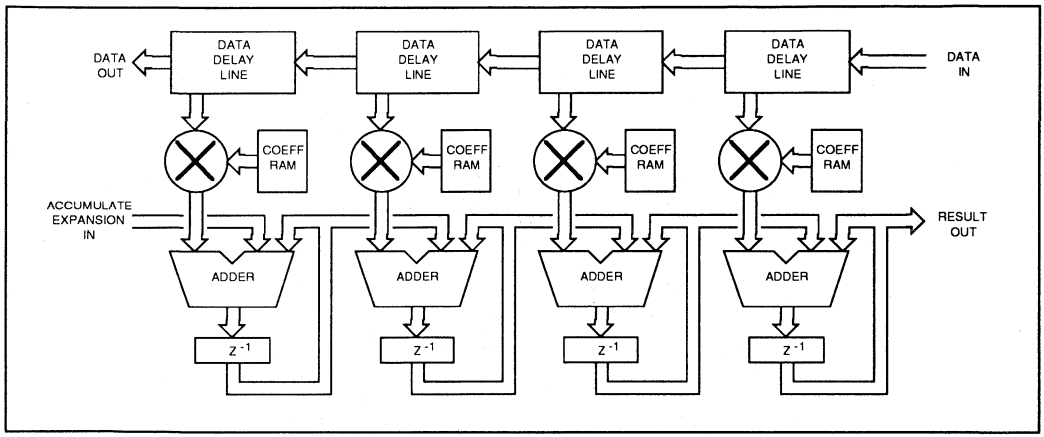


Fig. 5 Filter Network Diagram

SINGLE FILTER OPTIONS

When operating as a single filter the device accepts data on the 16 bit DA bus at the selected sample rate, see Figs 6 and 7. Results are presented on the 32 bit F bus, which may be tristated using the OEN input. Signal OEN is registered onto the device and does not therefore take effect until the first SCLK rising edge. Devices may be cascaded this allows filters with more taps than available from a single device. To accomplish this two further busses are utilised. The DB bus presents the input data to the next device in cascade after the appropriate delay, while, partial results are accepted on the X bus.

Single filter mode is selected by setting control register bit 15 to a one. The required filter length is then selected using control register bits 14 and 13 as summarised in Table 3. The options define the number of times each multiplier - accumulator is used per sample clock period. This can be once, twice, four times, or eight times.

In addition a normal/decimate bit (CR12) allows the filter length to be doubled at any sample rate. This is possible when the filter coefficients are selected to produce a low pass filter, since the filtered output would then not contain the higher frequency components present in the input. The Nyquist criterion, specifying that the sampling rate must be at least double the highest frequency component, can still then be satisfied even though the sampling rate has been halved.

CR 14	CR 13	CR 12	Input Rate	Output Rate	Filter Length	Setup Latency
0	0	0	SCLK	SCLK	16 Taps	16
0	0	1	SCLK	SCLK/2	32 Taps	17
0	1	0	SCLK/2	SCLK/2	32 Taps	16
0	1	1	SCLK/2	SCLK/4	64 Taps	18
1	0	0	SCLK/4	SCLK/4	64 Taps	20
1	0	1	SCLK/4	SCLK/8	128 Taps	24
1	1	0	SCLK/8	SCLK/8	128 Taps	24

Table 3. Single Filter Options

The system clock latency for a single device is shown in Table 3. This is defined as the delay from a particular data sample being available on the input pins to the first result including that input appearing on the output pins. It does not include the delay needed to gather N samples, for an N tap filter, before a mathematically correct result is obtained.

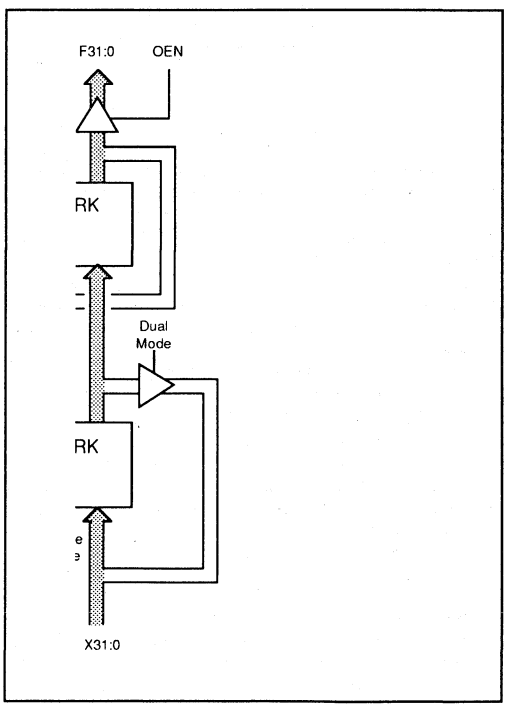
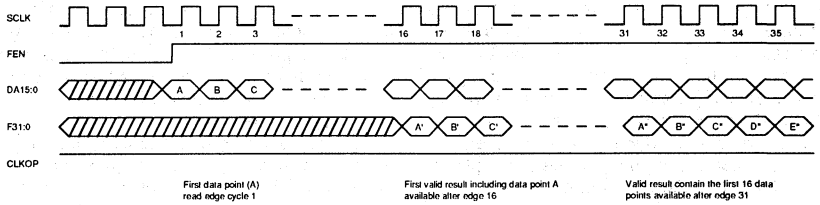
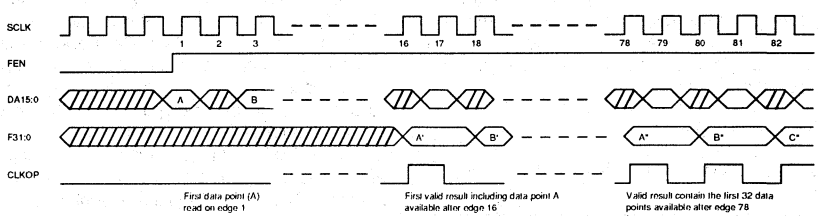


Fig. 6 Single Filter Bus Utilisation

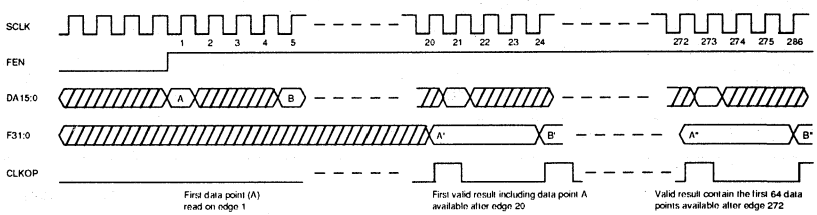
SPEED MODE 0 (Data input and output at the full SCLK rate) CR14:13 = 00, CR12 = 0



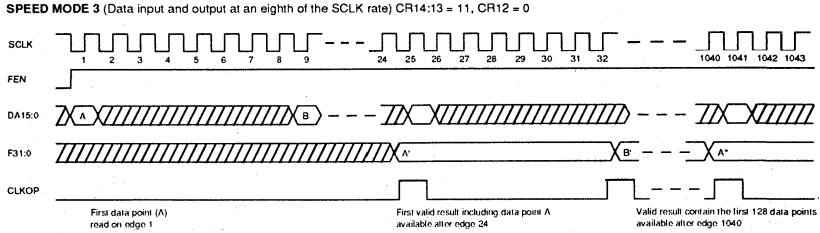
SPEED MODE 1 (Data input and output at half the SCLK rate) CR14:13 = 01, CR12 = 0



SPEED MODE 2 (Data input and output at a quarter of the SCLK rate) CR14:13 = 10, CR12 = 0



SPEED MODE 3 (Data input and output at an eighth of the SCLK rate) CR14:13 = 11, CR12 = 0



SPEED MODE 1 Decimating (Data input at half the SCLK rate and output at a quater of the SCLK rate) CR14:13 = 01, CR12 = 1

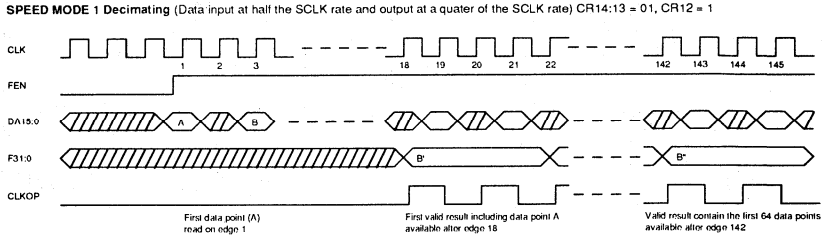


Fig. 7 Single Filter Timing Diagrams

DUAL INDEPENDENT FILTER OPTIONS

When operating as two independent filters the device accepts 16 bit data on both the DA and DB buses at the selected sample rate, see Fig. 8. Results are available from both the F and X buses. The F bus may be tristated using the OEN input. Signal OEN is registered onto the device and does not therefore take effect until the first SCLK rising edge

Each filter must be configured in the same manner, and multiple device expansion is not possible due to the pin reorganization. The latter requirement can, of course, still be satisfied by several devices configured as single filters.

Dual independent filter mode is selected by setting control register bits 15 and 4 to a zero. The required filter length is selected using control register bits 14 and 13 as summarised in Table 4, which also shows the resulting latency. As in single filter mode normal or decimate by two operation can be selected using control register bit 12.

CR 14 13 12	Input Rate	Output Rate	Filter Length	Setup Latency	
				Ind	Cas
0 0 0	SCLK	SCLK	8 Taps	16	27
0 0 1	SCLK	SCLK/2	16 Taps	17	-
0 1 0	SCLK/2	SCLK/2	16 Taps	16	28
0 1 1	SCLK/2	SCLK/4	32 Taps	18	-
1 0 0	SCLK/4	SCLK/4	32 Taps	20	36
1 0 1	SCLK/4	SCLK/8	64 Taps	24	-
1 1 0	SCLK/8	SCLK/8	64 Taps	24	40

Table 4. Dual Filter Options

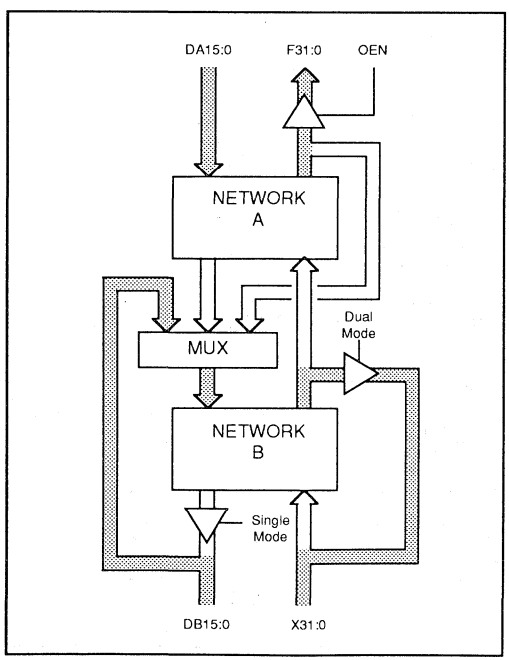


Fig. 8 Dual Independent Filter Bus Utilisation

DUAL CASCADED FILTER OPTIONS

When operating as two cascaded filters the device accepts 16 bit data on the DA bus at the selected sample rate. Results are presented on the 32 bit X bus, see Fig. 9. Each filter must be configured in the same manner. Multiple device expansion is not possible in this mode.

Dual cascaded filter mode is selected by setting control register bit 15 to a zero and bit 4 to a one. The required filter length is selected using control register bits 14 and 13 as summarised in Table 4, which also shows the resulting latency. The decimate by two option is not available in this mode.

The data for the second filter network is extracted as the middle 16 bits from the first networks accumulated result. For successful operation the first filter network must have unity gain. See the section on filter accuracy for more details.

The cascade option is used to increase the stop band rejection in a practical filter application. Theoretically, increasing the number of taps in an FIR filter will increase the stop band rejection, but this assumes floating point calculations with no accuracy limitations. In practice, with fixed point arithmetic, better performance is achieved with two smaller filters in series.

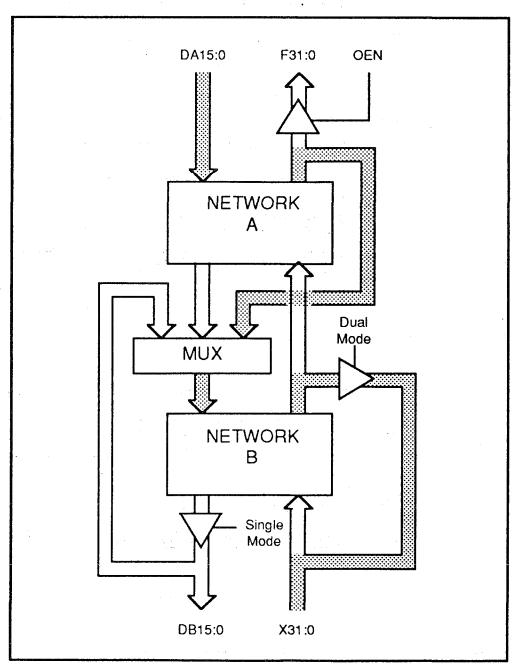


Fig. 9 Dual Cascaded Filter Bus Utilisation

FILTER ACCURACY

Input data and coefficients are both represented by 16bit two's complement numbers. The coefficients are converted to twelve bits by rounding towards zero. This is achieved as follows. If the coefficient is positive then the least significant 4 bits are discarded. If the coefficient is negative then the logical 'OR' of the least significant 4 bits are added to the remainder of the word. Twelve bit coefficients can be used directly provided the least significant four bits are set to zero.

The FIR filter results are calculated using a multiplier accumulator structure as shown in Fig. 10. The truncation and word growth allowed for in the data path are explained in Fig. 11. The 16 bit data and 12 bit coefficient inputs, (each with one sign bit before the binary point), are presented to the multiplier. This produces a 28 bit result with two bits before the binary point. Producing the full 28 bit result ensures that if both the data and coefficients are set to -1 a valid result is generated. Prior to entering the accumulator the least significant 4 bits of the multiplier result are truncated and the resulting 24 bits sign extended to 32 bits. The final accumulator result is 32 bits with 10 bits before the binary point. Thus 9 bits of word growth are allowed within the accumulator. All accumulator bits are made available on the output pins.

In cascade mode the middle 16 bits from the network A accumulator are fed round to the network B data inputs, see Fig. 11.

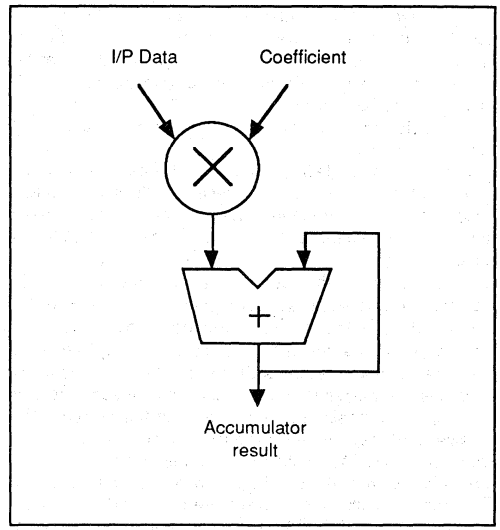


Fig. 10 Multiplier Accumulator

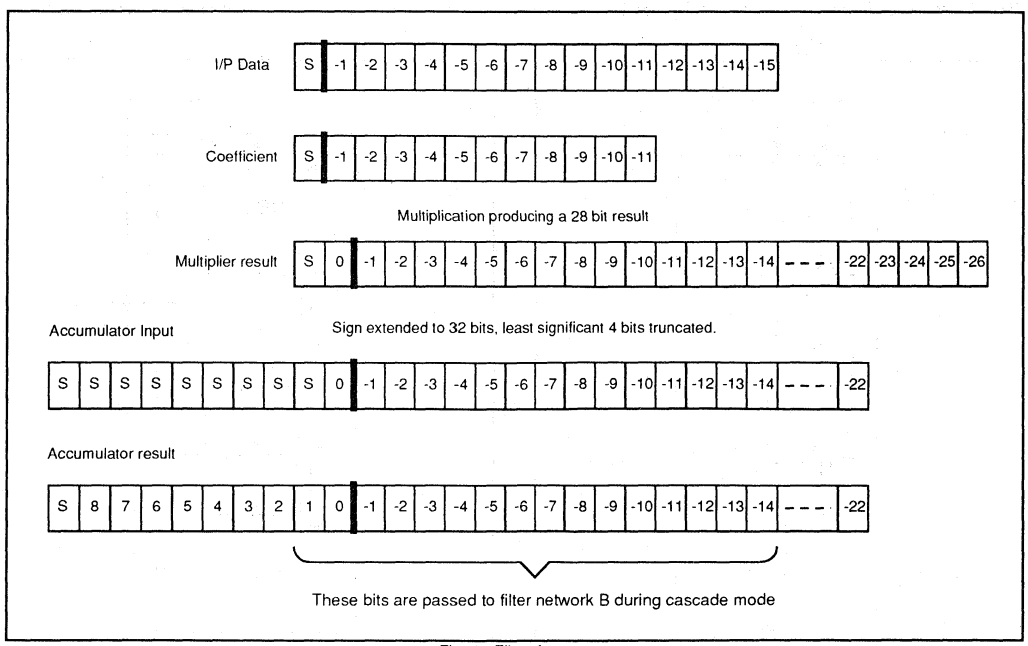


Fig. 11 Filter Accuracy

CASCADING DEVICES

When the filter requirements are beyond the capabilities of a single device, it is possible to connect several devices in cascade increasing the number of taps available at the required sample rate. Within each device all filter length, decimate, and bank swap options are still possible, but each device in the chain must be similarly programmed and configured as a single filter.

The number of devices which can be cascaded is only limited by the possibility of overflow in the 32 bit intermediate accumulations. If more than sixteen devices are cascaded in auto EPROM load mode, then an additional EPROM will be needed.

In modes where the data sample rate does not equal the clock rate. Then the cascade arrangement shown in Fig. 12 is utilised. Delayed data is passed from device to device in one direction, while intermediate results flow in the opposite direction. The interface device both accepts the input data and produces the final result. It is not necessary for each device to know its exact position in the chain, but the device which receives the input data and produces the final result must be identified, as must the device which terminates the chain. The former is known as the Interface device and the latter as the Termination device, all others are Intermediate devices. Control Register bits CR11:10 are used to define these positions as shown in Table 6.

The control logic in each of the devices must be synchronised with respect to the Interface device. This is achieved by connecting the Delayed Filter Enable output (DFEN) to the Filter Enable input (FEN) of the next device in the chain. The Interface device, itself, needs a Filter Enable signal produced by the system, unless the Free Run pin is pulled high. Even when the latter is true, the Filter Enable connection must be made between the remaining devices in the chain.

When devices are cascaded such that the data sample rate equals the clock rate, (Control register bits 14:13 = 00), then a different cascade configuration must be used. This is shown in Fig. 13. The number of devices which can be cascaded is, again, only limited by the 32 bit accumulators.

In this mode the delayed data is passed from device to device in the same direction as the intermediate results. The device which accepts the input data is now at the opposite end of the chain to the device which produces the final result. The control logic in each of the devices must be synchronised this is achieved by connecting all the device FEN inputs to the global Filter enable.

AVAILABLE OPTIONS

No more than 128 coefficients can be stored internally. This limits the filter length / decimate / bank swap options to those which do not require more than that number of coefficients. Thus when a filter with 128 taps is to be implemented in a single device, it is not possible to decimate or bank swap. When a filter with 64 taps is implemented, decimate or bank swap are possible, but not both. With all other filter lengths, all decimate and bank swap configurations are possible.

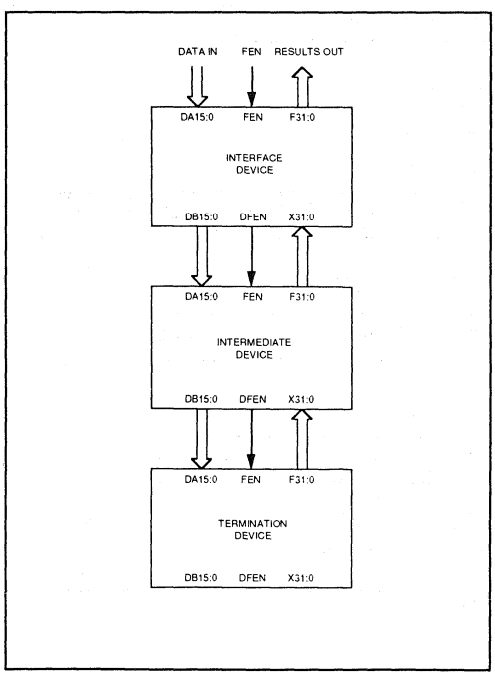


Fig. 12 Three Device Cascaded System

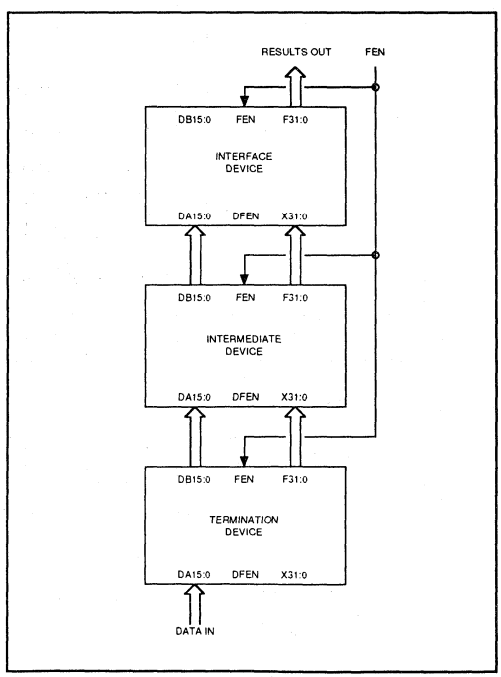


Fig. 13 Full Speed Cascaded System

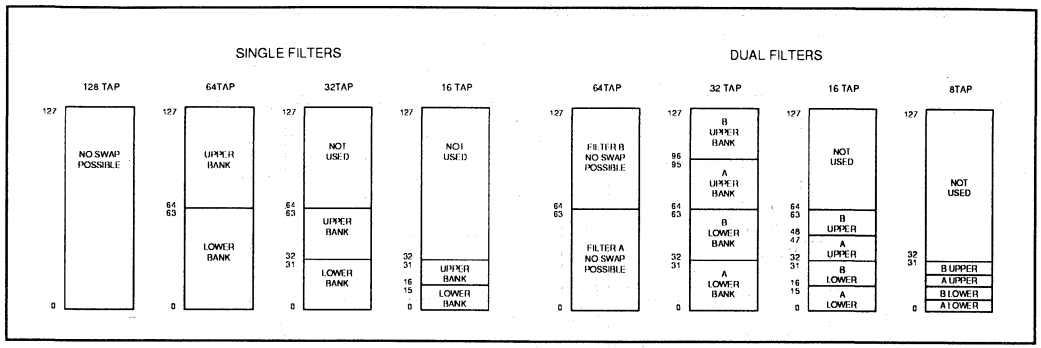


Fig. 14 Coefficient Memory Map

FILTER CONTROL

Two control modes are available selected by input signal FRUN. When FRUN is tied high the device will commence operation once the coefficients have been loaded. The CLKOP signal indicating when new input data is required and that new results are available, see Fig. 7. When FRUN is tied low filter operation will not commence until a high has been detected on signal FEN. This mode allows synchronisation to an existing data stream. Signal FEN should be taken high when the first valid data sample is available so that both are read into the device on the next SCLK rising edge.

During device reset the RES signal must be held low for a minimum of 16 SCLK cycles. After a reset the control register returns to it's default state of 8C80 Hex. This places the device into the following mode :-

- Single filter
- Sample rate equal to the clock rate
- Non-decimating
- A single device (Not in a cascade chain)
- Bank swap selected by bit in the control register

COEFFICIENT BANK SWAP

A Bank Swap feature is provided which allows ALL coefficients to be simultaneously replaced with a different set. A bit in the Control Register (CR7) allows the swap to be controlled by either input signal SWAP or Control Register bit (CR6). The latter is useful if the device is controlled by a microprocessor, when driving a separate pin would entail additional address decoding logic and an external latch.

If the pin or control register bit is low, the coefficients used will be those loaded into the lower banks illustrated in Fig. 14. When the pin or bit is high, the upper banks are used.

The actual swap will occur when the next sampling clock active going transition occurs. This can be up to seven system clocks later than the swap transition, and is filter length dependent. The first valid filtered output will then occur after the pipeline latancies given in Tables 3 and 4.

By setting a bit in the Control Register it is possible to bank swap on every data sampling clock. This function does not depend on the status of the SWAP pin or bit, and the lower bank will be initially selected after FEN goes active. The option can be used to implement filters with complex coefficients.

LOADING COEFFICIENTS

When the device is to operate in a stand alone application then the coefficients can be down loaded as a complete set from a previously programmed EPROM. Alternatively if the system contains a microprocessor they can be individually transferred from a remote master under software control. In any mode the system clock must be present and stable during the transfer, and the addressing scheme is such that the least significant address specifies the coefficient applied to the first multiplier seen by incoming data.

The addresses used during the load operation are those illustrated in Fig. 14. The Control Register is loaded when CCS is high. In BYTE mode address A0 is used to select the portion of control register loaded, otherwise the address bits are redundant. When an EPROM is used to provide coefficients, this redundancy causes the number of locations needed for any device to be double that for the coefficients alone.

AUTO EPROM LOAD

When the EPROM pin is tied low, the PDSP16256 assumes the role of a master device in the system and controls the loading of coefficients from an external EPROM, see Fig.15. A load sequence commences when the RESET input goes inactive, and will continue until every coefficient has been loaded. The BUSY pin goes high to indicate that a load sequence is occurring and the filter output is invalid. The device will not commence a filter operation until the Filter Enable edge is received (FEN) after BUSY has gone low. This requirement can be avoided if the Free Run pin (FRUN) is tied high.

The address bus pins become outputs on the Master device, and produce a new address every four system clock periods. This four clock interval, minus output delays and the data set up time, defines the available EPROM access time.

The coefficients are always loaded as bytes. The state of the BYTE pin on the master device is ignored. This arrangement also allows the eight, most significant, coefficient bus pins (C15:8) to be used for other purposes as described later. Since the 16 bit coefficients are loaded in two bytes the A0 pin specifies the required byte. The maximum number of stored coefficients is 128, eight address outputs are therefore provided for the EPROM. These eight outputs from the Master

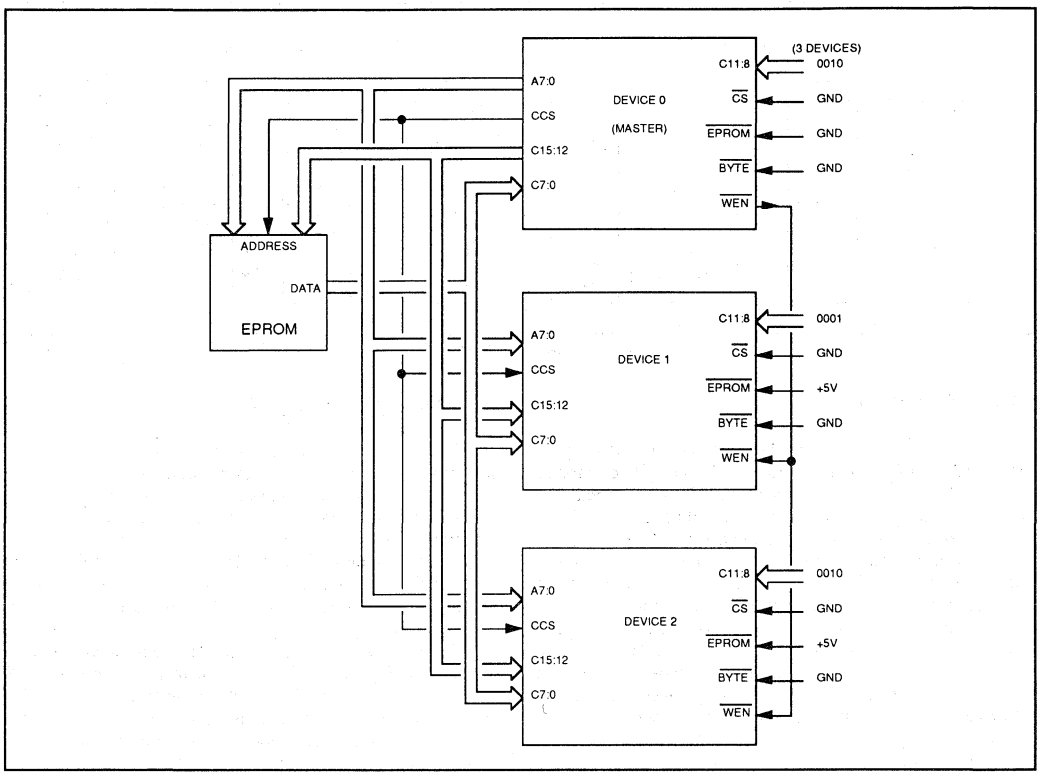


Fig. 15 Three device auto EPROM load

must also drive the address inputs on the slave devices.

When the filter length is less than the maximum, the PDSP16256 will only transfer the correct number of coefficients, and one or more significant address bits will remain low. Sufficient coefficients are always loaded to allow for a possible Bank Swap to occur, and the EPROM allocation must allow for this even if the feature is not to be used. Table 5 shows the number of coefficients loaded for each of the modes.

If several devices are cascaded, only one device assumes the role of the Master by having its EPROM pin grounded. It produces a Write Enable signal for the other devices, plus four higher order address outputs on C15:12. The extra address bits on C15:12 define separate areas of EPROM, containing coefficients for up to fifteen additional devices. The least significant block of memory must always be allocated to the Master device. The additional devices need not in practice be all part of the same cascaded chain, but can consist of several independent filters. They must, however, all have their BYTE pins tied low.

When one EPROM is supplying information for several devices, some means of selectively enabling each additional device must be provided. This is achieved by using the C11:8 pins on the slave devices as binary coded inputs to define one to fifteen extra devices. These coded inputs always correspond to the block address used for the segment of EPROM allocated to that device. Code 'all zeros' must not be used since the Master device has implied use of the bottom segment. This is necessary since the C11:8 pins are alternatively used on the Master device to define the number of devices supported by the EPROM.

In addition to providing the most significant addresses to the EPROM, the C15:12 address outputs from the master device must also drive the C15:12 inputs on the slave devices. These C15:12 inputs are internally compared to the C11:8 inputs to decide if that device is currently to be loaded. This approach avoids the need for external decoders and makes the Chip Enable input redundant. This input, however, must be tied low on every device in an EPROM supported system.

The Control Coefficient pin (CCS) is used to define when the control register is to be loaded. It becomes an output on the Master device which provides an EPROM address bit next in significance above A7:0, and also drives the CCS inputs on the slave devices. This output is high for the first two EPROM transfers in order to access the control information, and then remains low whilst the coefficients are loaded. This control information is thus not stored adjacent to the coefficients within the EPROM, and in fact the EPROM must provide twice the storage necessary to contain the coefficients alone. All but two of the bytes in the additional half are redundant. See Fig.16 for the EPROM memory map.

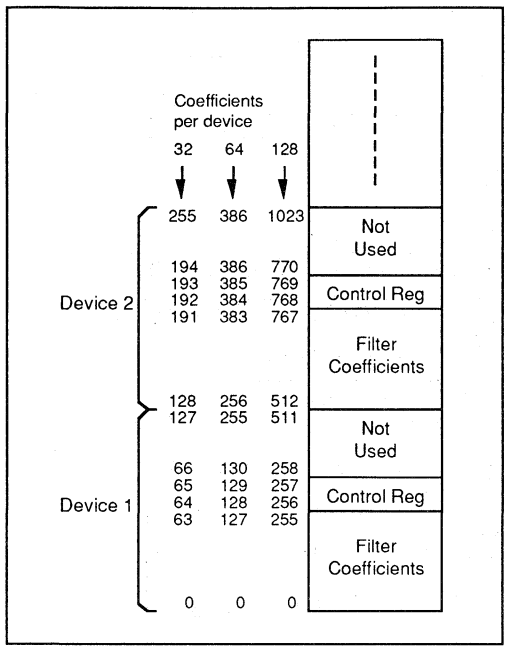


Fig. 16 EPROM Memory Map

Control Register 14 13 12	Number of Coefficients Loaded
0 0 0	32
0 0 1	64
0 1 0	64
0 1 1	128
1 0 0	128
1 0 1	128
1 1 0	128
1 1 1	Invalid Mode

Table 5. Number of Coefficients loaded

NOTE the EPROM memory map Fig. 16 assumes that, for the 32 and 64 coefficient per device options, that the unused address pins are unconnected. If all address pins are connected as shown in Fig. 15 then the 128 coefficients per device memory map column should be used. Only those coefficients required will be read, hence the upper portions of the coefficient address space will be ignored.

USING A REMOTE MASTER

When a remote master is used to load coefficients, the EPROM pin must be tied high and a conventional peripheral interface is then provided. It is not possible, however, to read coefficients already stored. The master supplies an address and data bus, and writes to the PDSP16256 occur under the control of synchronous Chip Enable and Write Strobe inputs. The Coefficient Control Register pin (CCS) must be driven by a master address line higher in significance than A7:0. Both the WEN and CS signals must be low for the load operation to occur. When loading the control register the CS signal must be held low for a further 2 cycles see Fig. 17. Since the internal write operation is actually performed with the system clock, it is necessary for the clock to be present during the transfer.

The BYTE input defines whether coefficients are loaded as a single 16 bit word or two 8 bytes. The latter saves on connections to the remote master. Address bits A7:0 are used in BYTE mode. 16 bit word mode uses bits A6:0, A7 being redundant. When writing in byte mode the least significant byte (A0 = 0) must be written first followed by the most significant byte (A0 = 1).

In the byte mode of working the internal comparison between C15:12 and C11:8 is made, regardless of the state of the EPROM pin. For this reason pins C15:8 should all be tied low when a remote master is used with byte transfers. This ensures that the internal comparison gives equality and allows the load operation to occur.

The address and coefficient busses plus the Write Enable and CS signals must all meet the specified set up and hold times with respect to the system clock, see Fig 17. This synchronous interface is optimum for the majority of high end applications, when individual coefficients must be updated at sample clock rates. If, for convenience reasons, the coefficients are loaded under software control from a general purpose microprocessor, the Write Enable will probably be asynchronous to the system clock used by the PDSP16256. In this case external synchronising logic is needed, see Fig.18.

Fig. 19 shows the recommended loading sequence and filter operation initiation. The simplest technique is to reset the device prior to loading a set of coefficients. Coefficients may be loaded once BUSY returns low or 22 cycles after RESET is taken high.

When loading a device from a remote master the control register must be loaded first followed by the filter coefficients. Fig. 19 shows the required loading sequence, two examples are given one for byte mode the other for word mode. A gap of at least one cycle must be left after loading the control register before loading the first coefficient.

Filter operations are started by presenting the first data word at the same time as raising signal FEN.

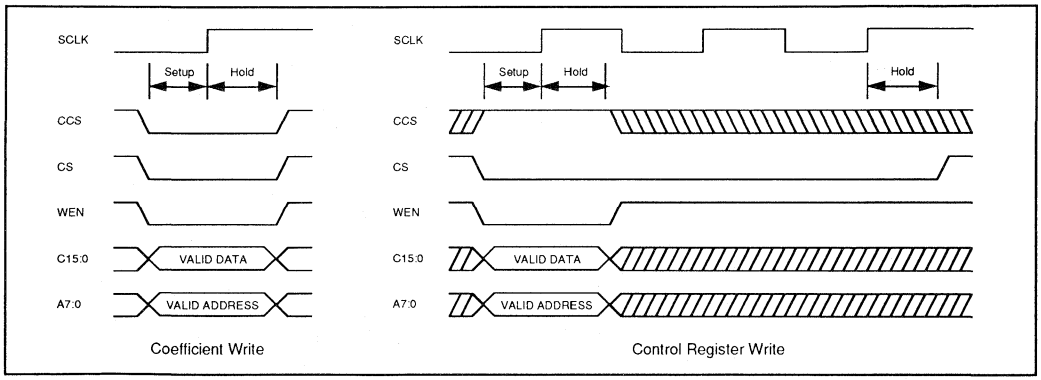


Fig. 17 Remote Master Setup & Hold Timings

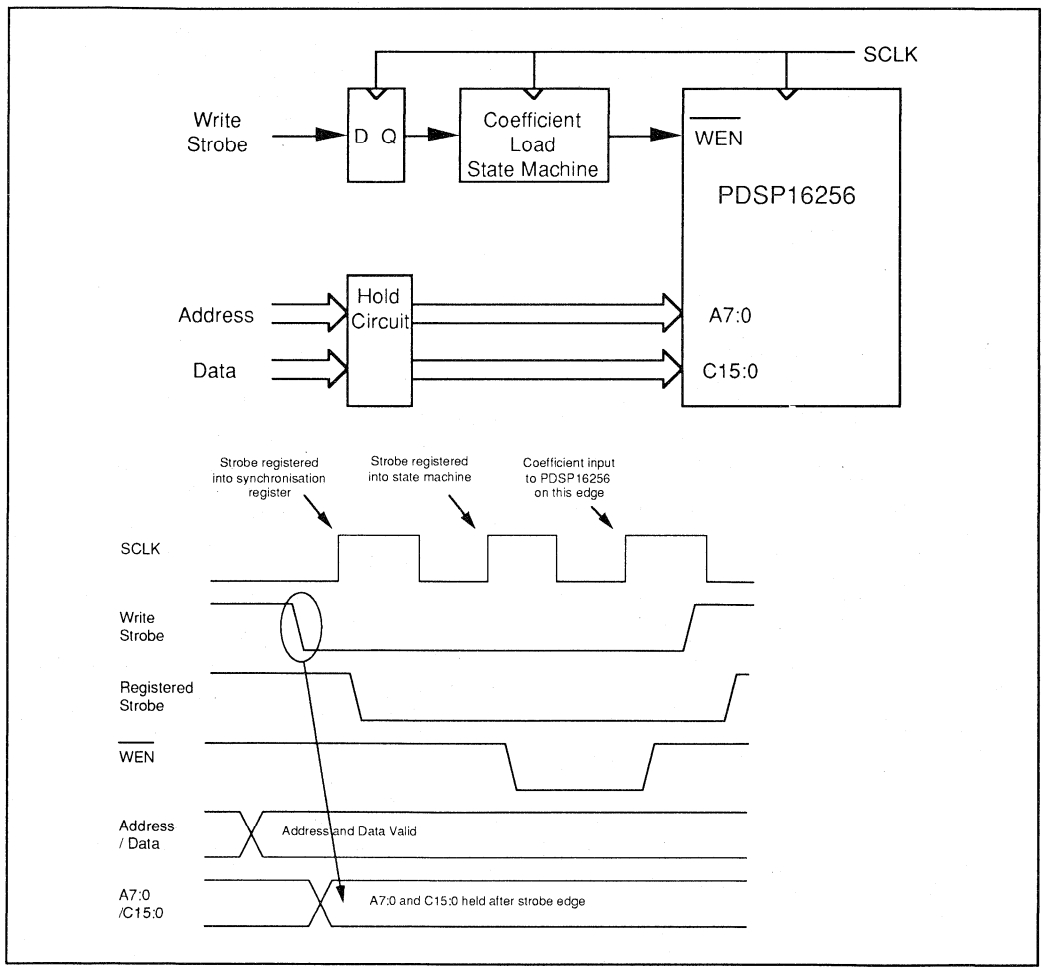


Fig. 18 Remote Master Synchronisation

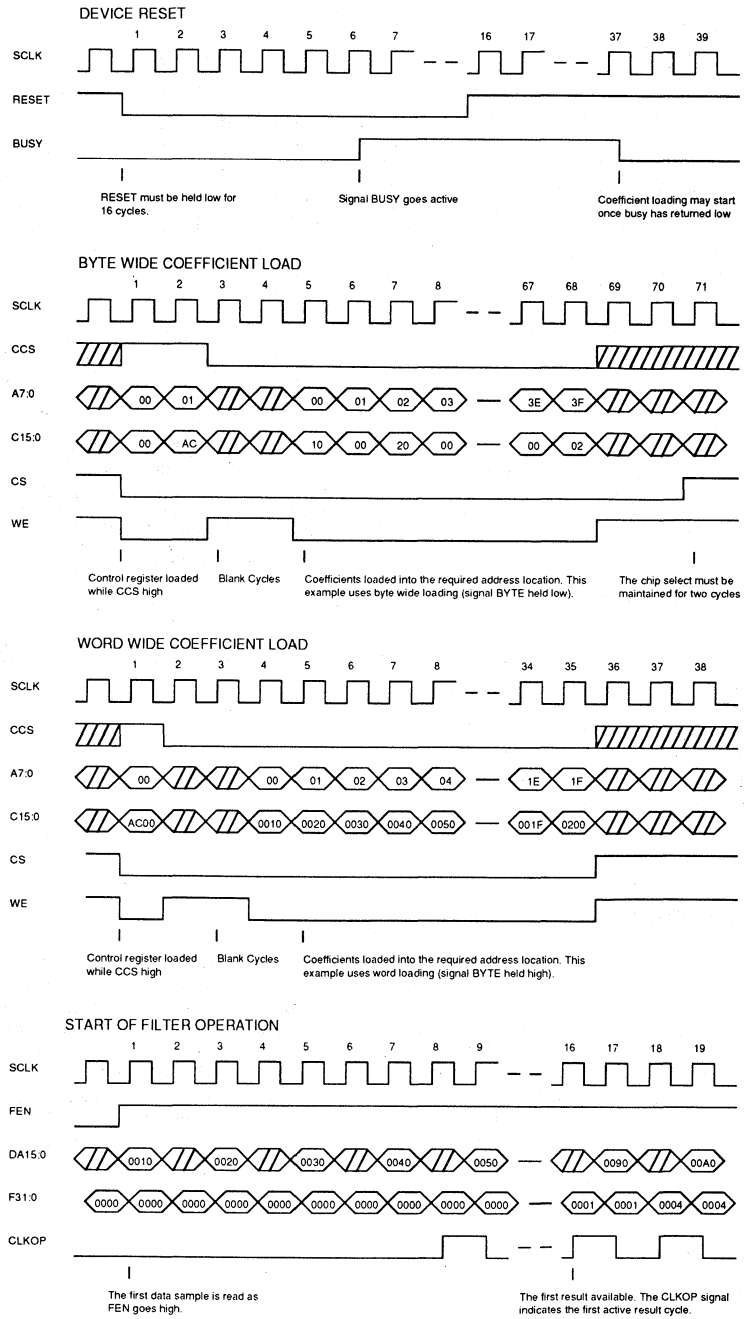


Fig. 19 Device Startup

CONTROL REGISTER

The internal operation of the PDSP16256 is controlled by the status of a 16 bit control register. In the dual filter modes both networks are controlled by the same register. The significance of the various bits are shown in Table 6. Tables 7 and 8 define the control register bit interdependence for the filter and bank swapping modes.

The control register is double buffered. This allows the writing of a new control word without affecting the current operation of the device. To activate the new control register after it has been written to the device the bank swap signal must be toggled. After a reset the active control register is loaded directly and bank swap need not be used.

Control Register Bits		Function
15	4	
0	0	Two independent filters
0	1	Two filters in cascade
1	X	Single Filter

Table 7 Control Register Filter Mode Bits

Control Register Bits			Function
7	6	5	
0	X	0	Control by input pin
1	0	0	Lower bank selected
1	1	0	Upper bank selected
X	X	1	Swap on every sample clock

Table 8 Control Register Bank Swap bits

Bits	Decode	Function
15	0	Dual filter mode
15	1	Single filter mode
14:13	00	Sample rate is the system clock
14:13	01	Sample rate is half the system clock
14:13	10	Sample rate is quarter the system clock
14:13	11	Sample rate is eighth the system clock
12	0	Output rate equals the input rate
12	1	Decimate bt two
11:10	00	Intermediate device
11:10	01	Interface device
11:10	10	Termination device
11:10	11	Single device
9:8	00	These bits MUST be at logical zero
7	0	Bank swap is controlled by input pin
7	1	Bank swap is controlled by Bit 6
6	0	Lower bank if Bit 7 is set
6	1	Upper bank if Bit 7 is set
5	0	Normal Bank Swap
5	1	Bank swap on every sample clock
4	0	Two independent filters
4	1	Two filters in cascade
3:0		These bits MUST be at logical zero

Table 6. Control Register Bit Allocation

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage Vcc	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to Vcc + 0.5V
Output voltage V_{OUT}	-0.5V to Vcc + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HBM)	500V
Storage temperature T_S	-65°C to 150°C
Ambient temperature with power applied T_{AMB}	-55°C to +125°C
Junction temperature with power applied T_J	150°C
Package power dissipation	3000mW
Thermal resistances	
Junction to Case $ø_{JC}$	5°C/W

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device
5. Vcc = Max, Outputs Unloaded, Clock Freq = Max
6. The $ø_{JC}$ data assumes that heat is extracted from the top face of the package.

ELECTRICAL CHARATERISTICS

Operating Conditions (unless otherwise stated)

Commercial:	T_{AMB} = 0°C to +70°C	$T_{J(MAX)}$ = 100°C	Vcc = 5.0V±5%	Ground = 0V
Industrial:	T_{AMB} = -40°C to +85°C	$T_{J(MAX)}$ = 110°C	Vcc = 5.0V±10%	Ground = 0V
Military:	T_{AMB} = -55°C to +125°C	$T_{J(MAX)}$ = 150°C	Vcc = 5.0V±10%	Ground = 0V

Static Charateristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage (CMOS)	V_{IH}	3.5		-	V	SCLK input only
Input low voltage (CMOS)	V_{IL}	-		1.0	V	SCLK input only
Input high voltage (TTL)	V_{IH}	2.0		-	V	All other inputs
Input low voltage (TTL)	V_{IL}	-		0.8	V	All other inputs
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{CC}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{CC}
Output S/C current	I_{OS}	10		300	mA	V_{CC} = Max

Switching Characteristic	Commercial		Industrial		Military		Units	Conditions
	Min.	Max.	Min.	Max.	Min.	Max.		
Input signal setup to clock rising edge	8	-	8	-	8	-	ns	
Input signal hold after clock rising edge	4	-	4	-	4	-	ns	
OEN setup to clock rising edge	20	-	20	-	20	-	ns	
OEN hold after clock rising edge	4	-	4	-	4	-	ns	
Clock rising edge to output signal valid	5	26	5	28	5	28	ns	30pF
Clock Frequency	-	25	-	20	-	20	MHz	
Clock High Time	18	-	20	-	20	-	ns	
Clock Low Time	11	-	12	-	12	-	ns	
Clock to data valid from high impedance	-	30	-	30	-	30	ns	see Fig. 20
Clock to data high impedance	-	30	-	30	-	30	ns	see Fig. 20
Vcc Current	-	320	-	250	-	250	mA	see Note 5

Test	Waveform - measurement level
Delay from output high to output high impedance	V_H, 0.5V
Delay from output low to output high impedance	V_L, 0.5V
Delay from output high impedance to output low	1.5V, 0.5V
Delay from output high impedance to output high	1.5V, 0.5V

V_H - Voltage reached when output driven high
V_L - Voltage reached when output driven low

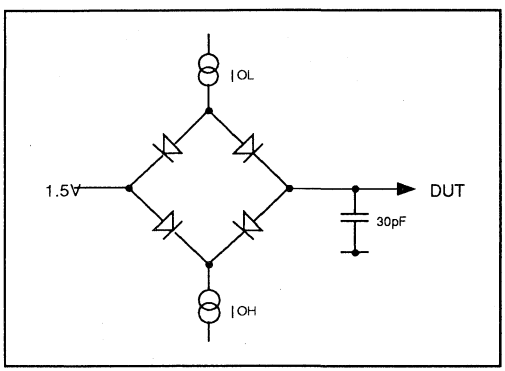


Fig. 20 Three state delay measurement load.

ORDERING INFORMATION

PDSP16256	**B0 AC**	20MHz, Industrial, PGA package
PDSP16256	**B0 GC**	20MHz, Industrial, QFP package
PDSP16256A	**A0 AC**	25MHz, Military, PGA package
PDSP16256A	**B0 AC**	25MHz, Industrial, PGA package
PDSP16256A	**C0 AC**	25MHz, Commercial, PGA package
PDSP16256A	**B0 GC**	25MHz, Industrial, QFP package
PDSP16256	**MA ACBR**	20MHz, MIL-STD-883, PGA package
PDSP16256	**MA GCPR**	20MHz, MIL-STD-883, QFP package
PDSP16256A	**MA GCPR**	25MHz, MIL-STD-883, QFP package

Note: It is anticipated that during the life of this handbook the above product line will be migrated to a newer process technology. This may require the adoption of new part numbers but all of the basic package, temperature grade and screening options will be retained. Contact your local Customer Service Centre to confirm availability.

PDSP16330/A/B

PYTHAGORAS PROCESSOR

(Supersedes version in December 1993 Digital Video & Digital Signal Processing IC Handbook, HB3923-1)

The PDSP16330 is a high speed digital CMOS IC that converts Cartesian data (Real and Imaginary) into Polar form (Magnitude and Phase), at rates up to 20MHz. Cartesian 16+16 bit 2's complement or Sign-Magnitude data is converted into 16 bit Phase format. The Magnitude output may be scaled in amplitude by powers of 2. The Phase output represents a full 2 x π field to eliminate phase ambiguities.

Polyimide is used as an inter-layer dielectric and as glassivation.

The PDSP16330 is offered in three speed grades: a basic 10MHz part (PDSP16330), a 20MHz version (PDSP16330A) and a 25MHz version (PDSP16330). A MIL-STD-883 version is also detailed in a separate datasheet.

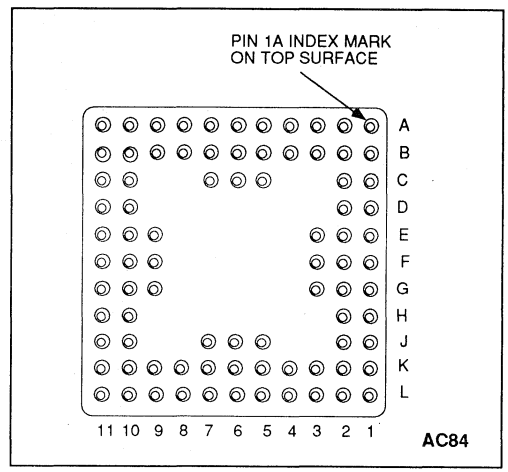


Fig.1 Pin connections - bottom view (PGA)

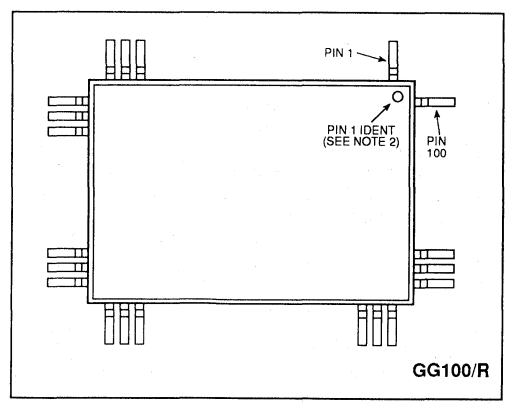


Fig.2 Pin connections - QFP Package

FEATURES

- 25MHz Cartesian to Polar Conversion
- 16-Bit Cartesian Inputs
- 16-Bit Magnitude Output
- 12-Bit Phase Output
- 2's Complement or Sign-Magnitude Input Formats
- Three-state Outputs and Independent Data Enables Simplify System Interfacing
- Magnitude Scaling Facility with Overflow Flag
- Less than 400 mW Power Dissipation at 10MHz
- 84-pin PGA or 100 pin QFP Package or 84 LCC

APPLICATIONS

- Digital Signal Processing
- Digital Radio
- Radar Processing
- Sonar Processing
- Robotics

ASSOCIATED PRODUCTS

PDSP16112	16 X 12 Complex Multiplier
PDSP16116	16 X 16 Complex Multiplier
PDSP16318	Complex Accumulator
PDSP16350	I/Q Splitter and NCO
PDSP16510A	Stand Alone FFT Processor

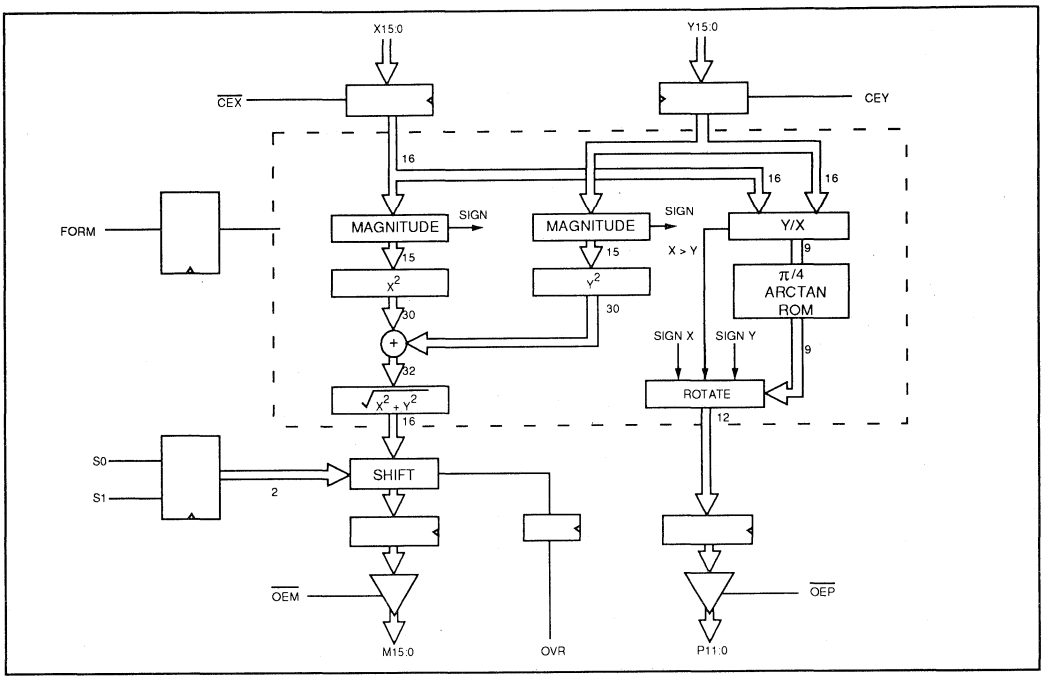


Fig.2 Block diagram

FUNCTIONAL DESCRIPTION

The PDSP16330 converts incoming Cartesian Data into the equivalent Polar Values. The device accepts new 16 + 16 bit complex data every cycle, and delivers a 16 bit + 12 bit Polar equivalent after 24 clock cycles. The input data can be in 2s' Complement or Sign Magnitude format selected via the FORM input. The output is in a magnitude format for both the Magnitude output and the Phase. Phase data is zero for data with a zero Y input and positive X, and is 400 hex for zero X data and positive Y, is 800 hex for zero Y data and negative X, and is C00 hex for zero X and negative Y. The LSB weighting (bit 0) is 2 x π/4096 radians. The 16 bit Magnitude result may be scaled by shifting one, two, or three places in the more significant direction, effectively multiplying the Magnitude result by 2,4 or 8 respectively. Any of these shifts can under certain conditions cause an invalid result to be output from the device. Under these circumstances the OVR output will become active. The PDSP16330 has independent clock enables and three state output controls for all ports.

FORM

This input selects the format of the X and Y input data. A low level on FORM indicates that the Input data is twos' complement format (Note: input data 8000 hex is not valid in 2s' complement mode). This input refers to the format of the current Input data and may be changed on a per cycle basis if desired. The level of FORM is latched at the same time as the data to which it refers.

S1-0

These inputs select the scaling factor to be applied to the Magnitude output. They are latched by the rising edge of CLK and determine the scaling of the output in the cycle after they are loaded into the device. The scale factor applied is determined by the table. Should the scaling factor applied cause an invalid Magnitude result to be output on the M Port, then the OVR Flag will become active for the period that the M Port output is invalid.

S1	S0	Scaling Factor
0	0	x1
0	1	x2
1	0	x4
1	1	x8

The output number range is from 0 to 2 when the scaling factor is set at x1.

PIN DESCRIPTIONS

Symbol	Pin Name and Description
CLK	**Clock:** Common Clock to device Registers. Register contents change on the rising edge of clock. Both pins must be connected.
$\overline{CEX}$	**Clock Enable:** Clock Enable for X Port. The clock to the X port is enabled by a low level.
$\overline{CEY}$	**Clock Enable:** Clock Enable for Y Port The clock to the Y port is enabled by a low level.
X15-X0	**X Data Input** Data presented to this input is loaded into the device by the rising edge of CLK. X15 is the MSB
Y15-Y0	**Y Data Input** Data presented to this input is loaded into the device by the rising edge of CLK. Y15 is the MSB
M15-M0	**M Data Output:** Magnitude data generated by the device is output on this port. Data changes on the rising edge of CLK, M15 is the MSB. The weighting of M15 is determined by the Scale factor selected .
P11-P0	**P Data Output:** Phase data generated by the device is output on this port. Data changes on the rising edge of CLK, P11 is the MSB. The weighting of P11 is π radians.
$\overline{OEM}$	**Output Enable:** Output Enable for M Port. The M Port is in a high impedance state when this input is high.
$\overline{OEP}$	**Output Enable:** Output Enable for P Port. The P Port is in a high impedance state when this input is high.
FORM	**Format Select** This input selects the format of the Cartesian Data input on the X and Y ports. This input is latched by the rising edge of CLK, and is applied at the same time as the data to which it refers. A low level indicates that two's complement data is applied, a high indicates Sign-Magnitude
S1-S0	**Scaling Control:** Control input for scaling of Magnitude Data. This input is latched by the rising edge of CLK, and determines the scaling to be applied to the Magnitude result. The Scaling is applied to the output data in the cycle following the cycle in which the control was latched.
OVR	**Overflow:** Overflow flag. This signal becomes active if the scaling currently selected causes an invalid value to be presented to the Magnitude output.
Vcc	**+5V supply.** All Vcc pins must be connected.
GND	**0V supply.** All GND pins must be connected.

INPUT DATA RANGE

2's Complement	Sign Magnitude
7FFF	7FFF
.	.
.	.
.	.
0001	0001
0000	0000
FFFF	8000
.	.
.	.
.	.
8001	FFF

PIN FUNCTION

Pin No. AC	GG	Function	Pin No. AC	GG	Function	Pin No. AC	GG	Function
F3	91	M7	L9	23	YO	A9	59	X1
G3	92	M6	L10	24	$\overline{CEY}$	B8	60	X2
G1	93	M5	K9	25	CLK	A8	61	X3
G2	94	M4	L11	26	Vcc	B6	62	X4
F1	95	M3	K10	31	GND	B7	63	X5
H1	96	M2	J10	32	GND	A7	64	X6
H2	97	M1	K11	33	GND	C7	65	X7
J1	98	M0	J11	34	GND	C6	66	X8
K1	99	S0	H10	35	GND	A6	67	X9
J2	100	S1	H11	36	GND	A5	68	X10
L1	1	GND	F10	37	GND	B5	69	X11
K2	6	Vcc	G10	38	$\overline{OEP}$	C5	70	X12
K3	7	FORM	G11	39	P0	A4	71	X13
L2	8	Y15	G9	40	P1	B4	72	X14
L3	9	Y14	F9	41	P2	A3	73	X15
K4	10	Y13	F11	42	P3	A2	74	CLK
L4	11	Y12	E11	43	P4	B3	75	OVR
J5	12	Y11	E10	44	P5	A1	76	Vcc
K5	13	Y10	E9	45	P6	B2	81	GND
L5	14	Y9	D11	46	P7	C2	82	$\overline{OEM}$
K6	15	Y8	D10	47	P8	B1	83	M15
J6	16	Y7	C11	48	P9	C1	84	M14
J7	17	Y6	B11	49	P10	D2	85	M13
L7	18	Y5	C10	50	P11	D1	86	M12
K7	19	Y4	A11	51	GND	E3	87	M11
L6	20	Y3	B10	52	Vcc	E2	88	M10
L8	21	Y2	B9	57	$\overline{CEX}$	E1	89	M9
K8	22	Y1	A10	58	X0	F2	90	M8

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): T_{amb} (Commercial) = 0°C to + 70°C, T_{amb} (Industrial) = -40°C to + 85°C
V_{cc} (Commercial) = 5.0V ± 5%, V_{cc} (Industrial and Military) = 5.0V ± 1%, GND = 0V

STATIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Sub-group	Conditions
		Min.	Typ.	Max.			
* Output high voltage	V_{OH}	2.4			V	1,2,3	IOH = 3.2mA
* Output low voltage	V_{OL}			0.6	V	1,2,3	IOL=-3.2mA
* Input high voltage (CMOS)	V_{IH}	3.0			V	1,2,3	Inputs $\overline{CEX}$, $\overline{CEY}$ and CLK only
* Input low voltage (CMOS)	V_{IL}			1.0	V	1,2,3	Inputs $\overline{CEX}$, $\overline{CEY}$ and CLK only
* Input high voltage (TTL)	V_{IH}	2.2			V	1,2,3	All other inputs
* Input low voltage (TTL)	V_{IL}			0.8	V	1,2,3	All other inputs
* Input leakage current (Note 1)	I_{IL}	-10		+ 120	µA	1,2,3	GND ≤ V_{IN}≤V_{CC}
† Input capacitance	C_{IN}		10		pF		
* Output leakage current	I_{oz}	-50		+ 50	µA	1,2,3	GND ≤V_{IN} ≤ V_{CC}
† Output SC current	I_{OS}	-50		230	mA		V_{cc} = Max

NOTES
1. All inputs except clock inputs have high value pull-down resistors
2. All parameters marked * are tested during production. Parameters marked † are guaranteed by design and characterisation.

SWITCHING CHARACTERISTICS

	Characteristic	Value						Units	Conditions
		PDSP16330		PDSP16330A		PDSP16330B			
		Min.	Max.	Min.	Max.	Min.	Max.		
†	Input data setup to clock rising edge	15		12		12		ns	
†	Input data Hold after clock rising edge	2		2		2		ns	
†	$\overline{CEX}$, $\overline{CEY}$ Setup to clock rising edge	30		12		12		ns	
†	$\overline{CEX}$, $\overline{CEY}$ Hold aher clock rising edge	0		0		0		ns	
†	FORM, S1:0 Setup to clock rising edge	15		12		12		ns	
†	FORM, S1:0 Hold after clock rising edge	7		2		2		ns	
†	Clock rising edge to valid data	5	40	5	25	5	25	ns	2 x LSTTL + 20pF
*	Clock period	100		50		40		ns	
†	Clock high time	25		15		15		ns	
†	Clock low time	25		15		15		ns	
†	Latency	24	24	24	24	24	24	cycles	
†	$\overline{OEM}$, $\overline{OEP}$ low to data high data valid		30		25	25		ns	2 x LSTTL + 20pF
†	$\overline{OEM}$, $\overline{OEP}$ low to data low data valid		30		25	25		ns	2 x LSTTL + 20pF
†	$\overline{OEM}$, $\overline{OEP}$ high to data high impedance		30		25	25		ns	2 x LSTTL + 20pF
†	$\overline{OEM}$, $\overline{OEP}$ low to data high impedance		30		25	25		ns	2 x LSTTL + 20pF
†	Vcc current (TTL input levels)		110		180	225		mA	V_{CC} = Max Outputs unloaded Clock freq. = Max
†	Vcc current (CMOS input levels)		70		120	150		mA	V_{CC} = Max Outputs unloaded Clock freq. = Max

NOTES
1. LSTTL is equivalent to I_{OH} = 20µA, I_{OL} = -0.4mA
2. Current is defined as negative into the device
3. CMOS input levels are defined as: $V_{IH} = V_{DD}$ - 0.5V, V_{IL} = +0.5V
4. All parameters marked * are tested during production.
   Parameters marked † are guaranteed by design and characterisation.
5. All timings are dependent on silicon speed. This speed is tested by measuring clock period.
   This guarantees all other timings by characterisation and design.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{cc}	-0.5V to + 7.0V
Input voltage, V_{IN}	-0.5V to VCC + 0.5V
Output voltage, V_{our}	-0.5V to VCC + 0.5V
Clamp diode current per pin, I_K (see Note 2)	±18mA
Static discharge voltage (HMB), V_{STAT}	500V
Storage temperature. T_{stg}	-65°C to + 150°C
Ambient temperature with power applied T_{amb}:	
Commercial	0°C to + 70°C
Industrial	-40°C to + 85°C
Military	-55 °C to + 125°C
Package power dissipation P_{TOT}	1200mW
Junction temperature	150°C

THERMAL CHARACTERISTICS

Package Type	θ_{JC}°C/W	θ_{JA}°C/W
AC	12	36
GG	12	35

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded; only one output to be tested at any one time.
3. Exposure to Absoulte Maximum Ratings for extended periods may affect device reliability.

ORDERING INFORMATION

Commercial (0°C to +70°C)

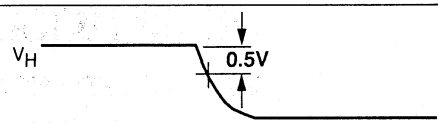
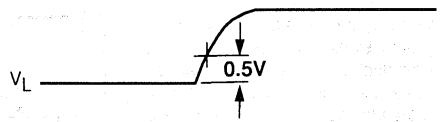
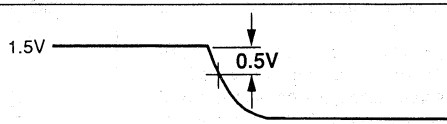
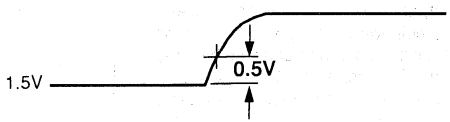
PDSP16330 CO AC	(10MHZ - PGA Package)
PDSP16330A CO AC	(20MHZ - PGA Package)
PDSP16330B CO AC	(25MHZ - PGA Package)

Industrial (-40°C to +85°C)

PDSP16330 BO AC	10MHZ - PGA Package
PDSP16330A BO AC	20MHZ - PGA Package
PDSP16330A BO GG	20MHZ - GG Package
PDSP16330B BO AC	25MHZ - PGA Package

Military (-55°C to +125°C)

PDSP16330A AO AC	20MHZ - PGA Package
PDSP16330A AO GG	20MHZ - GG Package
PDSP16330 AC GG	10MHz - GG Package Mil 883C Screened
PDSP16330A AC AC	20MHz - PGA Package Mil 883C Screened

Test	Waveform - measurement level
Delay from ouput high to output high impedance	
Delay from ouput low to output high impedance	
Delay from ouput high impedance to Output low	
Delay from ouput high impedance to Output high	

NOTES
1. V_H - Voltage reached when output driven high
2. V_L - Voltage reached when output driven low

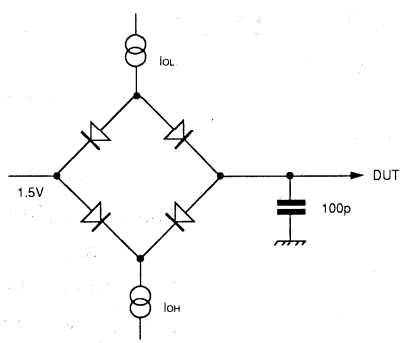


Fig.3 Three state delay measurement load

DS3711 - 2.3

PDSP16350

I/Q SPLITTER / NCO

(Supersedes version in December 1993 Digital Video & Digital Signal Processing IC Handbook, HB3923-1)

The PDSP16350 provides an integrated solution to the need for very accurate, digitised, sine and cosine waveforms. Both these waveforms are produced simultaneously, with 16 bit amplitude accuracy, and are synthesised using a 34 bit phase accumulator. The more significant bits of this provide 16 bits of phase accuracy for the sine and cosine look up tables.

With a 20 MHz system clock, waveforms up to 10 MHz can be produced, with 0.001 Hz resolution. If frequency modulation is required with no discontinuities, the phase increment value can be changed linearly on every clock cycle. Alternatively absolute phase jumps can be made to any phase value.

The provision of two output multipliers allows the sine and cosine waveforms to be amplitude modulated with a 16 bit value present on the input port. This option can also be used to generate the in-phase and quadrature components from an incoming signal. This I/Q split function is required by systems which employ complex signal processing.

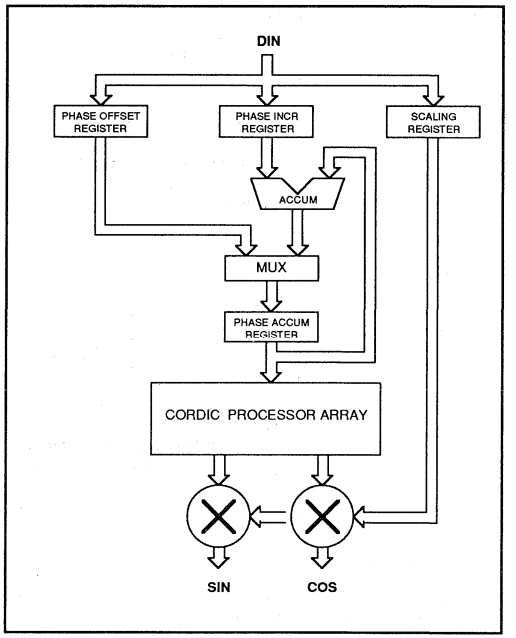


Fig. 1 Block Diagram

FEATURES

- Direct Digital Synthesiser producing simultaneous sine and cosine values
- 16 bit phase and amplitude accuracy, giving spur levels down to - 90 dB
- Synthesised outputs from DC to 10 MHz with accuracies better than 0.001 Hz
- Amplitude and Phase modulation modes
- 84 pin PGA or 132 pin QFP

APPLICATIONS

- Numerically controlled oscillator (NCO)
- Quadrature signal generator
- FM, PM, or AM signal modulator
- Sweep Oscillator
- High density signal constellation applications with simultaneous amplitude and phase modulation
- VHF reference for UHF generators
- Signal demodulator

ASSOCIATED PRODUCTS

PDSP16256/A	Programmable FIR Filter
PDSP16510A	FFT Processor
PDSP16488A	2D Convolver

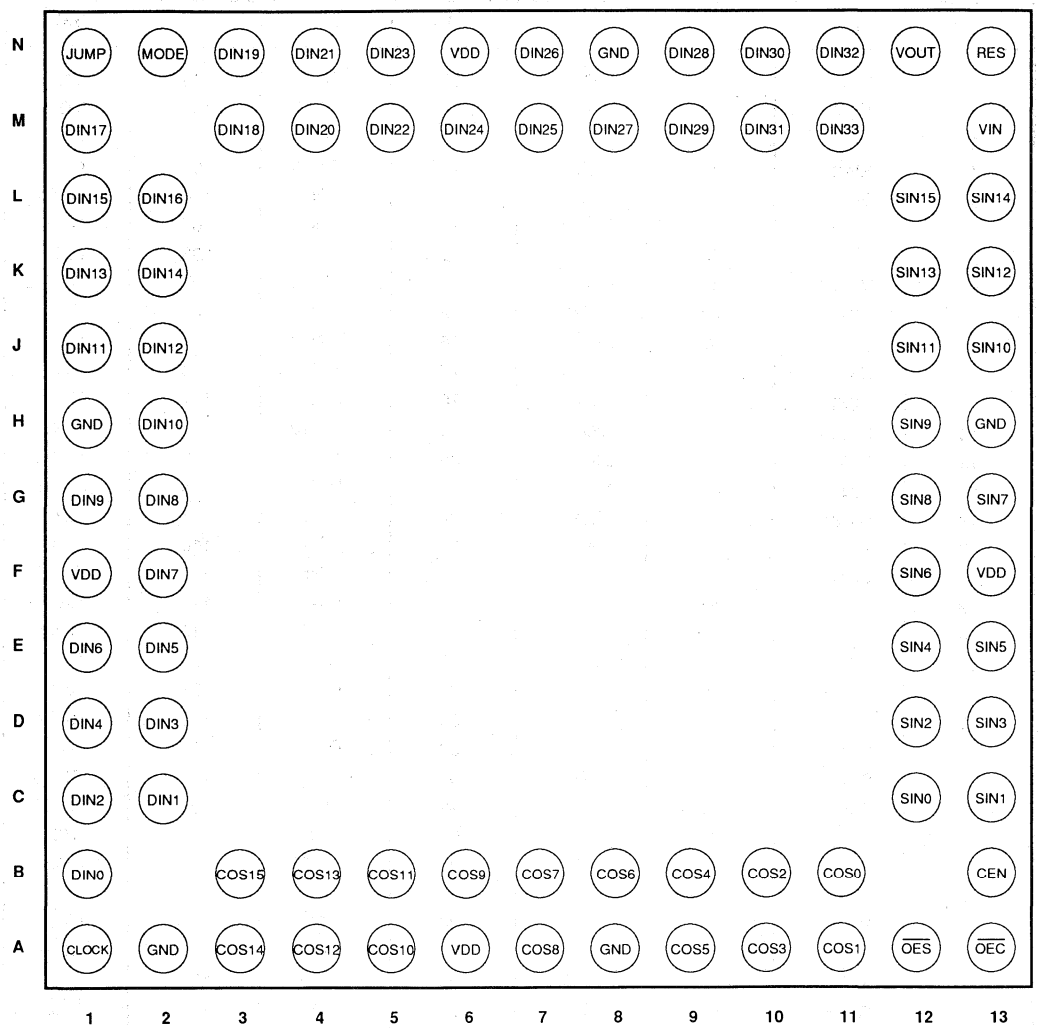


Fig. 2 A. Pin out - bottom view (84 pin PGA - AC84)

GC	SIG	GC	SIG	GC	SIG	GC	SIG
1	N/C	34	N/C	67	GND	100	GND
2	$\overline{CEN}$	35	VOUT	68	DIN17	101	VDD
3	N/C	36	DIN33	69	N/C	102	GND
4	SIN0	37	GND	70	DIN16	103	N/C
5	SIN1	38	VDD	71	DIN15	104	COS15
6	SIN2	39	DIN32	72	GND	105	COS14
7	GND	40	N/C	73	VDD	106	N/C
8	VDD	41	DIN31	74	DIN14	107	COS13
9	SIN3	42	DIN30	75	DIN13	108	COS12
10	SIN4	43	N/C	76	DIN12	109	N/C
11	N/C	44	DIN29	77	N/C	110	COS11
12	SIN5	45	DIN28	78	DIN11	111	N/C
13	SIN6	46	N/C	79	DIN10	112	COS10
14	N/C	47	DIN27	80	N/C	113	COS9
15	SIN7	48	GND	81	DIN9	114	VDD
16	SIN8	49	VDD	82	GND	115	GND
17	VDD	50	DIN26	83	VDD	116	COS8
18	GND	51	DIN25	84	DIN8	117	COS7
19	SIN9	52	DIN24	85	DIN7	118	N/C
20	N/C	53	DIN23	86	DIN6	119	COS6
21	SIN10	54	VDD	87	N/C	120	COS5
22	SIN11	55	DIN22	88	DIN5	121	N/C
23	N/C	56	GND	89	N/C	122	COS4
24	SIN12	57	DIN21	90	DIN4	123	N/C
25	SIN13	58	VDD	91	DIN3	124	COS3
26	SIN14	59	DIN20	92	VDD	125	COS2
27	VDD	60	DIN19	93	GND	126	N/C
28	GND	61	GND	94	DIN2	127	COS1
29	SIN15	62	VDD	95	DIN1	128	VDD
30	VIN	63	DIN18	96	N/C	129	GND
31	N/C	64	MODE	97	DIN0	130	COS0
32	N/C	65	JUMP	98	N/C	131	$\overline{OES}$
33	RESET	66	VDD	99	CLK	132	$\overline{OEC}$

Fig.2B Pin out (132 pin ceramic QFP - GC132)

SIGNAL	DESCRIPTION
DIN33:0	Data bus for the input register. This input register provides a 34 bit, incremental or absolute, phase value, if the mode pin is low. Alternatively if the mode pin is high, it provides either an 18 bit phase increment value, via D17:0, and a 16 bit scale value via D33:18 or a 34 bit phase increment value depending on the JUMP input see below.
SIN15:0	16 bit sine output data in fractional two's complement format.
COS15:0	16 bit cosine output data in fractional two's complement format.
$\overline{CEN}$	Clock enable for the data input register. When low, data will be latched on the rising edge of the clock. When high data will be retained in the input register.
MODE	Mode control input. When low, data in the input register is interpreted as either a 34 bit phase increment value or a 34 bit absolute phase value. When high, the output multipliers are enabled and will scale the waveforms with the upper 16 bits in the input register. The phase increment is loaded from the the lower 18 bits. The full 34 bit phase increment register can also be loaded using JUMP see below.
JUMP	With MODE low (Frequency or Phase Modulation) When low JUMP will allow normal phase incrementing to occur. When high, the data on the input pins will be interpreted as a 34 bit absolute phase value to replace the present value in the accumulator. JUMP is internally latched to match the delay through the data input register, and to allow data in the internal pipeline to be correctly processed. $\overline{CEN}$ must also be low to latch the required data from DIN. When Mode is high (Amplitude Modulation) When low JUMP will allow normal phase incrementing to occur, with the phase increment value taken from the lower 18 data inputs. When high, the data on the input pins will replace the full 34 bits of the phase increment register. $\overline{CEN}$ must also be low to latch the required data.
RES	When high will clear the phase accumulator and phase increment registers, after data in the internal pipeline has been correctly processed.
CLK	Input clock.
$\overline{OES}$	Output enable for SIN 15:0. Outputs are high impedance when $\overline{OES}$ is high.
$\overline{OEC}$	Output enable for COS15:0. Outputs are high impedance when $\overline{OEC}$ is high.
VIN	Valid input flag. A delayed version of this input is available on the VOUT pin, with the delay matching the data processing pipeline delay. This input has no other internal function.
VOUT	Valid output flag. See above.
GND	Five ground pins. All must be connected.
VCC	Four +5V pins. All must be connected.

Table 1. Pin Description

DEVICE OPERATION

Sine and cosine are simultaneously produced by the Cordic processor, which is addressed by the upper 16 bits of the output from a 34 bit phase accumulator. The accumulator divides the digital phase circle into a number of steps, one step for each state of the accumulator. When the accumulator reaches its maximum value it overflows back to zero and the sequence is repeated.

The accumulator is incremented once per incoming clock cycle, by an amount which defines the frequency which is to be generated. The increment required is defined by :

$$\text{Increment} = \frac{\text{Desired O/P Frequency}}{\text{Incoming Clock Frequency}} \times 2^N$$

where N is the number of bits in the accumulator. Since the Nyquist criteria for proper waveform reconstruction must still be obeyed, the maximum output frequency is half the incoming frequency. In practice, when a return is made to the analog world, just meeting the minimum Nyquist requirement would require a 'brick wall' low pass filter to remove the alias signals. A more useful 'rule of thumb' is to limit the generated waveforms to less than 40% of the clock frequency.

The resolution, or tuning sensitivity, of the waveform generator is given by :

$$\text{Resolution} = \frac{\text{Incoming Clock Frequency}}{2^N} \text{ Hz}$$

These equations illustrate some very important features of direct digital synthesisers :-

1) Tuning sensitivity is defined by both the number of bits in the accumulator and the incoming time base frequency.
2) The oscillator tunes linearly over its entire range.
3) The frequency accuracy matches the accuracy of the incoming increment value.
4) DC can be generated since the increment value can be zero.
5) Frequency stability will match the stability of the incoming frequency when the increment is fixed.

The residual noise characteristics of an oscillator are very important in modern communication systems. This parameter defines how well the device maintains its set frequency for very short periods (nanoseconds to seconds) of time. Poor figures will significantly affect the system signal to noise ratio and limit the dynamic range.

The PDSP16350 will, of course, inherit the residual noise characteristics of the source of the incoming frequency. The output frequency is, however, always less than half the incoming frequency in order to satisfy the Nyquist criterion. This is in contrast to a phase locked loop synthesiser, when a small input frequency controls a high output frequency.

The commonly used 20 log N rule states that the phase noise at the output of a synthesiser will be no better than twenty times the log of the ratio of the output frequency to the input frequency. In a phase locked loop synthesiser N is large, in the PDSP16350 it is less than half. Log N is thus less than zero and phase noise improvement is obtained.

The output waveforms are produced after a pipeline delay with respect to the DIN inputs. The effects of the JUMP or RES commands are delayed such that all data in the internal pipe will be processed before the discontinuity occurs. New data may be presented to the device on the cycle following the JUMP or RES and a valid result will be obtained after 31 clock cycles.

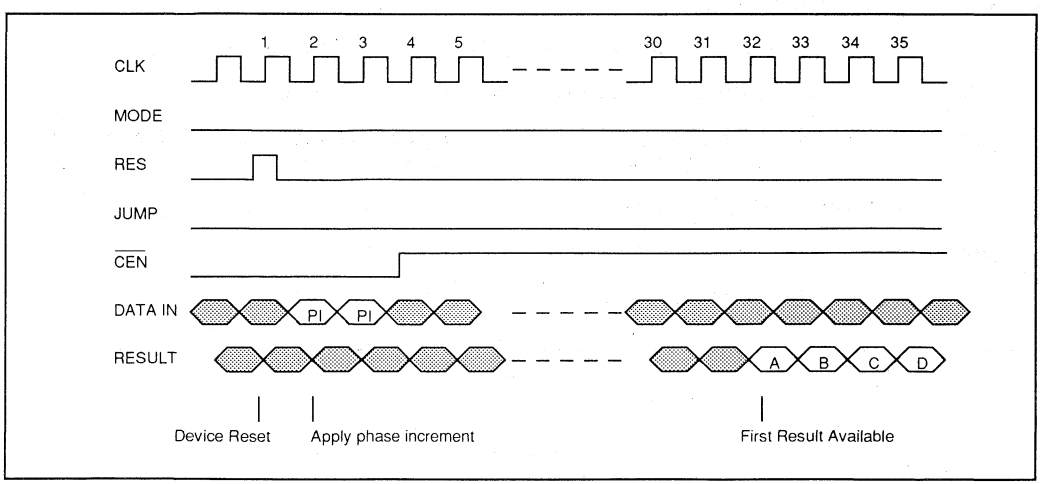


Fig. 3 Fixed Frequency Timing Diagram

USING THE PDSP16350

Frequency, phase, and amplitude modulation are all possible with the PDSP16350. The former two requirements are satisfied by the ability to change the phase increment value on every clock cycle. The latter needs the addition of two multipliers, which allow both sine and cosine to be modified by an incoming waveform.

Fixed Frequency, Constant Amplitude

To generate sine and cosine outputs at a fixed frequency, the MODE pin should be tied low, see Fig. 3. The phase increment value required to generate the desired frequency should be clocked into the internal phase increment register. This value is entered via the DIN port with $\overline{CEN}$ low. If $\overline{CEN}$ subsequently goes inactive (high), the value need not be maintained on the input pins.

The correct phase increment value can be calculated as follows :

$$\text{DIN value} = \frac{\text{Desired O/P Frequency}}{\text{Clock Frequency}} \times 2^{34}$$

This will give a decimal value which must be converted to a 34 bit binary number. The frequency resolution of the generated waveforms will be :

$$\text{Resolution} = \frac{\text{Clock Frequency}}{2^{34}} \text{ Hz}$$

With a 20 MHz clock this results in a frequency resolution of 0.001 Hz. This can be improved by reducing the clock frequency, with the Nyquist restraint being the limiting factor. The latter states that the frequency of the generated waveform must be no more than 50% of the input clock. In practice 40% is a better limit to use, as previously discussed.

A practical example can be used to illustrate the calculation. With a clock frequency of 10.73864 MHz, and the need to generate an output frequency of 20 kHz, then the above equation tells us we need a DIN value of 31996359. This corresponds to a binary value of:

DIN33:0 = 00 0000 0001 1110 1000 0011 1001 1100 0111

The resolution would be 0.0006 Hz. It should be noted that the accuracy of the PDSP16350 cannot be any better than the accuracy of the incoming clock, and these resolutions are based on perfect incoming waveforms.

Fixed Frequency, Modulated Amplitude

The MODE pin should be high if modulation of the output waveforms is required. In this mode each of the output waveforms is multiplied by the 16 bit, two's complement, value, present on the most significant 16 bits of the DIN port. The phase increment register is normally loaded with the 18 bit value on the least significant portion of the DIN bus. It is also possible to load the full 34 bits of the phase increment register when greater accuracy is required, this is explained below. When using the full 34 bits it is possible to obtain the same frequency resolution as in the fixed amplitude mode described earlier. When using 18 bit accuracy directly from the DIN bus the correct phase increment value can be calculated as follows :

$$\text{DIN value} = \frac{\text{Desired O/P Frequency}}{\text{Clock Frequency}} \times 2^{18}$$

The frequency resolution is correspondingly reduced and given by :

$$\text{Resolution} = \frac{\text{Clock Frequency}}{2^{18}} \text{ Hz}$$

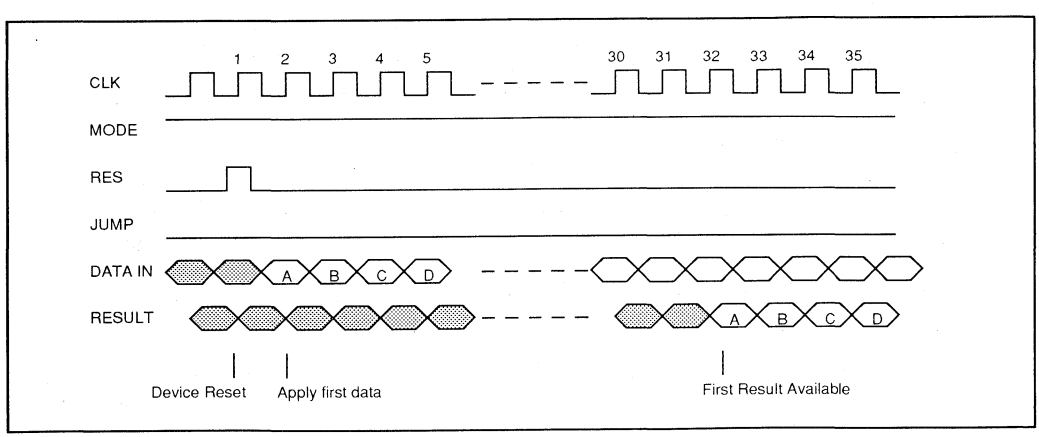


Fig. 4 Amplitude Modulation (18bit frequency accuracy)

Fig. 4 shows the operation of the device when loading the phase increment directly from the DIN bus. First the device must be reset then data is presented on each clock cycle. The amplitude modulation value is presented on the most significant 16 bits while the phase increment is presented on the least significant 18 bits. The first valid result is obtained after 31 cycles. (In this mode the least significant 16 bits of the phase increment register remain low).

Fig.6 shows the operation of the device when using the full 34 bits of the phase increment register. First the device must be reset, then the full 34 bits of the phase increment register are loaded from the DIN bus by taking signal JUMP high before the rising edge of the clock. Following this new data can be presented on each cycle of the clock. The amplitude modulation value is presented on the most significant 16 bits while the phase increment is presented on the least significant 18 bits. The least significant 16 bits of the phase increment register remain fixed at the value loaded using JUMP. The first valid result is obtained after 31 cycles. When using JUMP to load the phase increment register, normal operation cannot be maintained. This is because the amplitude modulation value normally presented on the most significant 16 bits of the DIN bus are replaced by part of the new phase increment value.

The AM mode is useful in systems requiring frequency sweeps. By varying the amplitudes at different frequencies, it is possible to compensate for the analog gain characteristics of amplifiers further along in the system.

It can also be used to generate the in-phase and quadrature components of an analog waveform, which has been digitized and which is to be processed using complex techniques. Such a quadrature heterodyning system, alternatively known as an IQ splitter, is shown in Fig. 5.

The output from an A/D converter drives the D33:18 inputs of the PDSP16350. If all sixteen inputs are not required, the unused least significant bits should be tied to ground, and the more significant inputs connected to the A/D converter. Multiplying an input signal with a local oscillator in this manner produces both sum and difference components. The former can be removed by using the PDSP16256 Programmable FIR Filter.

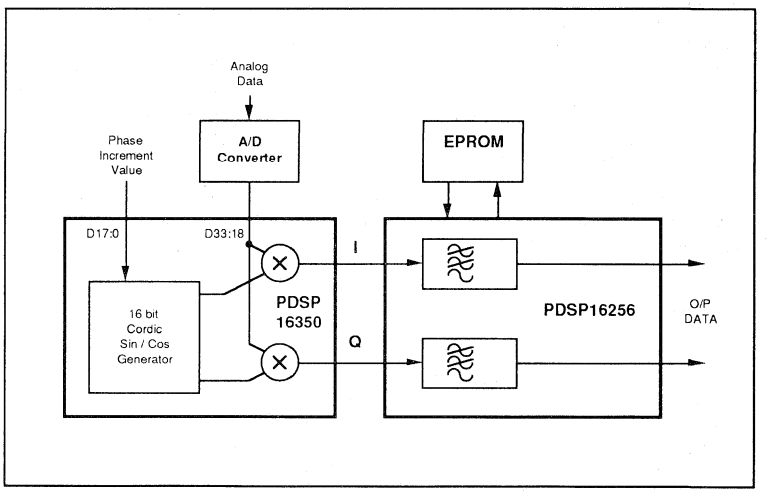


Fig. 5 IQ Split Function

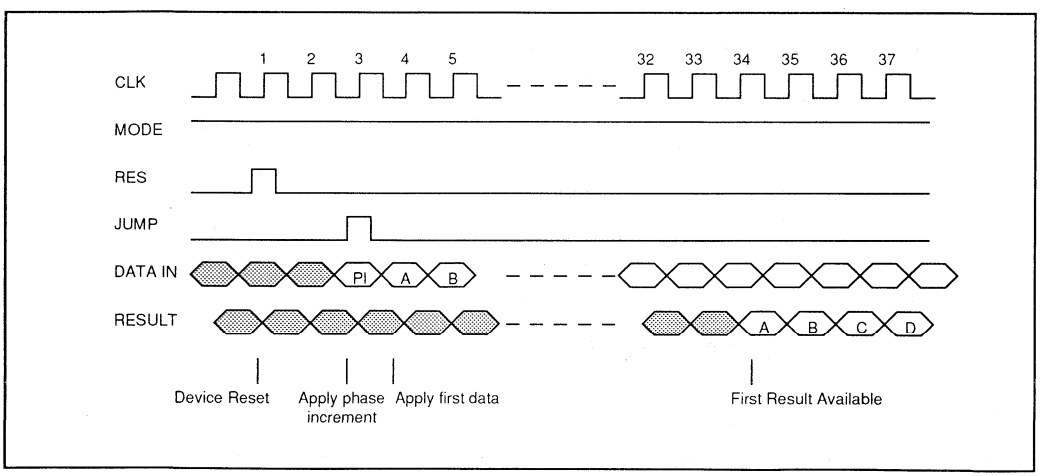


Fig. 6 Amplitude Modulation (34bit frequency accuracy)

Modulated Frequency

The output frequency can be modulated very simply, see Fig 8. Since the phase increment value can be loaded as a complete word every cycle, there is no need to provide internal double buffering to prevent spurious frequencies being generated during the load operation. Binary Frequency Shift Keyed (BFSK) modulation can easily be implemented by externally multiplexing between two phase increment values representing the two frequencies to be used. The value to be used can be instantaneously changed, thus maintaining phase coherence, whilst the bit to be transmitted changes from a mark to a space. Frequency hopping could also be simply effected by clocking a new random number into the DIN port once every thousand cycles, for instance. The output will reflect any change in the frequency after 31 system clock cycles.

If the phase increment value on the DIN port is changed on each clock cycle, then the output frequency will change without introducing any discontinuities. Thus, a linear frequency sweep can be achieved by incrementing the value on the DIN port by a fixed amount each cycle. Alternatively, a logarithmic sweep could be implemented by 'walking' a one across the DIN port. Shifting the input one place to the left every hundred cycles, for example, would double the frequency every time.

Chirp generation for FM - CW Radar systems is a typical example of the need for linear frequency sweeps. This application requires the generation of quadrature chirp waveforms and is illustrated in simplified form by Fig. 7. One waveform is needed for the transmitter, and the other for the receiver. The phase increment value is supplied by the counter block which simply increments at a rate determined by dividing down the time base clock. The synthesised frequency thus increases during the sweep period.

A number of the more significant phase increment bits are used to supply the addresses to a PROM. The output of this PROM is used to amplitude modulate the sine and cosine waveforms. In this manner it is possible to compensate, at the source, for any poor frequency versus gain characteristics of analog circuits further along in the system.

The digital outputs directly drive two D/A converters. Once in the analog world, it is necessary to remove the alias frequencies with low pass filters. The phase linearity and pass band ripple characteristics of these filters are very important, if the correct phase relationships are to be maintained between the two waveforms.

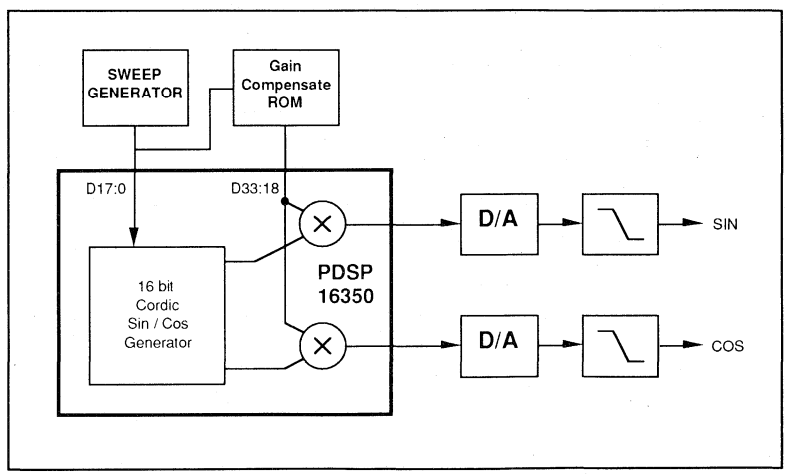


Fig. 7 Quadrature Chirp Generator

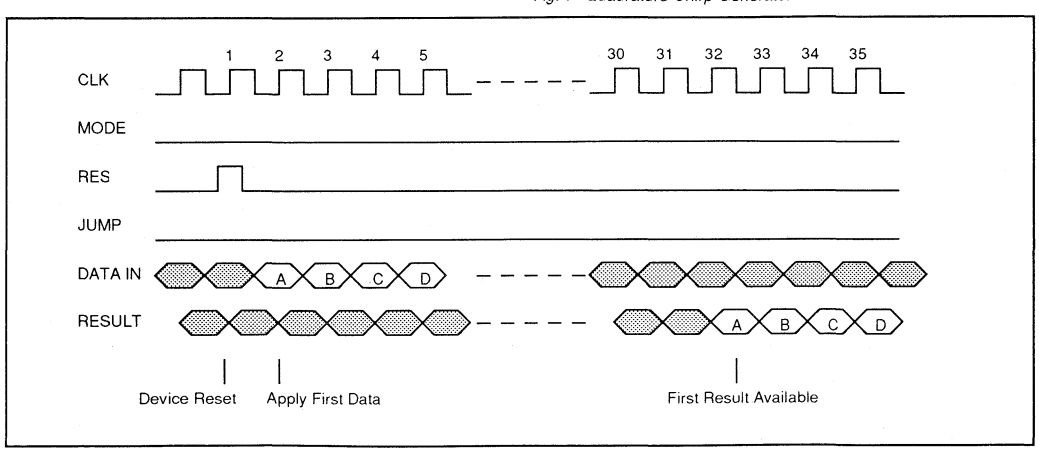


Fig. 8 Frequency Modulation Timing Diagram

Modulated Phase

Relative phase jumps may be made with or without amplitude modulation. For example, if a jump of 180 degrees is required, this can be done with a value of :

DIN33:0 = 10 0000 0000 0000 0000 0000 0000 0000 0000

This is loaded into the phase increment register for one cycle, then the normal increment value is re-loaded in the following cycle.

Alternatively, if no amplitude modulation is needed, an absolute jump to a phase value can be made, see Fig. 9. This can be done by activating the JUMP input during one cycle and also presenting the new phase value at the same time. For example, if a jump to 270 degrees is required :

DIN33:0 = 11 0000 0000 0000 0000 0000 0000 0000 0000

The RES (reset) input can alternatively be used if a jump to 0 degrees is needed. This avoids using the DIN inputs and can be used with or without amplitude modulation. The reset function is internally synchronised to the input clock.

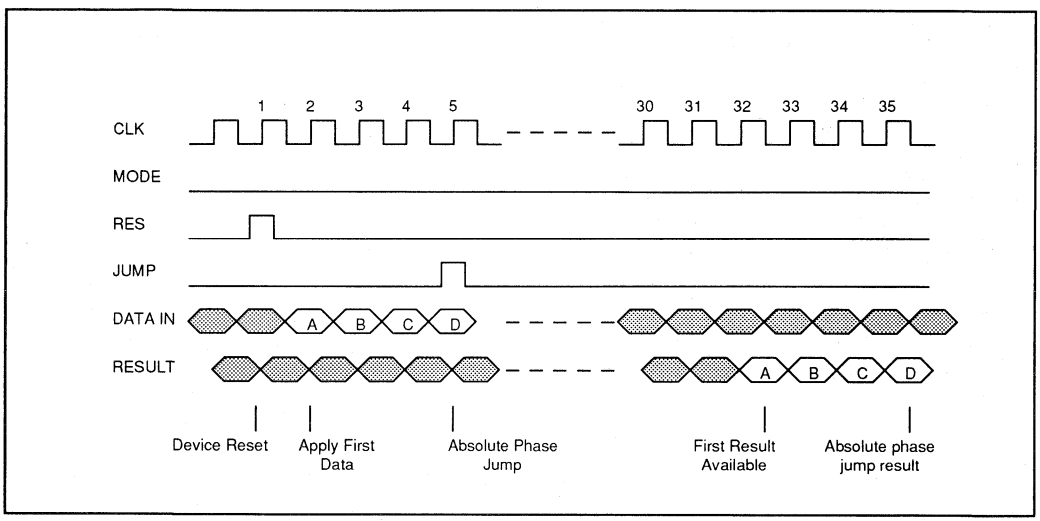


Fig. 9 Phase Modulation Timing Diagram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage Vcc	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to Vcc + 0.5V
Output voltage V_{OUT}	-0.5V to Vcc + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HMB)	500V
Storage temperature T_S	-65°C to 150°C
Ambient temperature with power applied T_{AMB}	
Military	-55°C to +125°C
Industrial	-40°C to 85°C
Junction temperature	150°C
Package power dissipation	3500mW
Thermal resistances	
Junction to Case $ø_{JC}$	5°C/W

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Vcc = Max, Outputs Unloaded, Clock Freq = Max.
5. CMOS levels are defined as
   $V_{IH} = V_{DD} - 0.5v$
   $V_{IL} = +0.5v$
6. Current is defined as positive into the device.
7. The $ø_{JC}$ data assumes that heat is extracted from the top face of the package.

ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise stated)

Commercial: T_{AMB} = 0°C to +70°C $T_{J(MAX)}$ = 95°C V_{CC} = 5.0V±5% Ground = 0V
Industrial: T_{AMB} = -40°C to +85°C $T_{J(MAX)}$ = 110°C V_{CC} = 5.0V±10% Ground = 0V
Military: T_{AMB} = -55°C to +125°C $T_{J(MAX)}$ = 150°C V_{CC} = 5.0V±10% Ground = 0V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	3.0		-	V	
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{CC}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{CC}
Output S/C current	I_{SC}	40		250	mA	V_{CC} = Max

Switching Characteristics

Characteristic	Industrial			Military			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
D33:0 signal setup to clock rising edge	15		-	15		-	ns	
D33:0 signal hold after clock rising edge	4		-	4		-	ns	
CEN setup to clock rising edge	20		-	20		-	ns	
CEN hold after clock rising edge	0		-	0		-	ns	
JUMP, RES setup to clock rising edge	10		-	10		-	ns	
JUMP hold after clock rising edge	6		-	6		-	ns	
RES hold after clock rising edge	8		-	8		-	ns	
Clock rising edge to output valid	5		30	5		30	ns	30pF
Clock freq	DC		20	DC		20	MHz	
Clock High Time	15		-	15		-	ns	
Clock Low Time	20		-	20		-	ns	
$\overline{OES}$,$\overline{OEC}$ low to data valid	-		20	-		20	ns	30pF
$\overline{OES}$,$\overline{OEC}$ high to data high impedance	-		20	-		20	ns	30pF
Pipeline delay VIN to VOUT	31		31	31		31	CLKs	
Vcc Current (CMOS inputs)	-		430	-		450	mA	See Note 4
Vcc Current (TTL inputs)	-		460	-		500	mA	See Note 4

ORDERING INFORMATION

Industrial (-40°C to +85°C)

PDSP16350 / B0 / AC (20MHz - PGA)
PDSP16350 / B0/ GC (20MHz - QFP)

Military (-55°C to +125°C)

PDSP16350 / A0 / AC (20MHz - PGA)
PDSP16350 / A0/ GC (20MHz - QFP)

PDSP16488A

SINGLE CHIP 2D CONVOLVER WITH INTEGRAL LINE DELAYS

(Supersedes October 1995 Edition, DS3713 - 4.0)

The PDSP16488A is a fully integrated, application specific, image processing device. It performs a two dimensional convolution between the pixels within a video window and a set of stored coefficients. An internal multiplier accumulator array can be multi-cycled at double or quadruple the pixel clock rate. This then gives the window size options listed in Table 1.

An internal 32k bit RAM can be configured to provide either four or eight line delays. The length of each delay can be programmed to the users requirement, up to a maximum of 1024 pixels per line. The line delays are arranged in two groups,which may be internally connected in series or may be configured to accept separate pixel inputs. This allows interlaced video or frame to frame operations to be supported.

The 8 bit coefficients are also stored internally and can be downloaded from a host computer or from an EPROM. No additional logic is required to support the EPROM and a single device can support up to 16 convolvers.

The PDSP16488A contains an expansion adder and delay network which allows several devices to be cascaded. Convolvers with larger windows can then be fabricated as shown in Table 2.

Intermediate 32 bit precision is provided to avoid any danger of overflow, but the final result will not normally occupy all bits. The PDSP16488A thus provides a multiplier in the output path, which allows the user to align the result to the most significant end of the 32 bit word.

Data Size	Window Size Width	X Depth	Max Pixel Rate	Line Delays
8	4	4	40MHz	4x1024
8	8	4	20MHz	4x1024
8	8	8	10MHz	8x512
16	4	4	20MHz	4x512
16	8	4	10MHz	4x512

Table 1 Single Device Configurations

Max Pixel Rate	Pixel Size	Window size 3x3	5x5	7x7	9x9	11x11	15x15	23x23
10MHz	8	1	1	1	4	4	4	9
10MHz	16	1	2	2	-	-	-	-
20MHz	8	1	2	2	6	6	8	-
20MHz	16	1	4	4	-	-	-	-
40MHz	8	1	4 *	4 *	-	-	-	-
40MHz	16	2	-	-	-	-	-	-

* Maximum rate is limited to 30 MHz by line store expansion delays

Table 2 Devices needed to implement typical window sizes

FEATURES

- The PDSP16488A is a fully compatible replacement for the PDSP16488
- 8 or 16 bit pixels with rates up to 40 MHz
- Window sizes up to 8 x 8 with a single device
- Eight internal line delays
- Supports interlace and frame to frame operations
- Coefficients supplied from an EPROM or remote host
- Expandable in both X and Y for larger windows
- Gain control and pixel output manipulation
- 84 pin PGA or 132 pin QFP

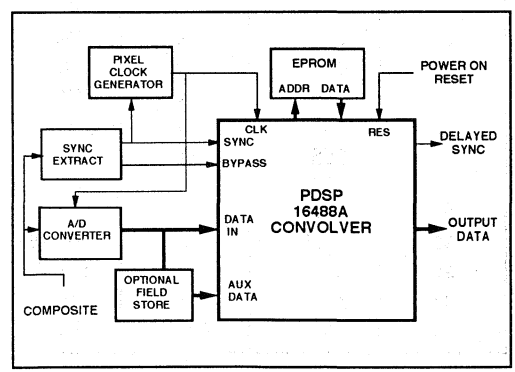


Fig. 1 Typical , Stand Alone, Real Time System

GC	SIG	GC	SIG	GC	SIG	GC	SIG
1	N/C	34	N/C	67	N/C	100	N/C
2	D0	35	X2	68	IP1	101	VDD
3	OEN	36	X3	69	GND	102	F0
4	BIN	37	X4	70	IP2	103	D15
5	PC1	38	N/C	71	N/C	104	N/C
6	VDD	39	X5	72	VDD	105	D14
7	GND	40	GND	73	UP3	106	D13
8	OVER	41	X6	74	VDD	107	GND
9	N/C	42	X7	75	IP4	108	D12
10	HRES	43	N/C	76	GND	109	GND
11	R/W	44	X8	77	IP5	110	VDD
12	CE	45	X9	78	GND	111	VDD
13	N/C	46	VDD	79	IP6	112	D11
14	N/C	47	VDD	80	VDD	113	D10
15	GND	48	VDD	81	IP7	114	D9
16	N/C	49	X10	82	VDD	115	GND
17	DS	50	MASTER	83	N/C	116	CLK
18	GND	51	N/C	84	L7	117	CLK
19	VDD	52	X11	85	GND	118	CLK
20	PROG	53	X12	86	L6	119	GND
21	GND	54	SINGLE	87	GND	120	GND
22	CS3	55	GND	88	L5	121	D8
23	CS2	56	GND	89	VDD	122	VDD
24	CS1	57	N/C	90	L4	123	D7
25	CS0	58	X13	91	VDD	124	D6
26	VDD	59	X14	92	L3	125	D5
27	RES	60	N/C	93	VDD	126	D4
28	PC0	61	X15	94	L2	127	GND
29	N/C	62	VDD	95	GND	128	D3
30	DELEOP	63	BYPASS	96	L1	129	N/C
31	X0	64	IP0	97	F1	130	D1
32	X1	65	VDD	98	L0	131	D2
33	N/C	66	N/C	99	N/C	132	N/C

Pin out Table (132 pin ceramic QFP - GC132)

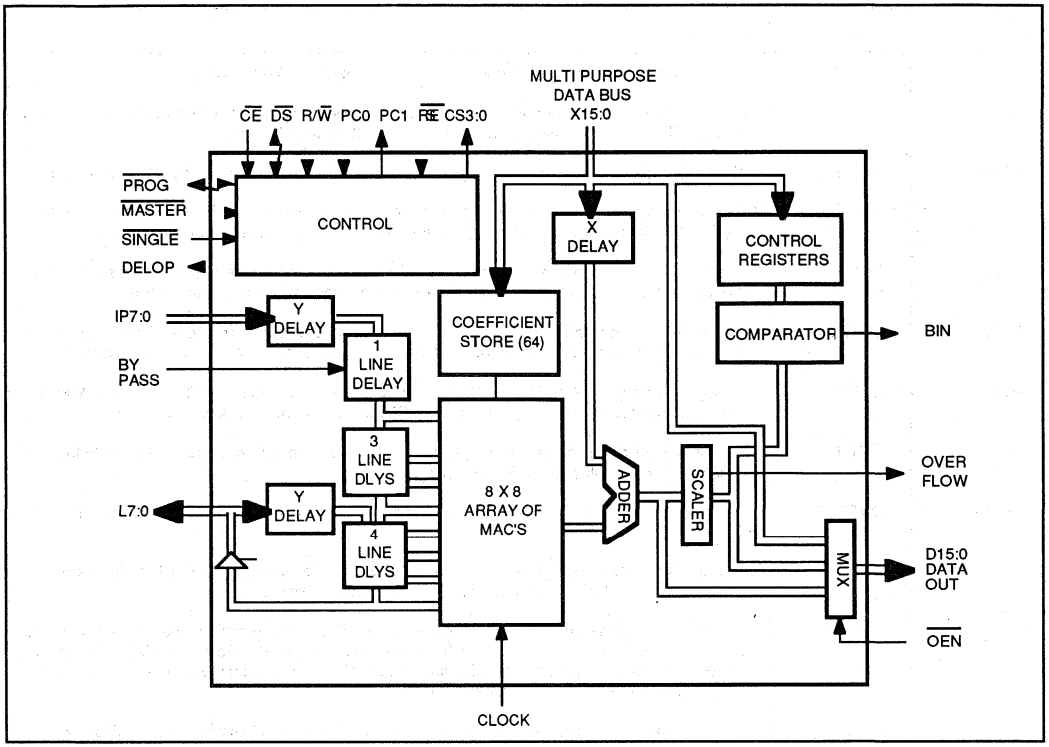


Fig. 2 Functional Block Diagram

PIN NO AC PACKAGE	FUNCTION
A1	L0
B1	F1
C2	L1
C1	L2
D2	L3
D1	SPARE
E2	L4
E1	L5
F2	L6
G2	L7
G1	IP7
H2	SPARE
J1	IP6
J2	IP5
K1	IP4
K2	SPARE
L1	IP3
L2	IP2
M1	IP1
N1	IP0
N2	BYPASS

PIN NO AC PACKAGE	FUNCTION
M3	X15
N3	X14
M4	X13
N4	SPARE
M5	SINGLE
N5	X12
M6	X11
M7	MASTER
N7	X10
M8	X9
N9	X8
M9	X7
N10	X6
M10	X5
N11	X4
M11	X3
N12	X2
N13	X1
M13	X0
L12	DELOP
L13	PC0

PIN NO AC PACKAGE	FUNCTION
K12	RES
K13	CS0
J12	CS1
J13	CS2
H12	CS3
G12	PROG
G13	DS
F12	CE
E13	R/W
E12	HRES
D13	OV
D12	PC1
C13	BIN
C12	OEN
B13	D0
A13	D1
A12	D2
B11	D3
A11	D4
B10	D5
A10	D6

PIN NO AC PACKAGE	FUNCTION
B9	D7
A9	D8
B8	CLK
B7	SPARE
A7	D9
B6	D10
A5	D11
B5	SPARE
A4	D12
B4	D13
A3	D14
B3	D15
A2	F0
F1	VDD
N6	VDD
F13	VDD
A6	VDD
H1	GND
N8	GND
H13	GND
A8	GND

Pin out Table (84 pin PGA - AC84)

NAME	TYPE	DESCRIPTION
IP7:0	INPUT	Pixel data input to the first line delay. [most significant byte in 16 bit mode]
L7:0	I/O	Pixel data input to the second group of line delays. [least significant byte in 16bit mode]. Alternatively an output from the last line delay when the appropriate mode bit is set.
BYPASS	INPUT	The first line delay in the first group is bypassed when this input is active. (High). No internal pull up.
HRES	INPUT	Resets the line delay address pointers when high. Normally the composite sync signal in real time applications. In non real time systems it defines a frame store update period, when low.
X15:0	DUAL FUNCTION	Address/data connections from a MASTER or SINGLE device to the external coefficient source, with X15 defining EPROM or Host support. Otherwise they provide the expansion data input.
D15:0	OUTPUT	Signed 16 bit scaled data or multiplexed 32 bit intermediate data. During intermediate transfers the most significant half is valid when the clock is low, and the least significant half when clock is high.
PC1	OUTPUT	During programming a MASTER device outputs a timing strobe on this pin. This is passed down the chain in a multiple device system, using the $\overline{PC0}$ input on the next device.
PC0	INPUT	This pin is used in conjunction with $\overline{PC1}$ in multiple device systems. It terminates the write strobe from a MASTER device which is EPROM supported.
DELOP	OUTPUT	This output provides a version of the HRES input which has been delayed by an amount defined by the user.
$\overline{DS}$	I/O	The data strobe from a host computer. Active low. This pin will be an output from an EPROM supported MASTER device which provides strobes to the remaining devices.
$\overline{CE}$	INPUT	An active low enable which is internally gated with R/ $\overline{W}$ and $\overline{DS}$ to perform reads or writes to the internal registers. In a SINGLE or MASTER device, which is supported from an EPROM, the bottom 72 addresses are always used and CE is not needed. $\overline{CE}$ can then be used to initiate a new register load sequence after the power on load sequence.
R/ $\overline{W}$	INPUT	Read / not write line from the host CPU. When an EPROM is used this pin should be tied low.
$\overline{PROG}$	I/O	This pin is normally an input which signifies that registers are to be changed or examined. It is, however, an output from an EPROM supported SINGLE or MASTER device indicating to the rest of the system that registers are being updated.
CLK	INPUT	Clock. All events are triggered on the rising edge of the clock, except the latching of least significant expansion inputs . Internally the clock can be multiplied by two or four in order to increase the effective number of multipliers.
BIN	OUTPUT	This output indicates the result from the internal comparison. A high value indicates that the pixel was greater than the internal threshold. The output is only valid from the last device in a chain.
OV	OUTPUT	When high this output indicates that there has been a gain control overflow.
$\overline{RES}$	INPUT	Active low power on reset signal.
$\overline{SINGLE}$	INPUT	Tied to ground to indicate a SINGLE device system. Internal pull up resistor.
MASTER	INPUT	Tied to ground to indicate the MASTER device in a multiple device system. Must be left open circuit in a SINGLE device system. Internal pull up.
$\overline{OEN}$	INPUT	Output enable signal. Active low.
CS3:0	OUTPUTS	Four address bits from a MASTER specifying one of sixteen devices in a multiple device system. Must be externally decoded to provide chip enables for the additional devices.
F1:0	OUTPUTS	These bits indicate the field selection given by the auto select logic. The same coding as that used for Control Register bits C5:4 is used.
VCC / GND	SUPPLY	Four Power and ground pairs. All must be connected.

BASIC OPERATION

The PDSP16488A convolver performs a weighted sum of all the pixels within an N x N two dimensional window. Each pixel value is multiplied by a signed coefficient, or weight, and the products are summed together. In practice positive weights would be used to produce averaging effects, with various distribution laws, and negative weights would be used for edge enhancement. The window is moved continuously over the video frame, and for real time operation a new result must be obtained for every pixel clock. In most applications odd sized windows will be used, resulting in a centre pixel whose value is modified by the surrounding pixels.

OUTPUT ACCURACY

With 8 bit pixels, and an 8 x 8 window, it is possible for the accumulated sum to grow to 22 bits within a single device. With 16 bit pixels, and an 8 x 4 window (the maximum possible), the sum can grow to 29 bits. The PDSP16488A actually allows for word growth up to 32 bits, and thus allows several devices to be cascaded without any danger of overflow. Since coefficients can be negative, the final result is a 32 bit signed two's complement number.

In a particular application the desired output will lie somewhere within these 32 bits, the actual position being dependent on the coefficient values used. This causes problems in physically choosing which output pins to connect to the rest of the system. To overcome this problem the PDSP16488A contains an output multiplier, or gain control, which allows the final result to be aligned to the most significant end of the 32 bit internal result.The provision of a multiplier, rather than a simple shifter, allows the gain to be defined more accurately.

The sixteen most significant bits of the adjusted result are available on output pins, and contain a sign bit.

OUTPUT SATURATION

If the output from the convolver is driving a display, negative pixels will give erroneous results. An option is thus provided which forces all negative results to zero, which are then interpreted as black by the display. At the same time positive results, which overflow the gain control, are forced to saturate at the most positive number ie peak white. In this mode the output sign bit is always zero,and should not be connected to an A/D converter.

A separate option forces both negative and positive overflows to saturate at their respective maximum values, but in scale negative results remain valid. A gain control overflow warning flag is also available, which can be used in a host CPU supported system to change the gain parameters if overflows are not acceptable.

BINARY OUTPUT

The PDSP16488A contains a 16 bit arithmetic comparator which allows the output from the gain control to be compared with a previously programmed value. An output flag allows the user to detemine if the result was above or below a value contained within an internal register.

MULTIPLIER ARRAY

The PDSP16488A contains sixteen 8x8 multipliers each producing a 16 bit result. Internally the pixel clock supplied by the user can be multiplied by two or four, which together with the proprietary architecture, allows each multiplier to be used several times within a pixel clock period. This increases the effective number of multipliers, which are available to the user, from 16 to 32 or 64 respectively. This architecture produces a very efficient utilization of chip area, and allows the line delays to be accommodated on the same device.

The sixteen multipliers are arranged in a 4 deep by 4 wide array, resulting in effective arrays of 4 by 8 or 8 by 8 with the multi-cycling options. The multiplier array can also be configured to handle 16 bit signed pixels; the effective number of available multipliers is then halved.

LINE DELAY OPERATION

Internal RAM is arranged in two separate groups, and can be configured to provide line delays to match the chosen size of the convolver. When a four deep arrangement is used, with 8 bit pixels, four line delays are available, and each can be programmed to contain up to 1024 pixels. In an eight deep array, or if16 bit pixels are needed, each line can contain up to 512 pixels. Figure 4 illustrates the options available.

The first line delay in one of the groups can optionally be switched in or out under the control of an input pin. It is used to delay the pixel input when data is obtained from another convolver in a multiple device system, or it is used to support interlaced video.

Signals L7:0 may be used as pixel inputs or outputs. They are configured as inputs at power-on to avoid possible bus conflicts, but by setting a mode control bit can become outputs. They can then be used to drive another device when multiple PDSP16488A's are required.

INTERLACED VIDEO

When using real time interlaced video, a picture or frame is composed from two fields, with odd lines in one field and even lines in the other. An external field delay is thus required to gather information from adjacent lines, and the convolver needs two input busses. The bus providing the delayed pixels has an extra internal line delay. This is only used in the field containing the upper line in any pair of lines, and must be bypassed in the other field. It ensures that data from the previous field always corresponds to the line above the present active line, and avoids the need to change the position of the coefficients from one field to the next.

Figure 3 shows the translation from physical to internal line positions, for single device interlaced systems. Line N is the line presently being convolved, which is either one or two lines previous to the line presently being produced.

When windows requiring four or more lines are to be implemented, the first line delay, in the group supplied from the L7:0 pins, must always be by-passed. This by-pass option is controlled by Register B, bit 7 and is not effected by the BYPASS input pin.. The coefficients must be loaded into the locations shown, which match the translated line positions, with unused coefficients, shown shaded, loaded with zero's.

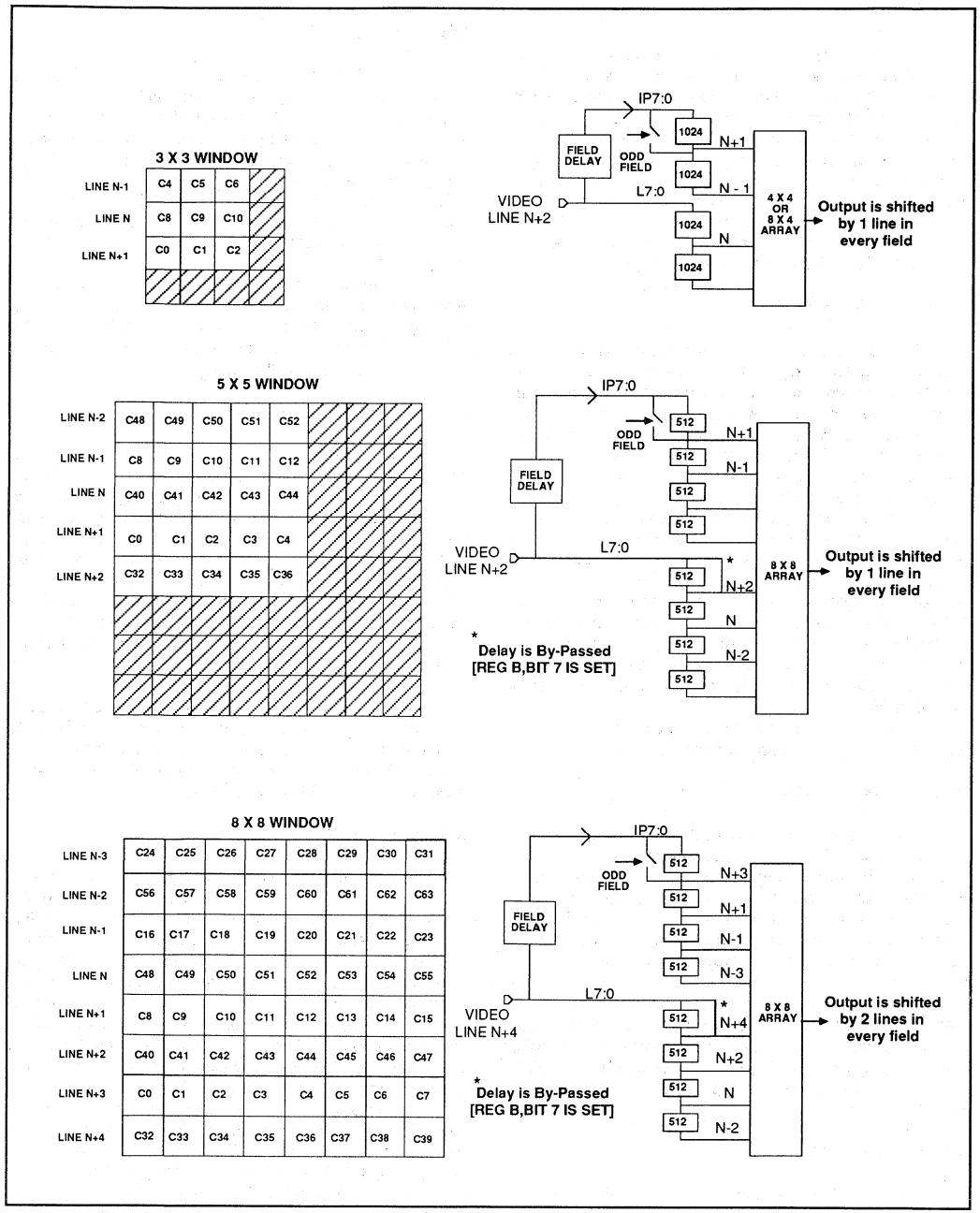


Figure 3. Line Delay Allocations in Single Device Interlaced Systems

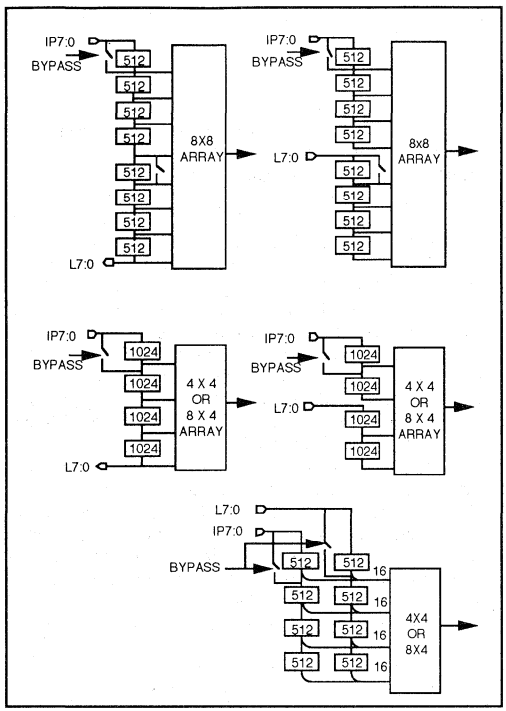


Fig. 4. Line Delay Configurations

DEFINING THE LENGTH OF THE LINE DELAY

Figure 4 defines the maximum line lengths available in each of the window size options. The actual line lengths can be defined in one of three ways, to support both real time applications, taking pixels directly from a camera, and also use in systems supported by a frame store. In the former case the line delays must be referenced to video synchronization pulses. In the latter case the line lengths are well defined, and the horizontal flyback 'dead times' will have been removed.

To support real time applications an option is provided in which the length of the line delay is defined by the number of clocks obtained whilst an input pin (HRES) is in-active. HRES would normally be composite sync when the convolver is directly attached to an NTSC or PAL video camera.

Conceptually, the line delay is achieved by reading the previous contents of a RAM based line store, and then writing new information to the same address. When HRES is active write operations are inhibited, and the address counter is reset. During an active line the counter is incremented by the pixel clock. If the maximum count is reached before the end of a line, then write operations are terminated and wrap-around effects avoided.

The active going edge of HRES, marking the end of a line, is normally asynchronous to the pixel clock, and it is possible for an additional pixel to be stored on some lines. This has no effect on the convolver operation, and will not cause a cumulative shift in the pixel position from line to line.

An alternative means of defining the line length is, however, provided when an exact number of pixels is needed. HRES going in-active then starts the delay operation for every line, but it ceases when the 10 bit value contained in two registers is reached. This method can avoid the need to store blank pixels at the end of a line before sync goes active. With this method the line must contain an even number of pixels, but the value loaded into the control registers defining the line length, must be one less than the even number needed.

In an image processing system, the pixel clock is often re-synchronized, or even inhibited, during blanking or sync. The next line is then started with a precise time interval from the end of sync to the first pixel clock edge. This avoids any visible pixel jitter at the beginning of the line, which would otherwise be present since pixel clock is asynchronous with respect to video sync pulses.

When using the PDSP16488A the pixel clock should not be inhibited, or re-synchronized, until the delayed version of the HRES input goes active. This is present on the DELOP output pin. This will ensure that no pixels on the right hand edge are lost due to the internal pipeline delay.

If the pixel clock is a continuous signal, the user must ensure that the HRES in-active transition meets the timing requirements defined in Figure 10. The active going edge at the end of a line need not be synchronized.

When pixels are read/written to a frame store, an alternative line delay configuration is needed. Within the frame store lines would be stored in contiguous locations, with no gaps caused by the flyback period between the lines. This method of use makes the HRES defined line delay operation difficult to use, and an alternative mode of operation is provided. The HRES input is then driven by a system provided signal, which defines a complete frame store update period. It is not a line defining signal. The high to low transition of this signal will initiate the line store update sequence and allow the internal address pointers to increment. These pointers will be synchronously reset at the end of a line, when they reach the pre-programmed value. They will then immediately start a new operation using address zero. The actual line delay must be pre-loaded into two control registers as described previously.

Write operations back to the frame store must allow for the total pipeline delay. This can be achieved by inhibiting write operations until the delayed version of HRES goes low at the DELOP output pin. Write operations then continue until it goes back high. The PDSP16488A assumes that data is valid when a clock signal is applied, and that it also meets the set up and hold requirements given in Figure 10. If data is not valid, due for example to a frame store DRAM refresh cycle, then the user must externally inhibit the clock. The clock supplied to the convolver will in this mode be a signal which defines a frame store cycle time.

The use of the convolver in a line scan system is similar to its use with a frame store. These systems have no flyback period, and the address counter must be synchronously reset at the end of the line and then allowed to continue.

GAIN CONTROL

The gain control is provided as an aid to locating the bits of interest in the 32 bit internal result. The magnitude of the largest convolved output will depend on the size of the

window, and the coefficient values used. The function of the gain control is then to produce an output, which is accurate to 16 bits, and which is aligned to the most significant end of this 32 bit word. The sixteen most significant bits of the word are available on output pins, and the largest number need only have one sign bit if the gain control is correctly adjusted.

Fiigure 5 indicates the mechanism employed with the required function implemented in two steps. Two mode control bits allow one of four 20 bit fields to be selected from the final 32 bit value. These four fields are positioned with the first at the most significant end, and then at four bit displacements down to the least significant end.

By setting an enabling bit, the field selection can optionally be done automatically. This feature should only be used in the real time operating mode, when HRES defines video lines. Internal logic examines the most significant 13, 9, or 5 bits from the 32 bit result, and makes a field selection dependent on which group does not contain identical sign bits. If less than five sign bits are obtained, the logic will select the field containing the most significant 20 bits.

The automatic selection is particularly useful when a fixed scene is being processed. The selection is reset when any internal register is updated (ie PROG has been active) and is then held in-active for ten further occurances of the HRES input. This allows the internal multiplier/ accumulator array to be completely flushed before a field selection is made. As convolver outputs of greater magnitude are produced the field selection logic will respond by selecting a more significant field. The most significant field found necessary remains selected until PROG again goes active. Even if the automatic field selection is not enabled, two outputs, F1:0, will still indicate which field would have been selected. These are coded in the same way as Register C, bits 5:4.

Having chosen a field, either manually or automatically, it is then multiplied by a 4 bit unsigned integer. This is contained within a user programmed register, and the multiplication will produce a 24 bit result . The middle 16 bits of this result contain the required output bits. The gain control multiplier can overflow in to the unused most significant four bits if the parameters are chosen wrongly. This condition is indicated by an overflow flag .

By setting appropriate mode control bits, further manipulation of the gain control output is possible. One option allows all negative outputs to be forced to zero, and at the same time positive gain control overflows will saturate at the maximum positive number. A different option will saturate positive and negative overflows at their respective maximum values, but otherwise leaves them unchanged. Occasional overflows can be tolerated in some systems, and this option prevents any gross errors.

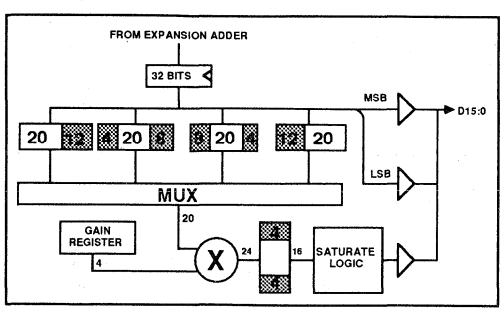


Fig. 5. Gain Control Operation

EXPANSION

Multiple devices can be connected in cascade in order to fabricate window sizes larger than those provided by a single device. This requires an additional adder in each device which is fed from expansion data inputs. This adder is not used by a single device or the first device in a cascaded system, and can be disabled by a mode control bit.

The first device in the cascaded system must be designated as a MASTER device by tying an input pin low. Its expansion input bus is then used as the source of data for the coefficient and control registers in all devices in the system.

In order to reduce the pin count required for 32 bit busses, both expansion in and data out are time multiplexed with the phases of the pixel clock. When the clock is high the least significant half will be valid, and when the clock is low the most significant half will be valid.

In practice this multiplexing is only possible with pixel clocks up to 20MHz. Above these frequencies the multiplexing must be inhibited by setting a Mode Control bit (Register A, Bit 7). The intermediate data accuracy will then be reduced, since only the lower 16 bits of the internal 32 bit intermediate sum are available on the output pins. In such systems the coefficients must be scaled down in order to keep the intermediate and final results down to 16 bits. The final device should not use the gain control, and instead should simply output the non-multiplexed 16 bit result. The overflow flag and pixel saturation options will not be available.

PIXEL INPUT AND OUTPUT DELAYS

In a real time system, when line delays are referenced to video sync pulses present on the HRES input, the first pixel from the last line delay does not appear on the L7:0 pins until the fifth active pixel clock edge after HRES has gone low. This is illustrated in Figure 7. In a vertically expanded system, this output provides the input to the first line delays in the vertically displaced devices. The internal logic is thus designed to always expect this five clock delay. Compensation must thus be applied to the devices which are directly connected to the video source, such that the first pixel is not valid until the fifth clock edge.

For this reason the PDSP16488A contains an optional four clock pipeline delay on each of the pixel data inputs. When the delay is used the first pixel in a video line must be available on the input pins after the first pixel clock edge. This would be so if the device were connected to an A/D converter, since that would introduce a one pixel pipeline delay. If the system introduces any further external pipeline delays, then the internal delay should be bypassed, and the user should ensure that the first pixel is valid after the fifth clock edge.

The use of this four clock delay is controlled by Bit 3, in Control Register B. This delay is in addition to the delays which are provided to support expansion in both the X and Y directions, and are controlled by Register D, Bits 3:2. Both delays are in fact simply added together in the device, but are provided for conceptually different reasons.

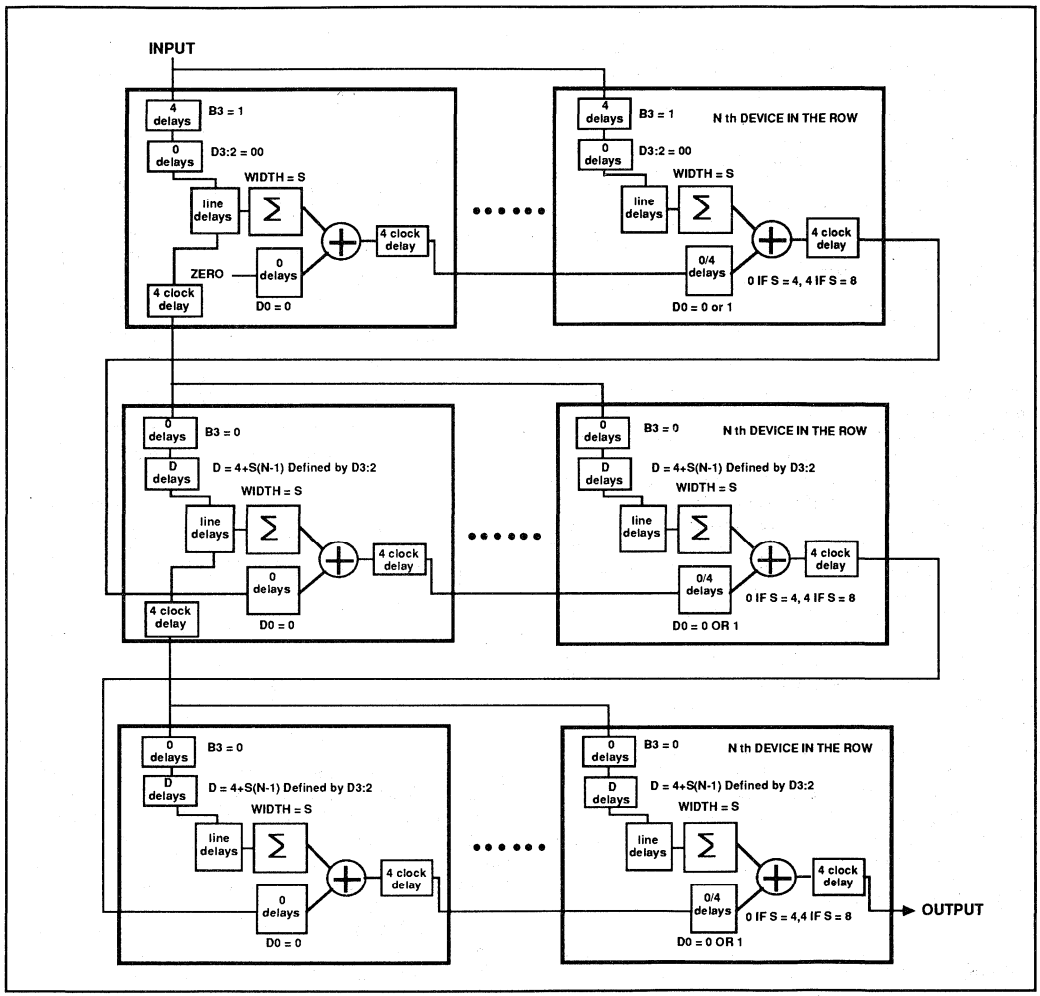


Fig. 6. Multi-Device Delay Paths

DELAY COMPENSATION FOR LARGE WINDOWS

A large window is composed of several partial windows each of which is implemented in an individual device. If necessary the partial window must be padded with zero coefficients to become one of the standard sizes. When constructing a large window it is necessary to delay the expansion data inputs in order to compensate for growth in the horizontal direction. Delays in the partial sums are also necessary to compensate for the total pipeline delay needed to produce the previous complete horizontal stripe.

Within each device in a horizontal stripe, apart from the first, the expansion input must be delayed by the width of the partial window, before it is added to the internal sum. Since partial windows can only be 4 or 8 pixels wide,a delay of 4 or 8 pixel clocks is needed. There is, however, an in-built delay of 4 pixels in the inter device connection, and the PDSP16488A thus only needs an option to delay the expansion input by an additional four pixels.

The data from the last device in a horizontal row of convolvers feeds the expansion input of the first device in the next row. This is shown in Figure 6. With this arrangement, the position of the partial window as illustrated, is the inverse of its vertical position on a normal TV screen. Thus the top, left hand, device corresponds to the bottom, left hand, portion of the complete window.

The output from the last device in the row is delayed with respect to the original data input by an amount given by the formula;

DELAY = 4 + [N-1].S where N is the number of devices in a row and S is the partial window width, ie 4 or 8.

The internal convolver sums, in each of the devices in the next row, must be delayed by this amount before they are added to results from the previous row. This is more conveniently achieved by delaying data going into the line stores. The required cumulative delay with respect to the first horizontal stripe is then automatically obtained when more than two rows of devices are needed.

Two bits in Control Register D are used to define one of four delay options. These delays have been selected to support systems needing from two to eight devices and are described in the applications section.

COEFFICIENTS

Sixty-four coefficients are stored internally and must be initially loaded from an external source. Table 3 gives the coefficient addresses within a device, with coefficent C0 specified by the least significant address and C63 by the most significant address. Table 5 shows the physical window position within the device which is allocated to each coefficient in the various modes of operation. Horizontally the coefficient positions correspond to the convolution process as if it were conceptually observed on a viewing screen, ie the left hand pixel is multiplied with C0. In the vertical direction the lines of coefficients are inverted with respect to a visual screen, ie the line starting with C0 is actually at the bottom of the visualized window.

The coefficients may be provided from a Host CPU using conventional addressing, a read/write line, data strobe, and a chip enable. Alternatively, in stand alone systems, an EPROM may be used. A single EPROM can support up to 16 devices with no additional hardware.

When windows are to be fabricated which are smaller than the maximum size that the device will provide in the required configuration, then the areas which are not to be used must contain zero coefficients. The pipeline delay will then be that of a completely filled window.

TOTAL PIPELINE DELAY

The total pipeline delay is dependent on the device configuration and the number of devices in the system. Table 4 gives the delays obtained with the various single device configurations when the gain control is used. These delays are the the internal processing delays and do not include the delays needed to move a given size window completely into a field of interest. When multiple devices are needed, additional delays are produced which must be calculated for the particular application. These delays are discussed in the applications section.

The PDSP16488A contains facilities for outputing a delayed version of HRES to match any processing delay. Control register bits allow this delay to be selected from any value between 29 and 92 pixel clocks.

Function	Hex. Addr
Mode Reg A	00
Mode Reg B	01
Mode Reg C	02
Mode Reg D	03
Comparator LSB	04
Comparator MSB	05
Scale Value	06
Pixels / Line LSB	07
Pixels / Line MSB	08
C0 - C15	40 - 4F
C16 - C31	50 - 5F
C32 - C47	60 - 6F
C48 - C63	70 - 7F
Unused	09 - 3F

Table 3 Internal Register Addressing

Data size	Window Size	Pipeline Delay
8	4x4	34
8	8x4	30
8	8x8	26
16	4x4	28
16	8x4	26

Table 4 Pipe line dalays

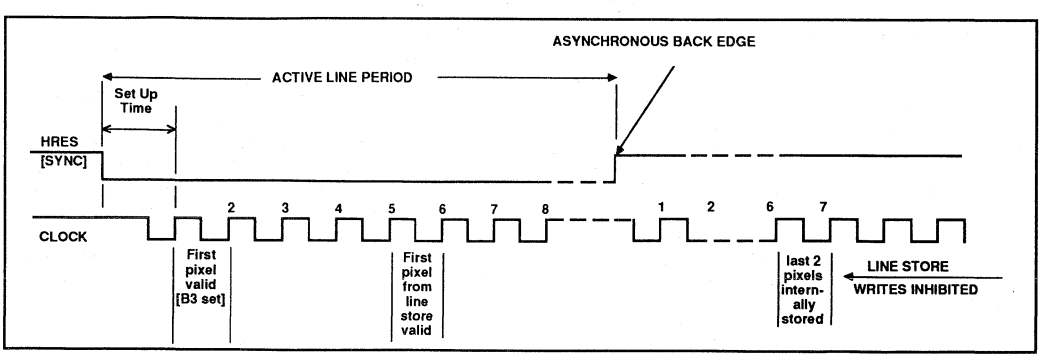
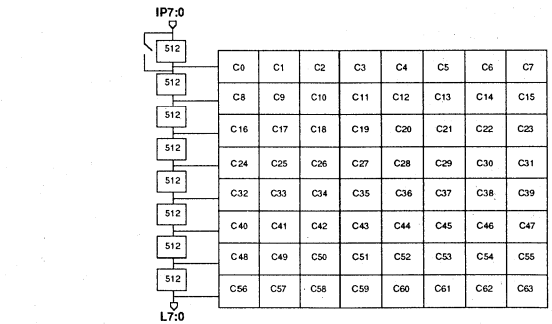
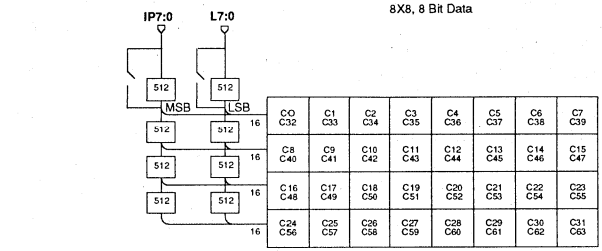


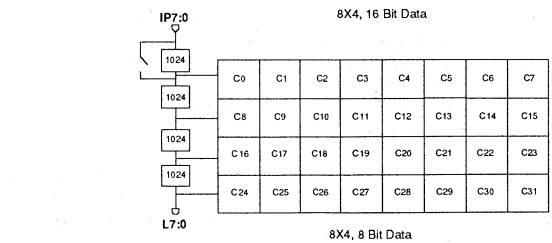
Fig.7 Pixel Input Delays



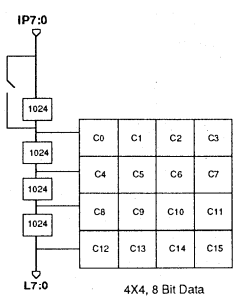
8X8, 8 Bit Data



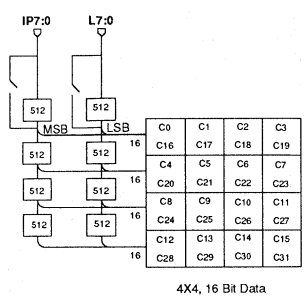
8X4, 16 Bit Data



8X4, 8 Bit Data



4X4, 8 Bit Data



4X4, 16 Bit Data

NOTE
Two coefficients occuring in the same box have identical values

Table 5 Physical Coefficient Position

LOADING REGISTERS FROM A HOST CPU

The expansion data inputs [X14:0] on a single or master device are connected to the host bus to provide address and data for the internal registers. In a multiple device system the remaining devices receive addresses and data which have been passed through the expansion connection between earlier devices in the cascade chain. Each device needs an individual chip enable plus a global data strobe, read/write line, and PROG signal from the host.

Registers are individually addressed and can be loaded in any sequence once the global PROG signal has been produced by the host. The latter would normally be produced from an address decode encompassing all the necessary device addresses.

If a self timed system is to be implemented, a timing strobe must be passed down the expansion chain through the PC1/PC0 connections. The PC0 output from the final device is used as a host REPLY signal, and indicates that the last device has received data after the propogation delay of previous devices. The timing strobe is produced in the MASTER device from the host data strobe, and will appear on the PC0 output. This feature allows the user to cascade any number of devices without knowing the propogation delay through each device. The timing information for this mode of operation is given in Figure 8.

The host can also read the data contained in the internal registers. The required device is selected using chip enable with the R/W line indicating a read operation. Single device systems output the data read on X7:0, but in multiple device systems data is read from the D7:0 outputs on the final device in the chain. These must be connected back to the host data bus through three-state drivers. When earlier devices in the chain are addressed, the register contents are transferred through the expansion connections down to the final device. In the self timed configuration the data will be valid when the REPLY goes active, as shown in Figure 8.

If the REPLY signal is not to be used , the PC0/PC1 connections are not necessary, and the host data strobe for a write operation must be wide enough to allow for the worst case propogation delay through all the devices (TDEL). If the data or address from the host does not meet the set up time given in Fugure 8, the width of the data strobe can be simply extended to compensate for the additional delay. When reading data the access time required is: TACC + (N - 1).TDEL using the maximum times obtained from Figure 8.

HOST CONTROL LINES

X7:0 — 8 bit data bus. In a single device system this bus is bi-directional; in other configurations it is an input. Only a SINGLE or MASTER device is connected directly to the host. Other devices receive data from the output of the previous device in the chain.

X14:8 — 7 bit address bus which is used to identify one of the 73 internal registers. Connected in the same manner as X7:0.

X15 — X15 must be open circuit on the MASTER device

PC0 — An input from the previous PC1 output in a multiple device chain. Not needed on a SINGLE device or if the self timed feature is not used.

PC1 — Reply to the host from a SINGLE device or from the last device in a cascade chain. It indicates that the write strobe can be terminated. Connected to PC0 input of the next device at intermediate points in the chain if the self timed feature is used.

R/W — Read/Not Write line from the host CPU which is connected to all devices in the system.

CE — An active low enable which is normally produced from a global address decode for the particular device. This must encompass all internal register addresses.

DS — An active low host data strobe which is connected to all devices. in the system.

PROG — An active low global signal, produced by the host, which is connected to all devices in the system. Together with a unique chip enable for every device, it allows the internal registers to be updated or examined by the host. PROG and CE should be tied together in a single device system.

LOADING REGISTERS FROM AN EPROM

In the EPROM supported mode, one device has to assume the role of a host computer. If more than one device is present, this must be the first component in the chain, which must have its MASTER pin tied low.

The MASTER device contains internal address counters which allow the registers in up to 16 cascaded devices to be specified. It also generates the PROG signal and a data strobe on the pins which were previously inputs. These outputs must be connected to the other devices in the system, which still use them as inputs. The R/W input should be tied low on all devices.

The width of the data strobe is determined by the feedback connection from the PC1 output on the last device to the PC0 input on the MASTER. The PC0/PC1 connections must be made between devices in a multiple device system; in a single device system the connection is made internally.

The available EPROM access time is determined by an internal oscillator and does not require the pixel clock to be present during the programming sequence. Any pixel clock re-synchronization in a real time system will thus not effect the coefficient load operation. The relevent EPROM timing information is shown in figure 9.

The load procedure will commence after reset has gone from active to in-active, and will be indicated by the PROG output going active. The data from 73 EPROM locations will be loaded into the internal registers using addresses corresponding to those in Table 3. Within a particular page of 128 EPROM locations, the first nine locations supply control register information, and the top 64 supply coefficients. The middle 55 locations are not used. If the window size is 8 x 4, the top 32 locations will also contain redundant data, and if the size is 4 x 4 the top 48 will be redundant.

In a multiple device system the load sequence will be repeated for every device, and four additional address bits will be generated on the CS3:0 pins. These address bits provide the EPROM with a page address, with one page allocated to each device in the system. Within each page only 73 locations provide data for a convolver, the remainder are redundant as in the single device system. The CS3:0 outputs must also be decoded in order to provide individual chip enables for each device. These can readily be derived by using an AS138 TTL decoder. Bits in an internal control register determine the number of times that the sequence is repeated.

If changes to the convolver operation are to be made after power-on, activating the CE input on the MASTER or SINGLE device will instigate the load procedure. Additional EPROM address bits supplied from the system will allow different filter coefficients to be used.

EPROM CONTROL LINES

X7:0 — 8 bit data from the EPROM to the MASTER or SINGLE device. Otherwise data is received from the previous device in the chain.

X14:8 — Lower 7 address bits to the EPROM from a MASTER or SINGLE device. Otherwise an input from the data outs of the previous device.

X15 — Tied to ground on a MASTER device to indicate the EPROM mode.

R/W — Tied low on all devices.

DS — An output from a MASTER or SINGLE device which provides a data strobe for the other devices.

CS3: 0 — Four additional address bits for the EPROM which are provided by the MASTER device. They allow 16 additional devices to be used and must be externally decoded to provide chip enables.

PC0 — An input on the MASTER device which is driven from the PC1 output of the last device in the chain. Used internally to terminate the write strobe. Connected to previous PC1 outputs at intermediate points in the chain. Not needed for a SINGLE device.

PC1 — An output connected to the PC0 input of the next device in the chain. The last device feeds back to the MASTER. Not needed for a SINGLE device.

CE — An enable which is produced by decoding CS3:0 from the MASTER. It is not needed for a MASTER or SINGLE device which will always use the bottom block of addresses with internally generated write strobes. It can however be used on these devices to initiate a new load procedure after the initial power on sequence.

PROG — An active low going signal produced by an EPROM supported MASTER or SINGLE device. An input to all other devices. It indicates that a register load sequence is occuring, either after power on, or as the result of CE as explained above. It remains active until register 73 in the final device has been loaded. Four bits in a control register define the number of cascaded devices.

SYSTEM CONFIGURATION

The device is configured using a combination of the state of the SINGLE and MASTER pins, and the contents of the four Mode Control registers. In a MASTER or SINGLE device the state of the X15 pin is used to define whether the system is EPROM or host supported.

MODE CONTROL REGISTERS

REGISTER A Bit Allocation

BIT	CODE	FUNCTION
3:0	XXXX	Number of extra devices from1-15
6:4	000	8 bit, 8x8 window, 10MHz max, 8x512 line delays.
6:4	001	16 bit, 8x4 window, 10MHz max, 4x512 line delays.
6:4	010	16 bit, 4x4 window, 20MHz max, 4x512 line delays.
6:4	011	8 bit, 8x4 window, 20MHz max, 4x1024 line delays.
6:4	101	8 bit, 4x4 window, 40MHz max, 4x1024 line delays
7	0	Multiplexed exp. data
7	1	Non-mux. exp. data

BITS 3:0 — These bits are 'don't care' when using a host computer but to a MASTER device, in an EPROM supported system, they define the number of interconnected chips. The EPROM must contain contiguous 128 byte blocks for each of the devices in the system and a 4 bit counter in the MASTER device will sequence through up to 16 block reads. An internal comparator in the MASTER causes the loading of the internal registers to cease when the value in the counter equals that contained in these bits. The bits are redundant in a SINGLE device which only uses one 128 byte block.

BITS 6:4 — These bits define one of the five basic configurations. The line delays will automatically be configured to match the chosen window size and pixel accuracy. The maximum clock rate that is available to the user reflects the internal mutiplication factor.

BIT 7 This bit must be set if the pixel clock is greater than 20MHz. It disables the output and input time multiplexing, and instead outputs the least significant half of the 32 bit intermediate sum for the complete clock cycle. When the gain control is used, the output multiplexing will automatically be disabled.

REGISTER B Bit Allocation

BIT	CODE	FUNCTION
0	0	Second line delay group fed from the first group
0	1	Second line delay group fed from L7:0 which become inputs
2:1	00	Store pixels to end of line
2:1	01	Store pixels till count is reached
2:1	10	Frame store operation
2:1	11	Not Used
3	0	No delays on pixel inputs
3	1	4 delays on both pixel inputs
4	0	Use expansion adder
4	1	Expansion adder disabled
6:5		Not used
7	0	Use first delay in second group
7	1	Bypass first delay in second group

BIT 0 This bit defines the input for the second group of line delays. It must be set in the 16 bit pixel modes, and is set by power on reset.

BIT 2:1 These bits control the mode of operation of the line stores. In real time systems pixels can be stored either until HRES [SYNC] goes active , or until a pre-determined count is reached. In the frame store mode line store operations are continuous, with a pre-determined line length.

BIT 3 When this bit is set four pipeline delays are added to the pixel inputs to compensate for the internal/ external delays between line stores. The extra delay is only necessary when a device supplied with system video in which the first pixel in a line is valid in the period following the first active clock edge. See Fig 7. The delay is not necessary if the device is fed from the output of another convolver. When set this bit will add four additional delays to those defined by Register D, bits 4: 2.

BIT 4 When this bit is set the expansion adder will not be used. It is automatically set in a MASTER or SINGLE device.

BIT 7 This bit controls the bypass option on the first line delay on the L7:0 inputs. It is only effective when an 8 bit pixel mode is selected, which also needs more than four line delays. When L7:0 are used as outputs it should always be reset. In the 16 bit modes the bypass function is only controlled by the BYPASS pin, and the bit is redundant.

REGISTER C Bit Allocation

BIT	CODE	FUNCTION
0	0	Field selection defined by C5:4
0	1	Automatic field selection
3:1	000	DELOP = 29 + 0 clks
3:1	001	DELOP = 29 + 8 clks
3:1	010	DELOP = 29 + 16 clks
3:1	011	DELOP = 29 + 24 clks
3:1	100	DELOP = 29 + 32 clks
3:1	101	DELOP = 29 + 40 clks
3:1	110	DELOP = 29 + 48 clks
3:1	111	DELOP = 29 + 56 clks
5:4	00	Select upper 20 bits
5:4	01	Select next 20 bits
5:4	10	Select next 20 bits
5:4	11	Select bottom 20 bits
7:6	00	By-pass the gain control
7:6	01	Normal gain control O/P
7:6	10	Saturate at max + and -ve values.
7:6	11	Force -ve to zero.Sat.+ve values.

BIT 0 If this bit is set, the 20 bit field selected from the 32 bit result, is defined automatically by internal logic.

BITS 3:1 These bits are in conjunction with Register D, bits 7:5 to define the pixel delay from the HRES input to the DELOP pin. They are used to match the appropriate processing delay in a particular system. The minimum delay is 29 pixel clocks.

BITS 5:4 These bits define which of the four 20 bit fields out of the 32 bit final result is selected as the input to the gain control. They are redundant when the gain control is not used, or if Register C, bit0, is set.

BITS 7:6 These bits define the use of the gain control as given in the table. Intermediate devices in a multiple device system MUST by-pass the gain control, otherwise the additional pipeline delays will effect the result. Disabling the scaler will reduce the device pipeline by 13 PCLK cycles from the delays shown in Table 4.

REGISTER D Bit Allocation

BIT	CODE	FUNCTION
0	0	X15:0 Not delayed
0	1	X15:0 Delayed
1	0	Internal sum not shifted
1	1	Internal sum multiplied by 256
3:2	00	I/P to line stores not delayed
3:2	01	I/P to line stores delayed by 4
3:2	10	I/P to line stores delayed by 8
3:2	11	I/P to line stores delayed by 12
4	0	Un-signed pixel data input
4	1	2's complement pixel data input
7:5	XXX	Add 0 to 7 clock delays to DELOP output.

BIT 0 If this bit is set the expansion data input is delayed by four pixel clocks before it is added to the present convolver output. It is used in multiple device systems when the partial window width is 8 pixels.

BIT 1 When this bit is set the internal sum is shifted to the left by 8 places before being added to the expansion input. It is used when two devices are used, each in an 8 bit pixel mode, to fabricate a 16 bit pixel mode.

BITS 3::2 These bits define the delays on both sets of pixel inputs before entering the line stores. The delays are always identical on both sets.

BIT 4 When this bit is set the convolver interprets 8 or 16 bit pixels as 2's complement signed numbers

BIT 7:5 These bits add 0 to 7 additional clock delays to those selected by Register C, bits 3:1.

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage Vcc	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to Vcc + 0.5V
Output voltage V_{OUT}	-0.5V to Vcc + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HMB)	500V
Storage temperature T_s	-65°C to 150°C
Max. junction temperature	
commercial	100°C
industrial	110°C
Package power dissipation	3000mW
Thermal resistances, junction to case $ø_{JC}$	5°C/W
Device power dissipation	2000mW

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.

ELECTRICAL CHARACTERISTICS

Operating Conditions

Commercial: T_{amb} = 0°C to +70°C, T_{JMAX} = 95°C, V_{CC} = 5.0V ± 5%, ground = 0V

Industrial: T_{amb} = -40°C to +85C, T_{JMAX} = 110°C, V_{CC} = 5.0V ± 10, ground = 0V

Military : T_{amb} = -55°C to +125°C, T_{JMAX} = 150°C, V_{CC} = 5.0V ± 10%, ground = 0V

NOTE: Signal pins PROG, PC0, X15, MASTER, SINGLE, DS and 0V have pull-up resistors in the range 15kΩ to 200kΩ. BYPASS has no internal pull-up resistor.

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.0		-	V	
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{CC}.no internal pull up
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{CC}.no internal pull up
Output S/C current	I_{SC}	10		300	mA	V_{CC} = Max

Characteristic	Symbol	Value		Units	Notes
		Min.	Max.		
DS Hold Time after REPLY active	T_{DSH}	20		ns	Only applicable for read ops & if $\overline{REPLY}$ is used.
Host Address/data Set Up Time	T_{HSU}	0		ns	Only applicable if $\overline{REPLY}$ is used. Otherwise time is referenced to risng edge of strobe when set up must be N xTDEL, for Ndevices
Read Set UpTime to prevent Write	T_{RA}	5		ns	
Host Signal Hold Time	T_{HH}	10		ns	Must always be guaranteed.
Expansion in to Data Out in $\overline{PROG}$ mode	T_{DEL}		30	ns	No clocks are needed in $\overline{PROG}$ mode
Delay from strobe to $\overline{PC1}$ [Equivalent to $\overline{PC0}$ to $\overline{PC1}$ delay]	T_{EXP}		50	ns	Greater than TDEL under all conditions
Chip Enable Set Up Time	T_{CSU}	0		ns	
$\overline{PROG}$ Set Up Time	T_{PSU}	0		ns	
$\overline{PROG}$ Hold Time	T_{PH}	0			
Chip Enable Hold Time	T_{CH}	0			
$\overline{PC1}$ In-active Delay after $\overline{DS}$ in-active	T_{PCH}		50	ns	Defines Data Strobe in-active time
Coefficient Read Time	T_{ACC}		50	ns	From MASTER or SINGLE device
Coefficients valid Time before $\overline{REPLY}$	T_{RSU}	5		ns	

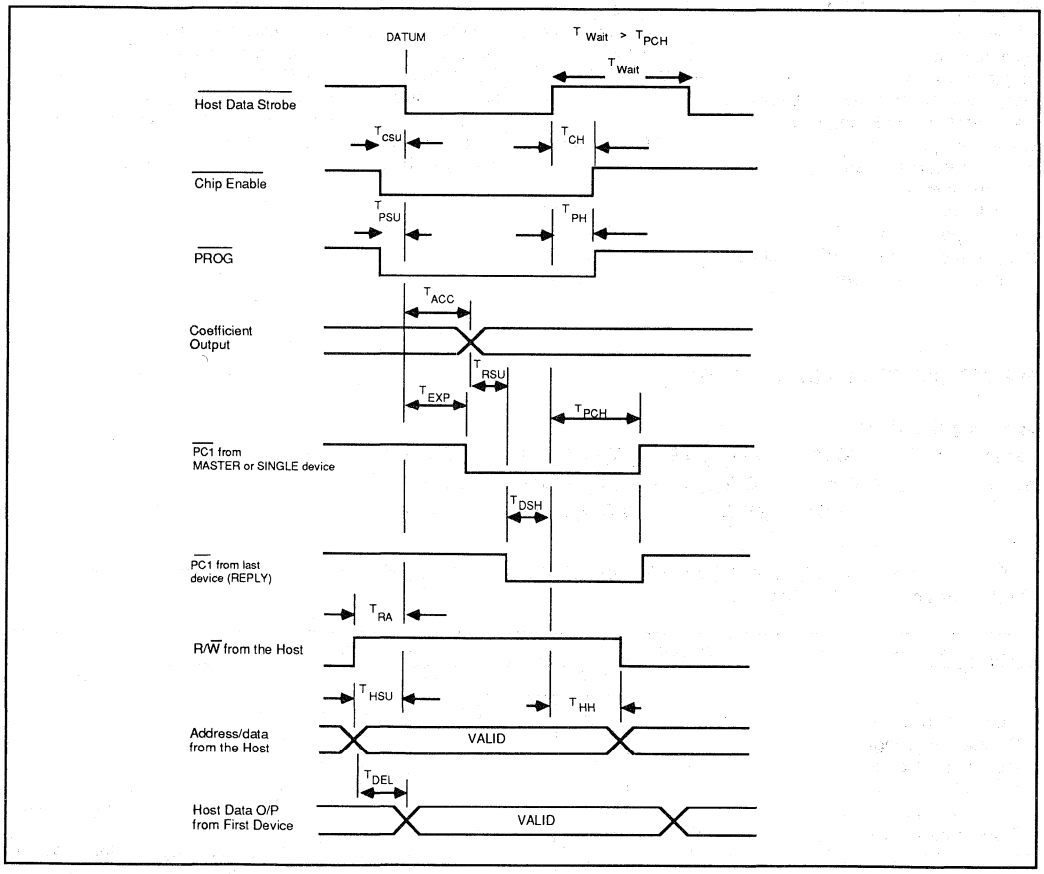


FIG. 8. Host Timing

Characteristic	Symbol	Value		Units	Notes
		Min.	Max.		
Delay from Data Strobe to MASTER $\overline{PC1}$	T_{PCD}		50	ns	
Delay from $\overline{PC0}$ Input to Write in-active	T_{WH}	5		ns	
$\overline{PC1}$ In-Active Delay	T_{PCH}		50	ns	
Write from $\overline{MASTER}$ In-Active	T_{WW}	250		ns	
Write In-Active to new Address	T_{AD}		30	ns	
EPROM Data Set Up Time	T_{DS}	20		ns	
Data Strobe from MASTER	T_{RW}	10		ns	Single device
Chip Enable Set Up Time	T_{CSU}	0		ns	
Chip Enable Hold Time	T_{CH}	0		ns	
Availible EPROM Access Time	T_{DA}	200		ns	
Expansion In to Data Out	T_{DEL}		30	ns	
$\overline{PC0}$ to $\overline{PC1}$ Delay	T_{EXP}		50	ns	Greater than T_{DEL} at all temps

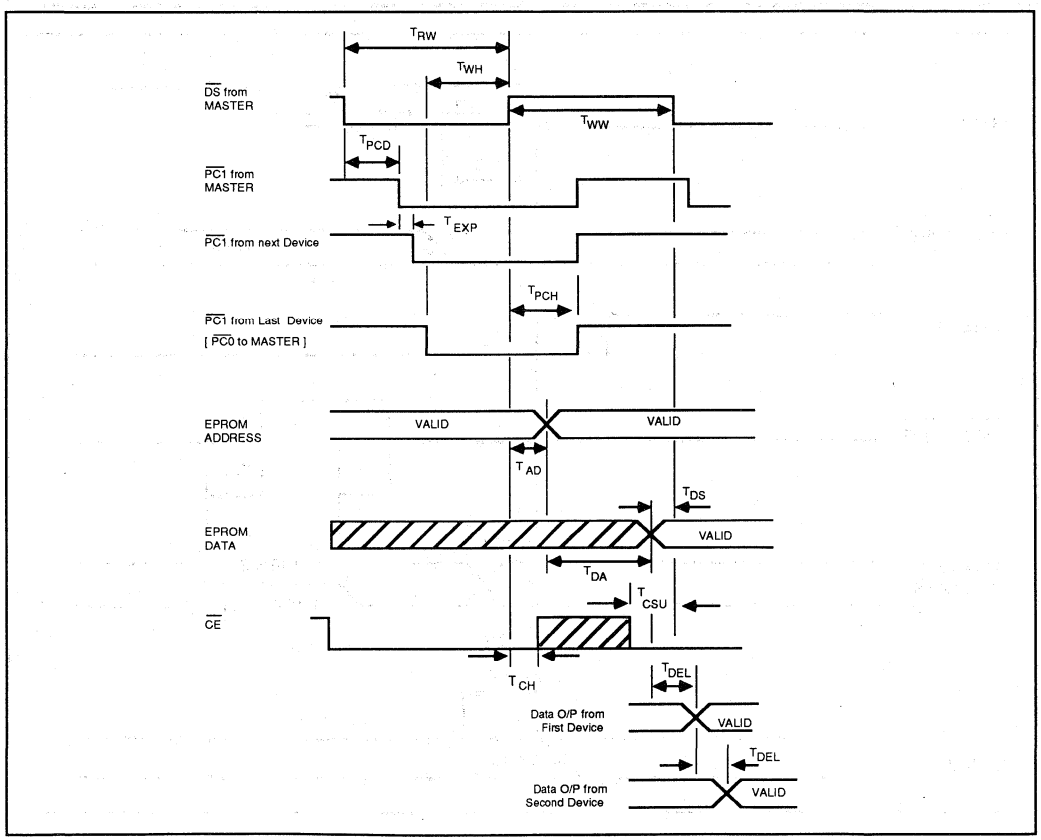


Fig. 9. EPROM Timing

Characteristic	Symbol	Value		Units	Notes
		Min.	Max.		
Pixel Clock Low Time	T_{CL}	25 (a) 10 (b)		ns ns	(a) 32 Bit Muxed Output (b) 16 Bit Output
Pixel Clock High Time	T_{CH}	25 (a) 10 (b)			(a) 32 Bit Muxed Output (b) 16 Bit Output
Data in Set Up Time	T_{DSU}	10		ns	
Data in Hold Time	T_{DH}	0		ns	
CLK rising to Output delay	T_{RD}		21	ns	Increase to 40ns for DELOP output
Line Store Output Delay	T_{LD}		20	ns	
HRES In-active Set Up Time	T_{RSU}	10		ns	
$\overline{\text{Output Enable}}$ Time	T_{DLZ}		15	ns	} Measured with a 15kΩ series resistor and 30pF load capacitance
Output Disable Time	T_{DHZ}		15	ns	

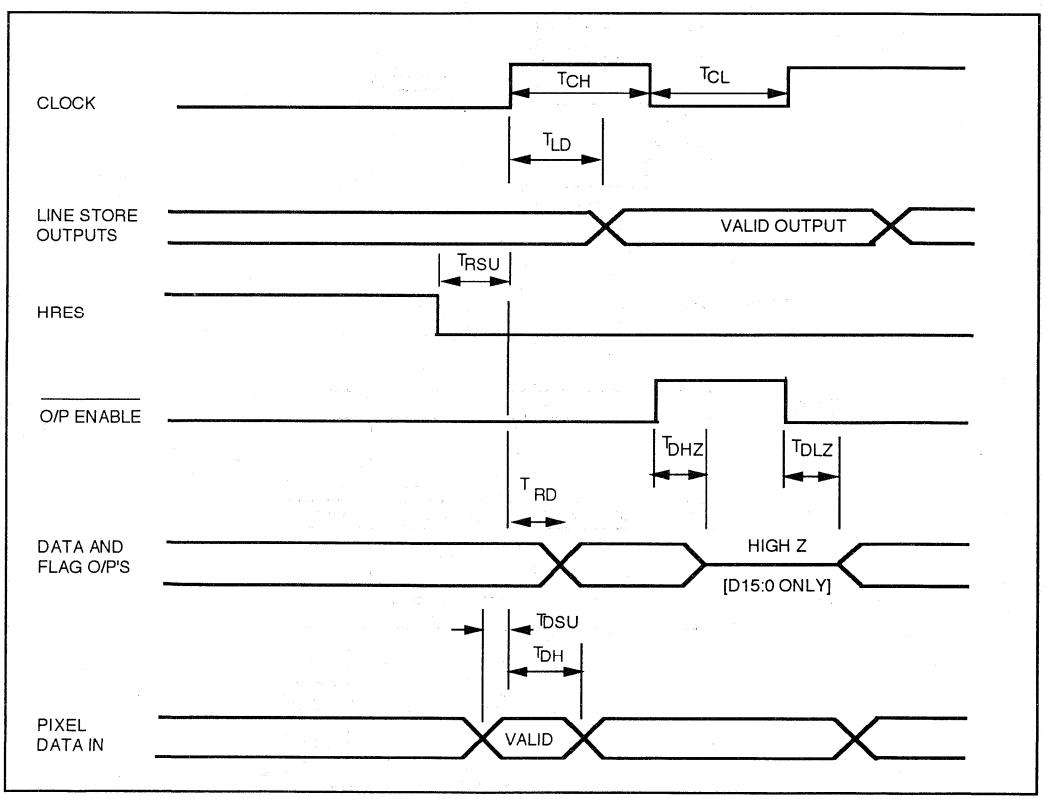


Fig. 10. I/O Timing

APPLICATIONS INFORMATION

DEVICE REQUIREMENTS

The number of devices required to implement a given convolver window depends on the size of the window, the required pixel rate, and whether the pixel accuracy is to be 8 or 16 bits. In practice the PDSP16488A supports windows requiring one, two, four, six, or eight devices without additional logic. Table 2 gives typical window sizes which may be obtained with the above number of devices.

Figures 11 through 18 show system interconnections for these arrangements. Other configurations are possible but may need the support of additional pixel/line delays and/or expansion adders. Although not necessarily shown, all configurations can be supported by either an EPROM or a Host Computer . Interlaced or non-interlaced video may also be used, unless explicitly stated otherwise in the text.

Expansion with 8 bit pixels is a straightforward process and the number of devices needed is easily deduced from the window sizes available in a single device. At pixel rates above 20MHz it may not be practical to use more than four devices. since the full 32 bit intermediate precision is not available. The lack of expansion multiplexing reduces the intermediate precision to 16 bits. The partial sum outputs must thus not overflow these 16 bits; this will require the coefficients to be scaled down appropriately with a resulting loss in accuracy.

Expansion with 16 bit pixels can be achieved in several ways. The simplest way is to use two devices, each working with 8 bit pixels. One device handles the least significant part of the data, and its output feeds the expansion input of a second device. This performs the most significant half of the calculation. The least significant half is then added to the most significant sum, after the latter has been multiplied by 256 ie shifted by eight places. This shift is done internally and controlled by Register D, bit 1. The internal 32 bit accuracy prevents any loss in precision due the shift and add operation.

The window size with this arrangement is restricted to that available in a single device, at the required pixel rate but with 8 bit pixels. Thus two devices can be used , for example, to provide an 8 x 8 window with 16 bit pixels and 10 MHz rates.

If a larger extended precision window is needed, it is possible to use four devices. Each device is then programmed to be in a 16 bit data mode, but should be restricted to rates below 20 MHz, if the 32 bit intermediate precision is to be maintained. In the 16 bit modes, however, the output from the last line delay is not available due to pin limitations. This is not a problem in a four device interlaced system, since half of the devices will be fed from an external field delay. In non interlaced systems additional external line delays would be needed. An alternative approach would be to configure all the devices in the appropriate 8 bit mode, do separate least significant and most significant calculations, and then combine the results in an external adder after a wired in shift.

SINGLE DEVICE SYSTEMS

Figures 11 illustrates both EPROM and Host supported single device systems, with or without interlaced video. In both cases the SINGLE and X15 pins must be tied tied low, and the PC0, PC1, and DS pins are redundant. The PROG pin becomes an output and indicates that a register load sequence is occuring. The first line delay must always be bypassed in a non interlaced system, however, since an internal pull up is not provided, the BYPASS pin should be tied to VCC for the correct operation. With interlaced video the BYPASS input is used to distinguish between the odd and even fields.

The CE input may be left open circuit if coefficients are to be simply loaded after a power on reset signal; the latter being applied to the RES input. Alternatively the CE input may be used to change the coefficients at any time after power on reset; the EPROM would then need additional address bits for the extra sets of coefficients that are to be stored.

In an interlaced system the pixels from the previous field must use the IP7:0 inputs, and the live pixels must use the L7:0 inputs. Interlaced sysytems requiring extended precision pixels are non supported with a single device, since the L7:0 inputs are then use for the least significant 8 bits, and the IP7:0 inputs for any more significant bits.

If the X15 pin is left open circuit, an internal pull up will configure the device in the host supported mode. The host must then supply a data strobe and a R/W control line. The X7:0 pins must be connected to the host data bus, and are used to both load and read back register values. The PROG and CE pins may be connected together, and then driven by a host address decode. The output on PC1, which provides a REPLY to the host, need not be used if the width of the data strobe is greater than the maximum TEXP value given in Figure 7.

The configuration bits 6:4 in REGISTER A define the window size, maximum pixel rate, and pixel resolution. Window sizes smaller than the maximum in any configuration are implemented by filling in the window with `zero' coefficients. Bits 3:0 are irrelevent in the SINGLE mode, as is bit 7 if the gain contol is used.

The result would be expected to lie in either the bottom 20 bits of the 32 bit result , or possibly in the next 20 bit field displaced by four bits. Register C, bits 5:4, must thus select one of these fields for subsequent use by the gain control. The gain is then adjusted such that the 16 outputs available on pins are in fact the 16 most significant bits of the result. The gain needed is application specific, but if too much gain is used the OV pin will indicate an overflow.

Register B, bits 2:1, must be set to select the required method of defining the length of the line delays, and the use of bit 3 is dependent on any external pixel delays before the convolver input. No additional delays are needed on the pixel inputs in a single device system, and REGISTER D, bits 4:2, should be reset. The pipeline delay in the DELOP output path should match one of those in Table 4, and is window size dependent.

DUAL DEVICE CONFIGURATIONS

Two devices, each configured with 8 bit pixels and 8W x 4D windows, can be used to provide an 8 x 8 window at up to 20 MHz pixel rates. Figure 12 shows both the non interlaced and interlaced arrangements.

Video lines containing up to 1024 pixels are possible in both configurations, since each device only needs four line delays. One device is configured as the MASTER by grounding the MASTER pin; the other then receives control signals in

the normal way and has its MASTER and SINGLE pins left open circuit.

The internal convolver sum, in the device producing the final result, must be delayed by 4 pixels to match the inherent delay in the expansion output from the other device. This is actually achieved by delaying the pixel inputs to the line stores [Register D bits 3:2 = 01]. No additional delay in the expansion input is needed, but the pipeline delay used to produce DELOP must be four clocks greater than that given in Table 4 for a single device. The DELOP output is redundant in one of the two devices.

Two devices can also be used to support systems requiring 16 bit pixels. With this approach the 16 x 8 multiplication is mechanized as two 8 x 8 operations, with the results added together after the most significant half has been shifted by 8 places to the most significant end. This shift operation is controlled by Register D, Bit 1. Both convolvers are programmed to contain the same coefficients. The convolved output can theoretically grow to 30 bits, and the appropriate field must be selected before using the gain control.

Examples of this operating mode are shown in Figure 13. Each device must be configured in the same 8 bit pixel operating mode, but the device producing the final result must use the 8 place shift option on its internal sum.

The least significant 8 bits of the pixel are connected to the MASTER device and the most significant 8 bits are connected to the device producing the final result.. The internal sum in this device must be delayed by four pixels to match the delay in the expansion output from the first device. This is actually achieved by delaying the pixel inputs to the line stores(Register D, bits 4:2, = 001]. The expansion input needs no additional delay [Register D bits 1:0 = 10].

The actual pixel precision can be any number of pixels between 8 and 16, and may be a signed or unsigned number. Any unused, more significant bits, must respectively be either sign extended or be tied low.

DELOP must have four additional pipeline delays in order to match the total processing delay. This output can be obtained from either device.

FOUR DEVICE SYSTEMS

Four devices, each in the 8x8 mode, can be used to provide a 16 x 16 window, with 8 bit pixel resolution and 10 MHz clock rates. The partial sum from the first device in each row must be delayed by eight pixel clocks before it is added to the result from the next device. This provides the eight pixel displacement to match the width of the window. The delay is actually provided by four additional delays in the expansion input to the next device, plus the inherent four clock delays in outputing results from the first device. Register D, Bit 0 controls the additional delay.

The internal convolver sums, in the two devices in the second row, must be delayed by 12 clocks before they are added to the result from the first row. This twelve clock delay is necessary because of the combination of the eight pixel horizontal displacement delay , and the four clock delay in outputing the result from the last device in the top row. It is actually achieved by delaying the pixel inputs to the line stores. (Register D, bits 3:2 = 11].

The DELOP output must have 20 delays additional to those in a single device. This compensates for the twelve delays added to the convolver sums in the second row, plus an additional eight delays to compensate for the partial width of the first device in the secind row.

Four devices can also be used to give an 8x8 window, but with a 30 MHz pixel clock. Each device is configured to provide a 4x4 partial window, but the maximum pixel rate is reduced from 40 to 30 MHz because of the response of the line delay expansion circuitry. Intermediate precision is restricted to 16 bits, since time multiplexed data outputs cannot be used above 20 MHz.

This configuration requires no additional delay in the expansion inputs, and the inputs to the line stores in both devices in the second row must be delayed by 8 clock cycles [Register D bits 3:2 = 10]. The DELOP output needs twelve additional clock delays to match the processing delay.

Figures 14 and 15 show non-interlaced and interlaced versions of the above 8 x 8 and 4 x 4 arrangements

Figure 16 shows how four devices can also be used to provide an 8x8 window, with 16 bit pixels and 20MHz clock rates. The expansion data from a previous device needs no additional delay since the partial window size in each device is only 4x4. The internal convolver sums from each device in the second row must be delayed by 8 Clks and the DELOP output must have 12 additional delays. If this arrangement is to be used in a non-interlaced application, the field store must be replaced by four line delays.

SIX DEVICE SYSTEMS

As shown in figure 17, six devices, each in an 8Wx4D mode using 8 bit pixels, can provide a 16W x 12D window at 20MHz clock rates. Expansion inputs from previous devices in a row [but not the first device in each row] need an extra 4 Clks of delay since the partial window is eight pixels wide. Internal convolver sums need a differential delay of 12 Clk cycles from row to row [Register D bits 3:2 = 11].

The DELOP output must have 32 additional delays to match the total processing delay.

EIGHT DEVICE SYSTEMS

Two additional chips will extend the above six device configuration to a 16 x 16 window. Internal convolver sums must have differential delays of 12 clock cycles between rows, as in the six device system. The DELOP output needs 44 additional clock delays.

NINE DEVICE SYSTEMS

Nine devices each in the 8 x 8 mode will provide a 24 x 24 window with 8 bit data and 10 MHz pixel clocks. This is shown in Figure 18. Expansion data inputs from previous devices in a row [but not the first device in each row] need an extra 4 Clks of delay. The internal convolver sums need differential delays of 20 Clk cycles between rows. Sixteen of the latter delays can be provided internally by setting Register B, bit3, and also Register D, bits 3:2. The four extra delays must be provided externally.

The DELOP output needs 56 clock delays in addition to the 29 required for the 8 x 8 single device configuration.

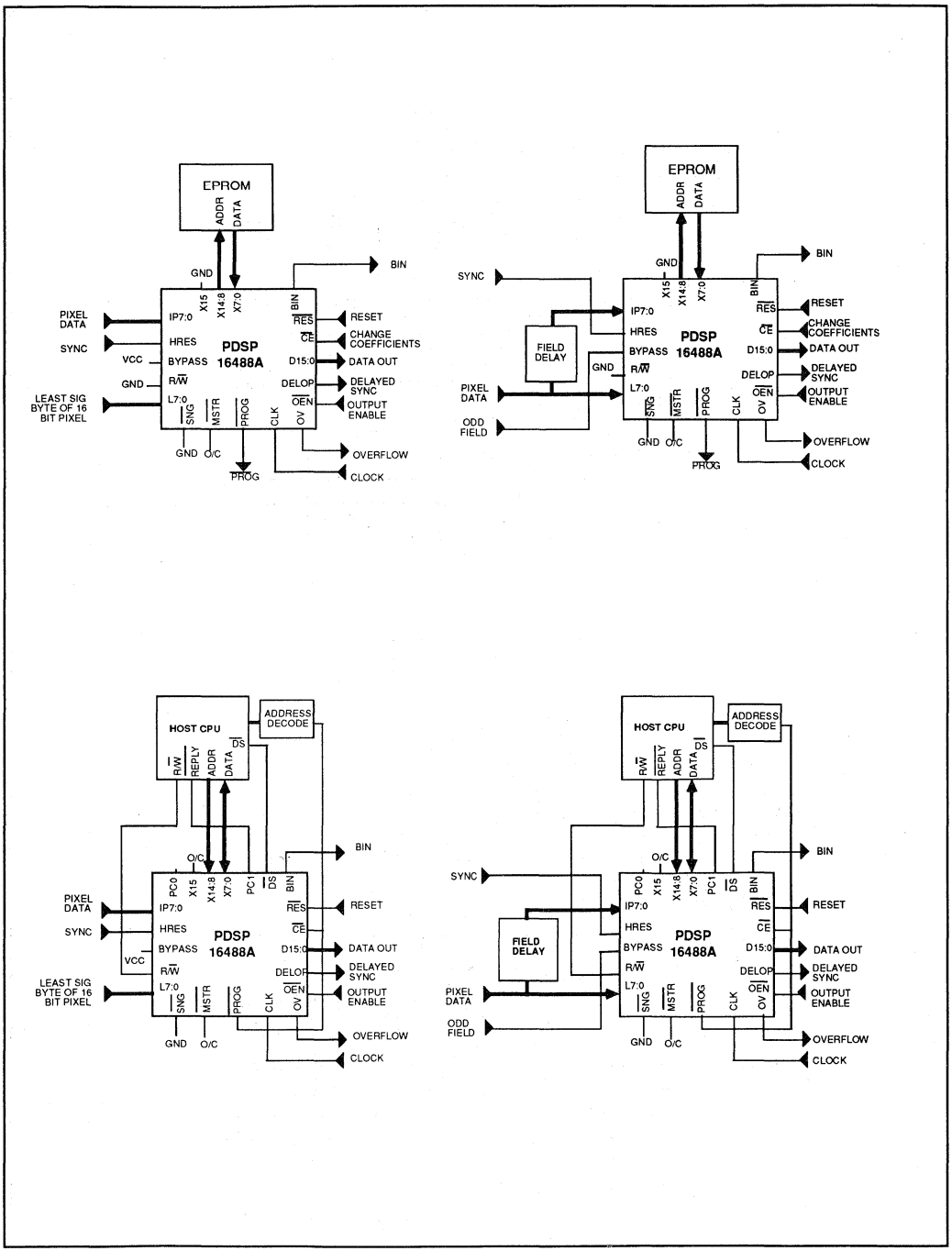


Figure 11 Single Device Systems

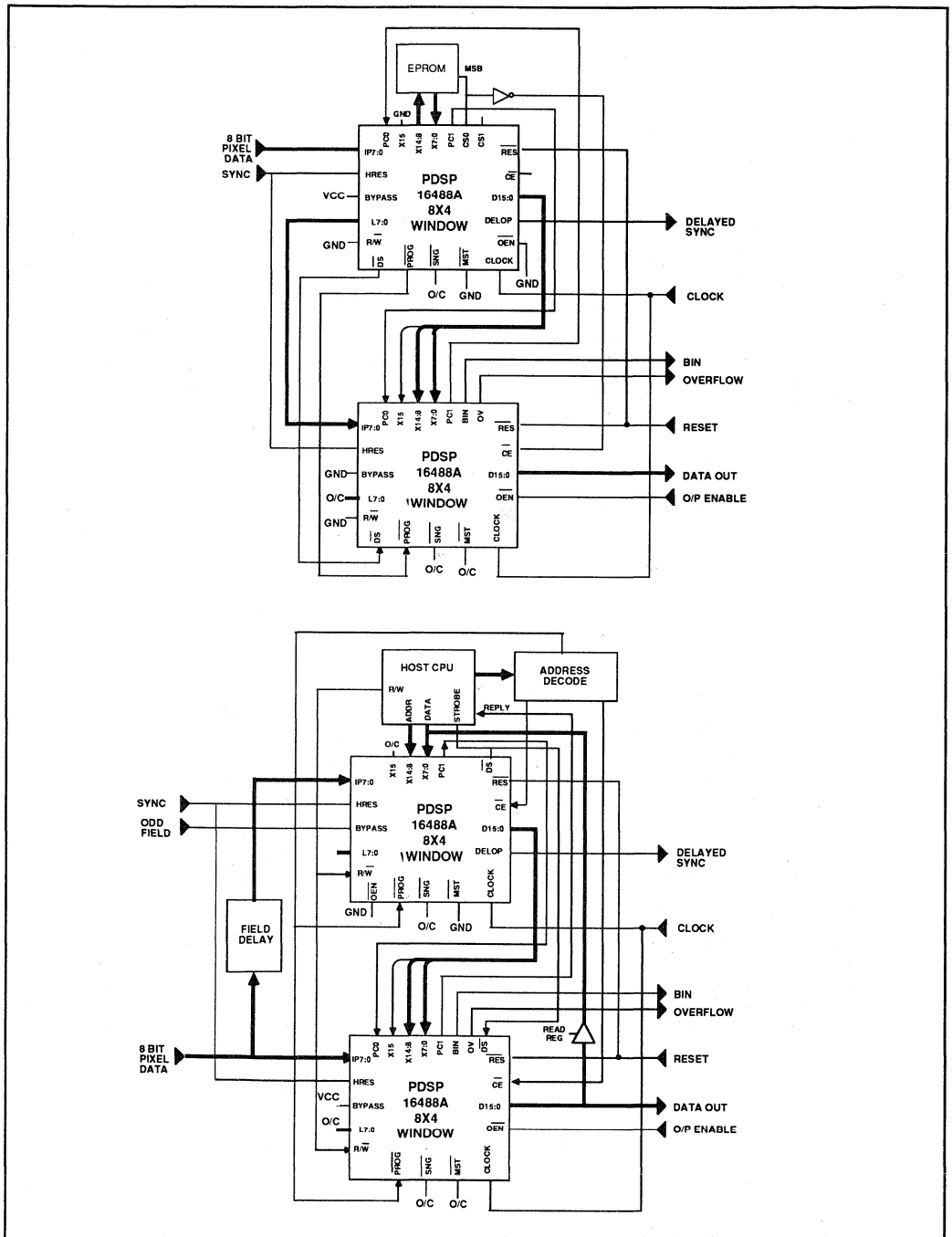


Figure 12. 8 Bit Dual Device Systems

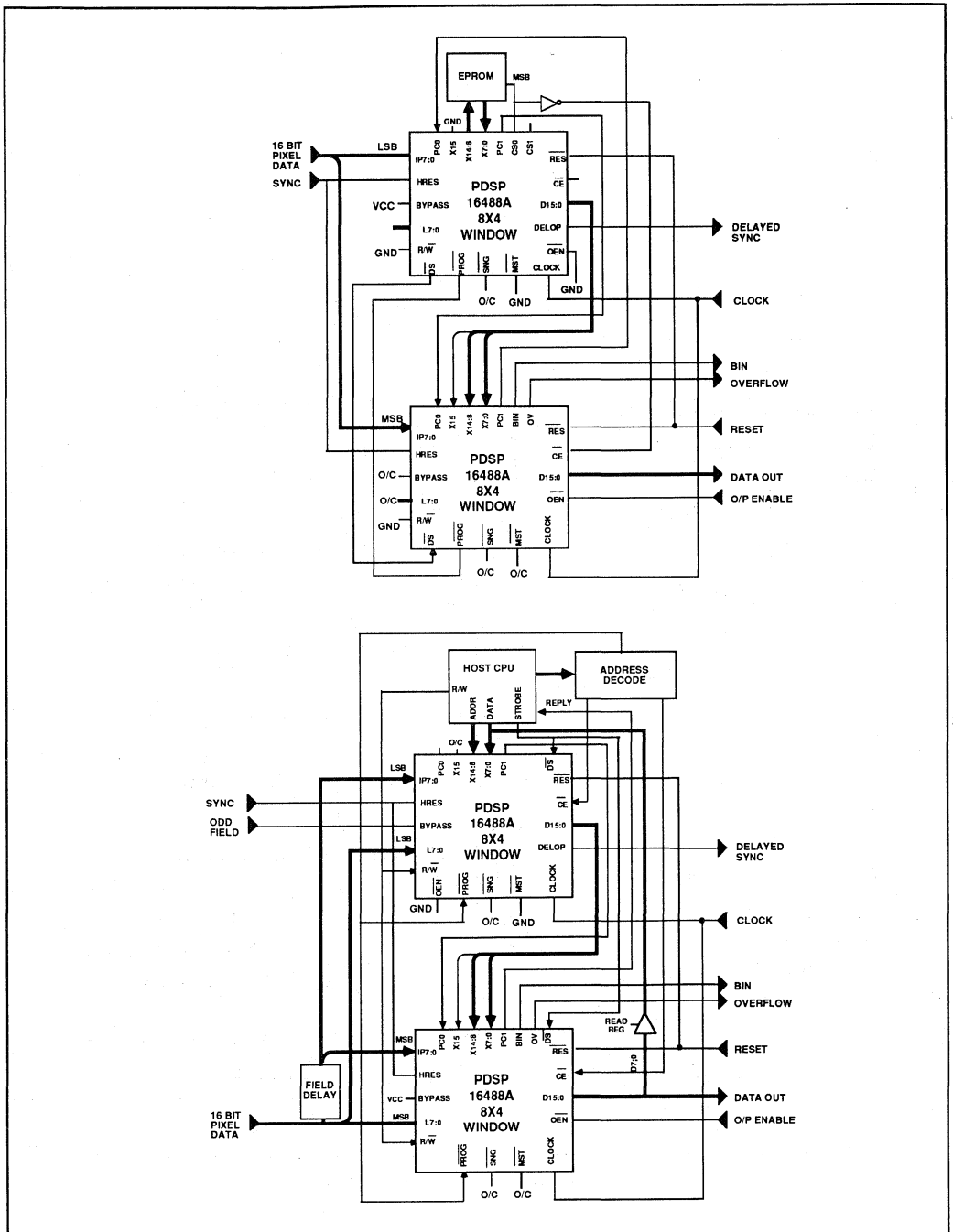


Figure 13. Dual Device 16 Bit Systems.

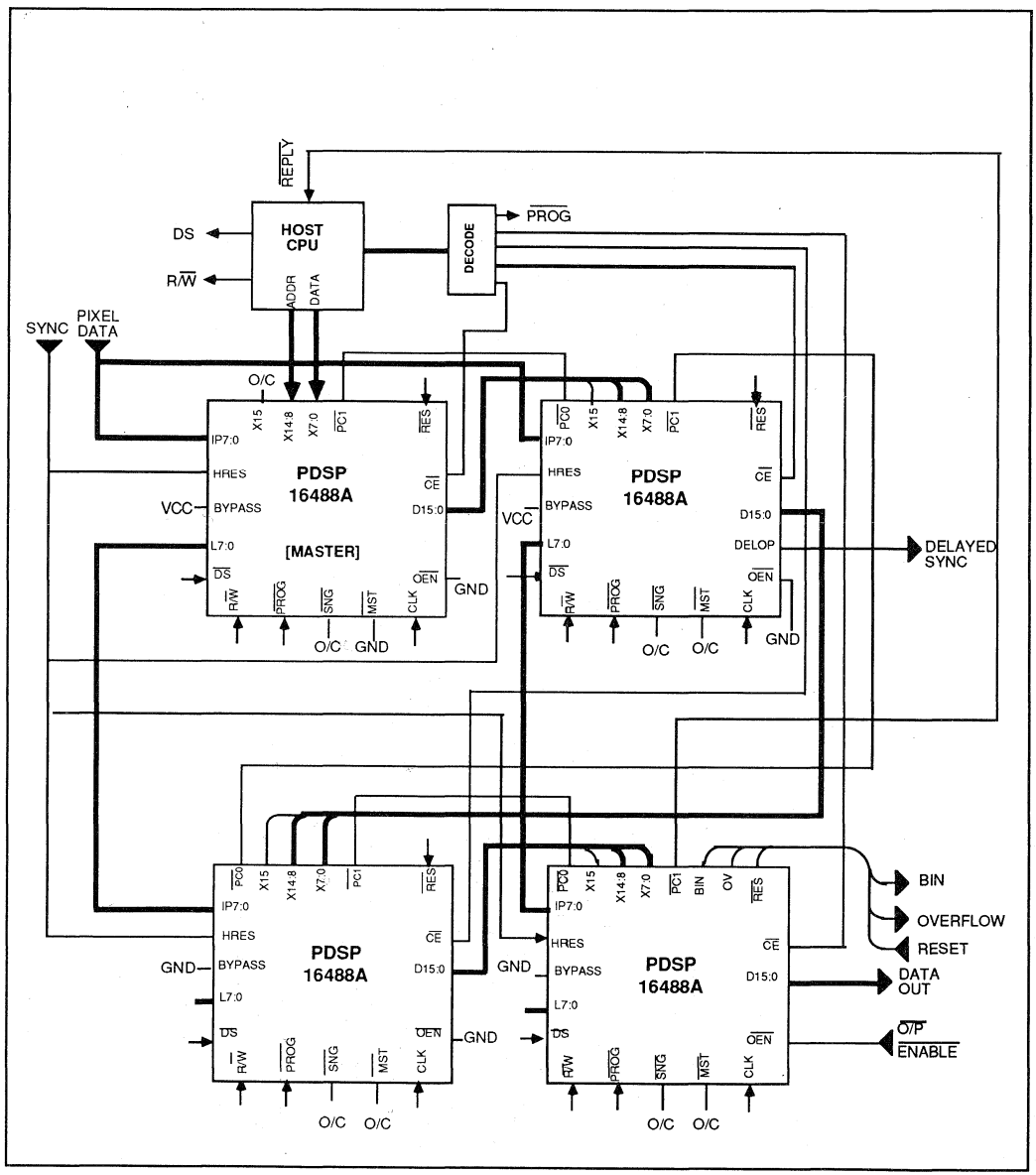


Figure 14. Four Device Non Interlaced System.

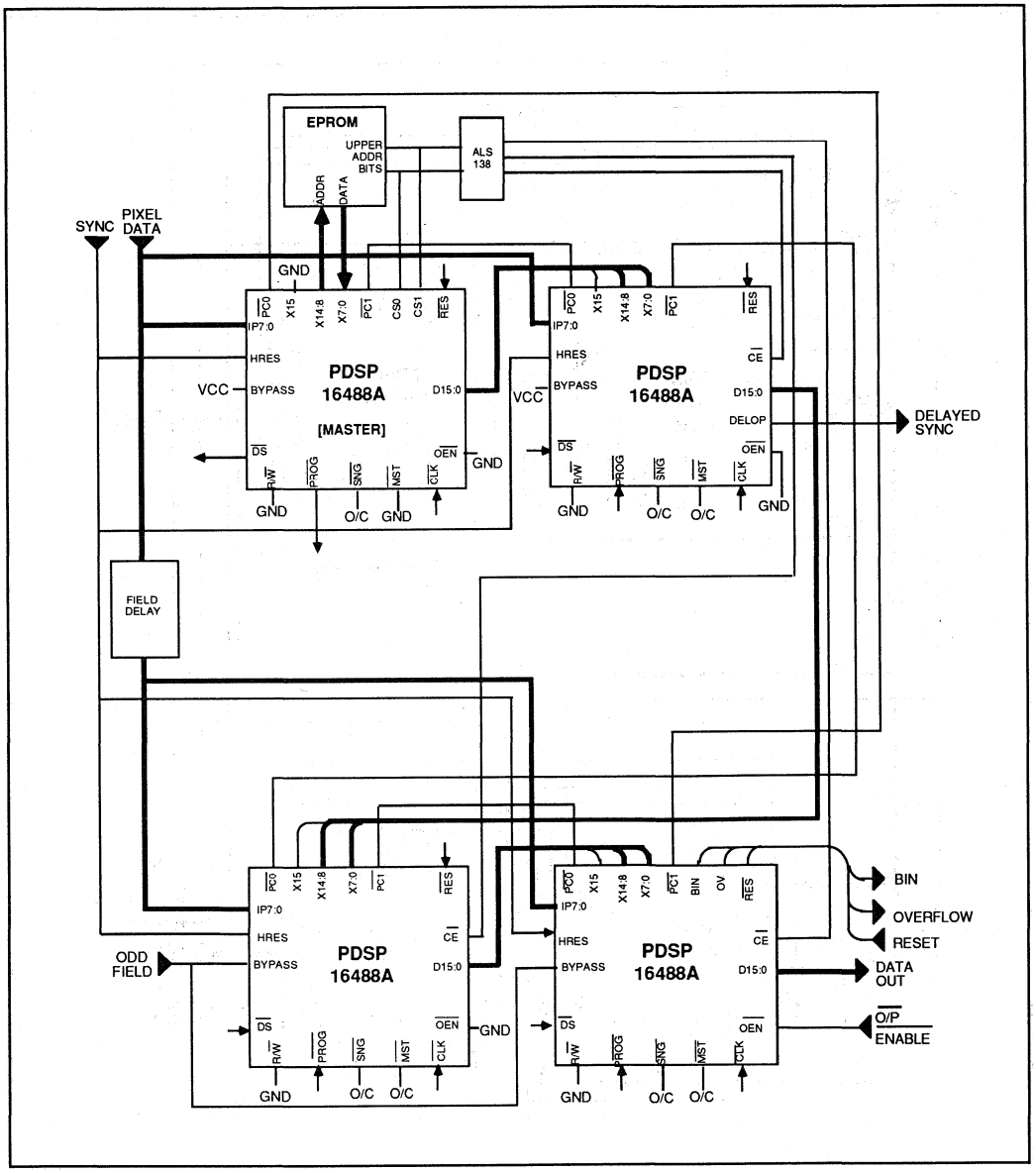


Figure 15. Four Device Interlaced System.

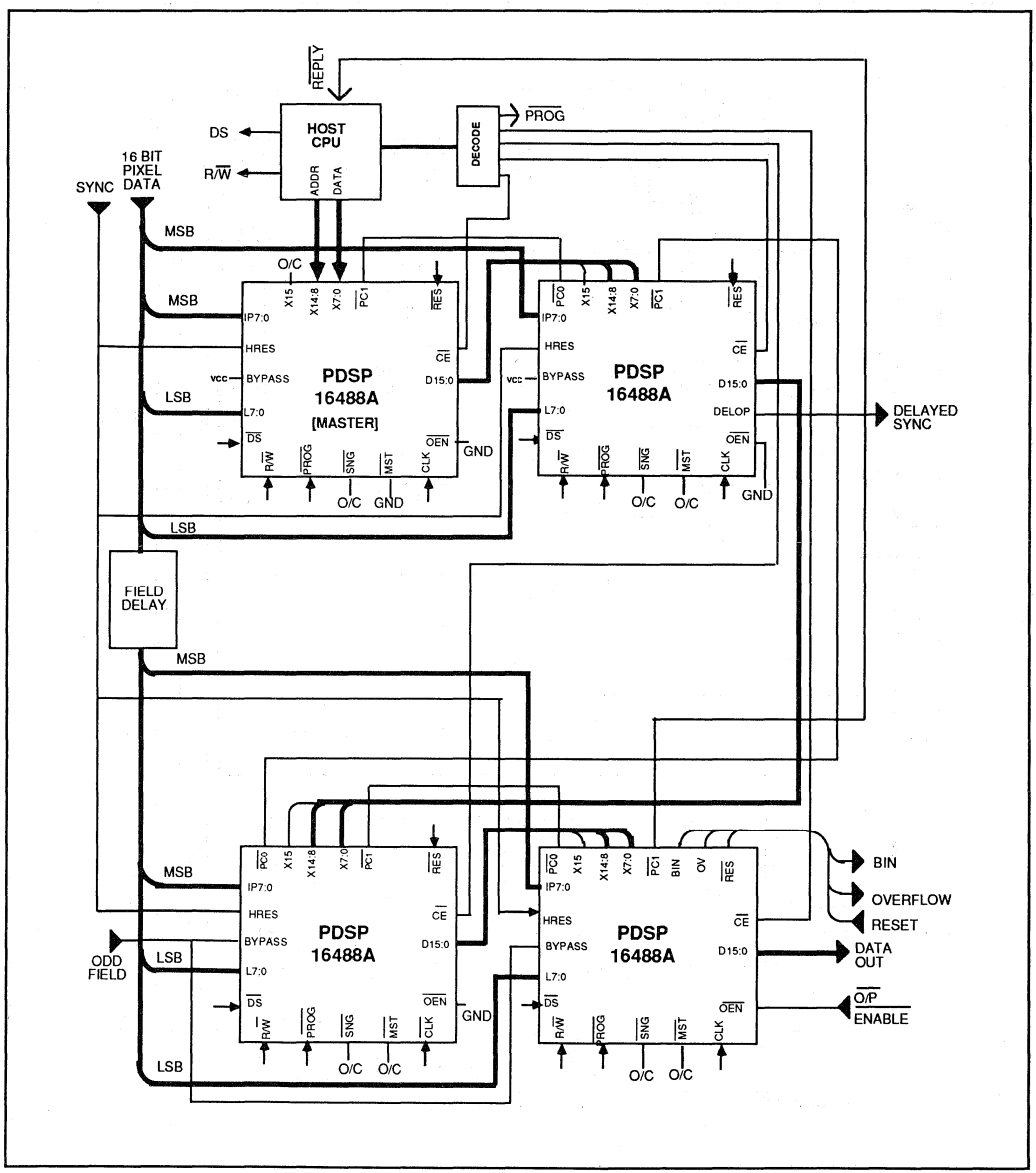


Figure 16. Four Device System with 16 Bit Pixels

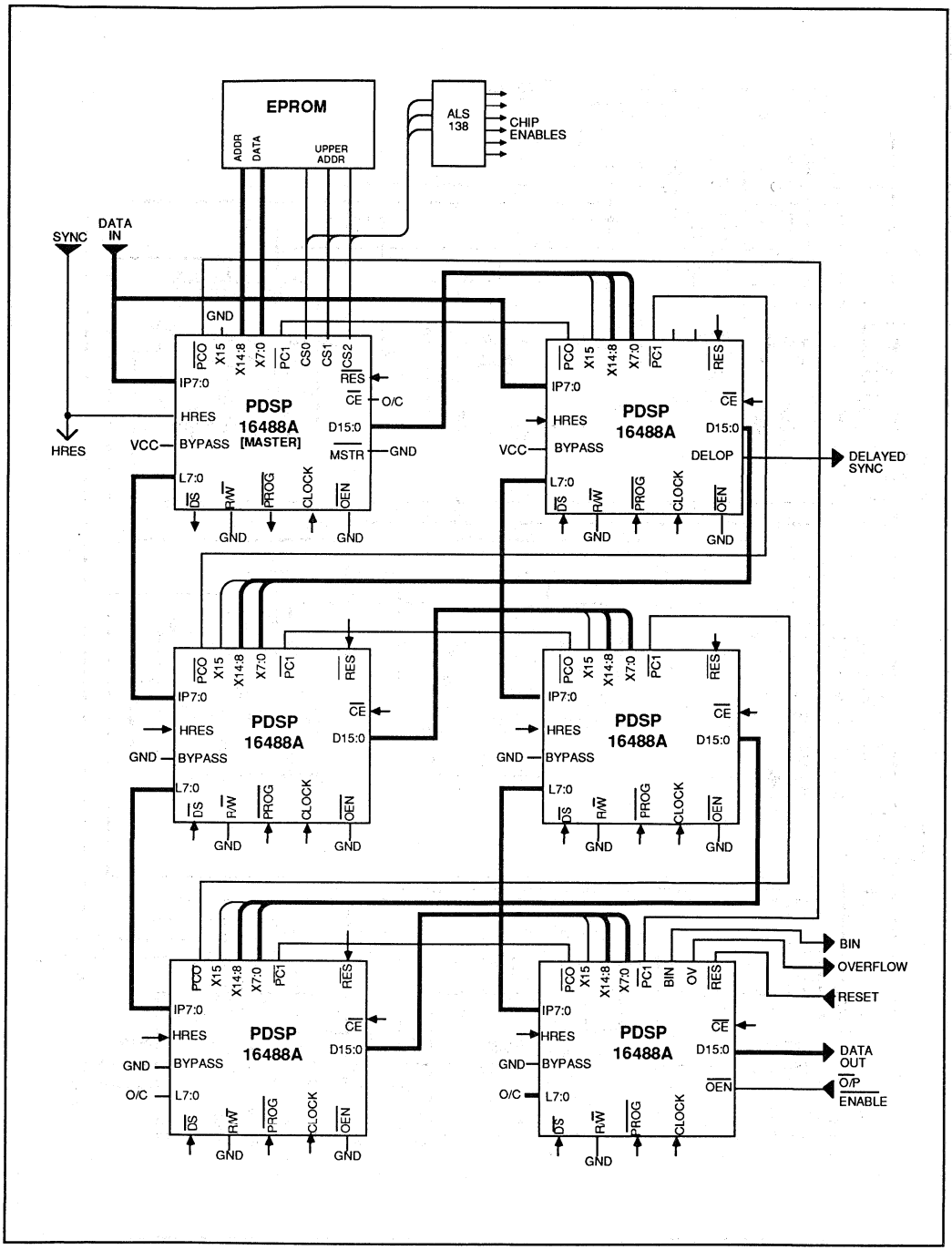


Figure 17. Six Device Non Interlaced System.

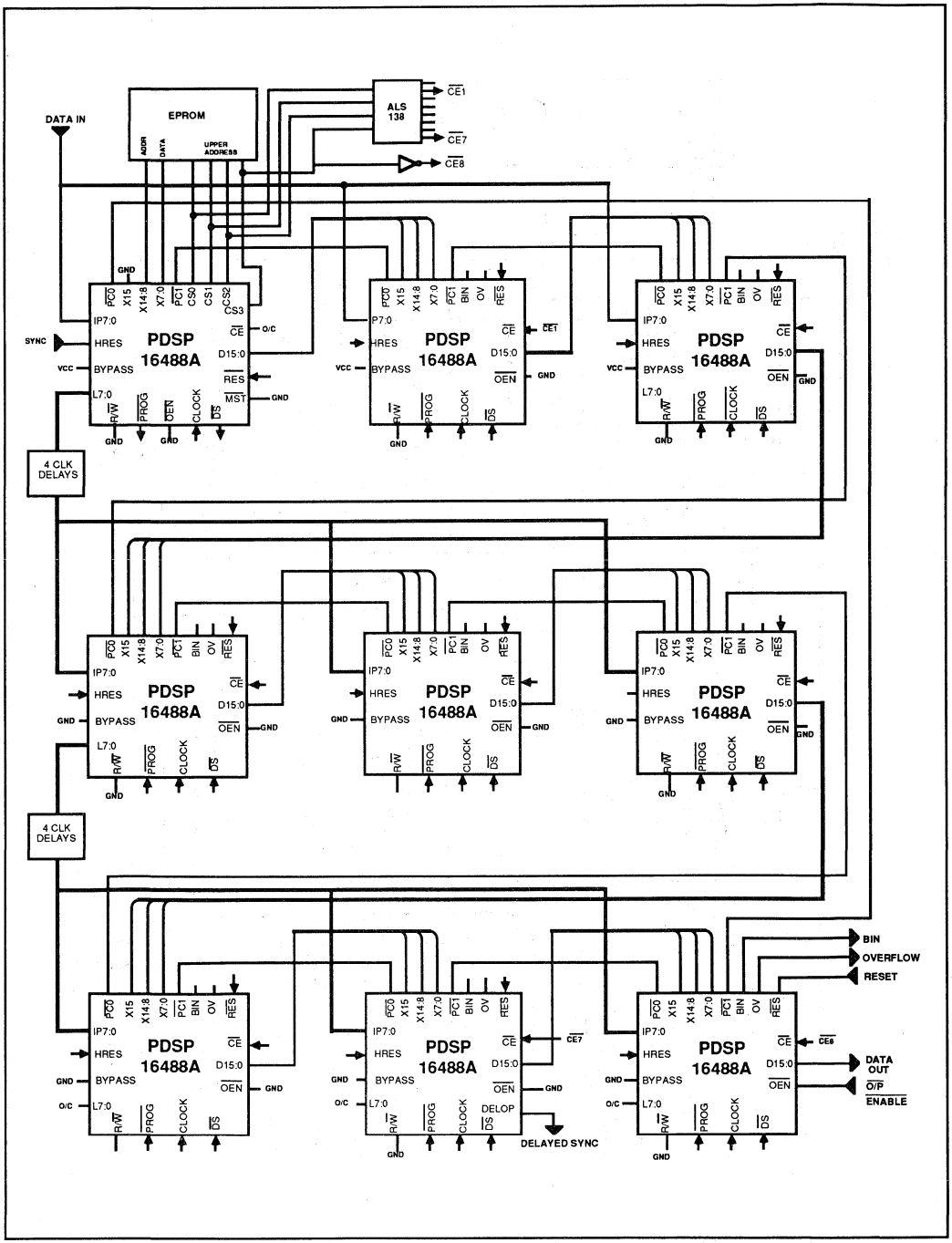


Figure 18. Nine Device Non Interlaced System.

ORDERING INFORMATION

Commercial (0°C to +70°C)
PDSP16488A / C0 / AC (PGA)
PDSP16488A / C0 / GC (QFP)

Industrial (-40°C to +85°C)
PDSP16488A / B0 / AC (PGA)
PDSP16488A / B0 / GC (QFP)

Military (-55°C to +125°C)
PDSP16488A / A0 / AC (PGA)
PDSP16488A / A0 / GC (QFP)

Call for availability of high rel and MIL883 screened parts

PDSP16510A

STAND ALONE FFT PROCESSOR

(Supersedes version in December 1993 Digital Video & DSP IC Handbook, HB3923-1)

The PDSP16510 performs Forward or Inverse Fast Fourier Transforms on complex or real data sets containing up to 1024 points. Data and coefficients are each represented by 16 bits, with block floating point arithmetic for increased dynamic range.

An internal RAM is provided which can hold up to 1024 complex data points. This removes the memory transfer bottleneck, inherent in building block solutions. Its organisation allows the PDSP16510 to simultaneously input new data, transform data stored in the RAM, and to output previous results. No external buffering is needed for transforms containing up to 256 points, and the PDSP16510 can be directly connected to an A/D converter to perform continuous transforms. The user can choose to overlap data blocks by either 0%, 50%, or 75%. Inputs and outputs are synchronous to the 40MHz system clock used for internal operations.

A 1024 point complex transform can be completed in some 98µs, which is equivalent to throughput rates of 450 million operations per second. Multiple devices can be connected in parallel in order to increase the sampling rate up to the 40MHz system clock. Six devices are needed to give the maximum performance with 1024 point transforms.

Either a Hamming or a Blackman-Harris window operator can be internally applied to the incoming real or complex data. The latter gives 67dB side lobe attenuation. The operator values are calculated internally and do not require an external ROM nor do they incur any time penalty.

The device outputs the real and imaginary components of the frequency bins. These can be directly connected to the PDSP16330 in order to produce magnitude and phase values from the complex data.

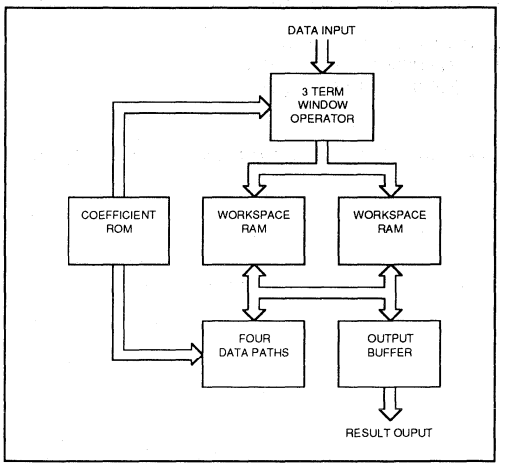


Fig. 1. Block Diagram

FEATURES

- Completely self contained FFT Processor
- Internal RAM supports up to1024 complex points
- 16 bit data and coefficients plus block floating point for increased dynamic range
- 450 MIP operation gives 98 microsecond transformation times for 1024 points
- Up to 40MHz sampling rates with multiple devices.
- Internal window operator gives 67dB side lobe attenuation and needs no external ROM.
- 84 pin PGA or 132 surface mount package

ASSOCIATED PRODUCTS

PDSP16540 Bucket Buffer

PDSP16330 Pythagoras Processor.

PDSP16256 Programmable FIR Filter.

PDSP16350 I/Q Splitter / NCO

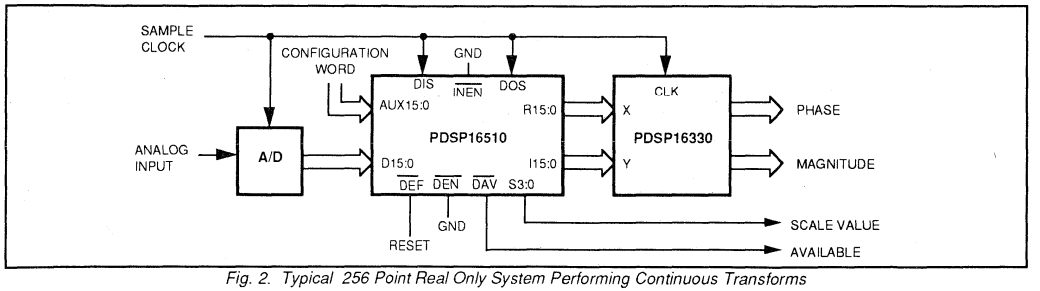
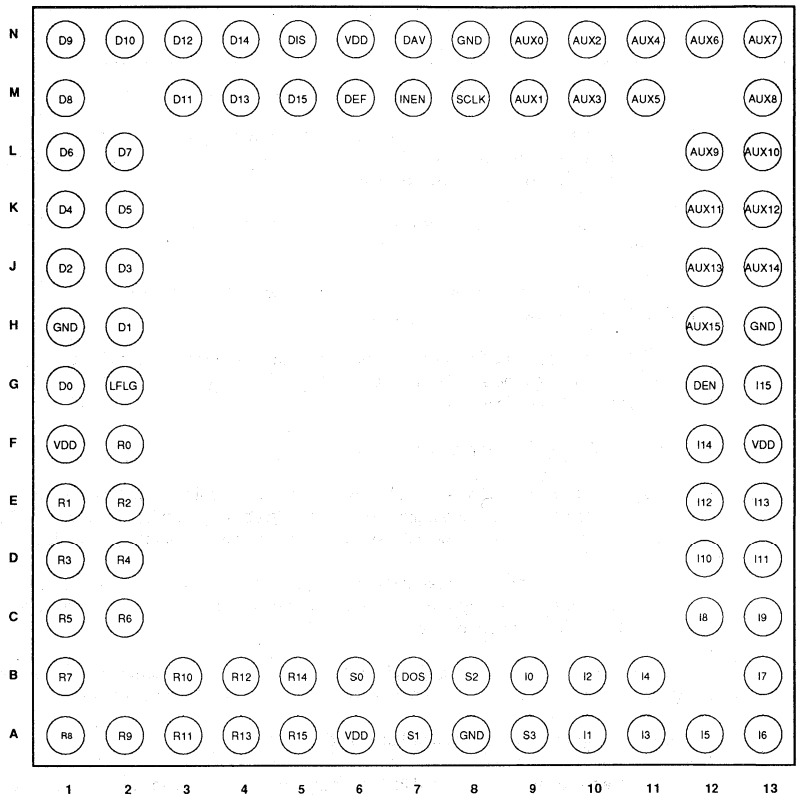


Fig. 2. Typical 256 Point Real Only System Performing Continuous Transforms



Pin Out for 84 PGA Package (AC84) - bottom view

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	VDD	23	AUX13	45	GND	67	D8	89	GND	111	GND
2	GND	24	VDD	46	VDD	68	D7	90	R3	112	S1
3	I7	25	AUX12	47	SCLK	69	D6	91	VDD	113	GND
4	I8	26	GND	48	GND	70	D5	92	R4	114	DOS
5	I9	27	AUX11	49	GND	71	GND	93	GND	115	DOS
6	I10	28	VDD	50	DAV	72	VDD	94	R5	116	VDD
7	VDD	29	GND	51	GND	73	D4	95	R6	117	S2
8	I11	30	AUX10	52	INEN	74	GND	96	R7	118	GND
9	GND	31	AUX9	53	VDD	75	D3	97	R8	119	S3
10	I12	32	AUX8	54	DEF	76	VDD	98	GND	120	GND
11	VDD	33	AUX7	55	GND	77	D2	99	VDD	121	VDD
12	I13	34	VDD	56	DIS	78	GND	100	R9	122	I0
13	GND	35	AUX6	57	VDD	79	D1	101	VDD	123	I1
14	I14	36	VDD	58	D15	80	VDD	102	R10	124	GND
15	VDD	37	AUX5	59	D14	81	D0	103	R11	125	I2
16	I15	38	GND	60	GND	82	LFLG	104	R12	126	I3
17	GND	39	AUX4	61	D13	83	GND	105	R13	127	I4
18	DEN	40	AUX3	62	D12	84	R0	106	GND	128	GND
19	AUX15	41	AUX2	63	D11	85	GND	107	R14	129	VDD
20	GND	42	VDD	64	D10	86	R1	108	R15	130	I5
21	AUX14	43	AUX1	65	VDD	87	VDD	109	DISAB	131	I6
22	GND	44	AUX0	66	D9	88	R2	110	S0	132	VDD

Pin Out for 132 Leaded Chip Carrier (GC132)

SIGNAL	TYPE	DESCRIPTION
D15:0	I	Data input during real only mode. The real component in complex data mode.
AUX15:0	I	When DEF is active AUX15:0 are used to define the operating mode as defined in Table 3. When DEF is in-active AUX15:0 either provide the 16 bit imaginary component of complex input data, or a second set of real only inputs.
R15:0	O	These pins output the real component of the transformed data when DAV and DEN are active. Otherwise they are high impedance.
I15:0	O	These pins output the imaginary component of the transformed data when DAV and DEN are active. Otherwise they are high impedance.
$\overline{\text{DEF}}$	I	The high going edge of DEF is used to internally latch the contents of AUX15:0, which then define the operating mode. In the simplest system DEF is a power on reset. When DEF is low the internal control logic is reset.
SCLK	I	System clock used for internal computations.
S3:0	O	These pins indicate the number of shifts towards the binary point which have occurred as the result of the conditional scaling logic. When the data path right shift is restricted to 2 places per pass, state 15 is used to indicate an overflow and only a total of 14 shifts is possible.
LFLG	O	This flag indicates that data is being loaded into the device. It goes active in response to an INEN input, and may be programmed to go in-active after the complete, one quarter, or one half a data block has been loaded.
$\overline{\text{INEN}}$	I	The use of this input is mode dependent. It is either used as an active low, load enabling, signal for the DIS strobe, or it is used to initiate a new block load operation.
DIS	I	The rising edge of this input is used to load data into the device.
DOS	I	The rising edge of this input is used to dump data from the device. In most applications it may be tied to the DIS input, even if the output rate must be higher than the input rate because of overlapped data blocks. The DIS input is then internally divided down.
$\overline{\text{DAV}}$	O	An active low signal that indicates that a transform is complete. Transformed data will then be output in normal sequential order using DOS. It may be optionally programmed to be delayed by 24 DOS strobes to match the delay through a PDSP16330.
$\overline{\text{DEN}}$	I	This input is used to enable the data dump operation when DAV has gone active. If it is tied low the device will automatically dump data when DAV goes active. Otherwise the device will wait for the enabling signal to go low before the dump operation commences.
DISAB	I	Only available in the 132 pin GC package. When high the block floating logic is disabled.
VDD	P	+5V pins
GND	P	Ground pins

NOTE. All references to DEF, INEN, DAV, and DEN within the text do not contain the bar designator, signifying an active low signal. This is considered to be implied by the signal name and is not meant to imply a change in the signal function.

FUNCTIONAL OPERATION

The PDSP16510 performs decimation in time, radix 4, forward or inverse Fast Fourier Transforms. Data is loaded into an internal workspace RAM in normal sequential order, processed, and then dumped in the correct order. With real only input data the processing time can approximately be halved for a given transform size. Two real inputs then replace a single complex input, and are processed in parallel.

Either a Blackman-Harris or a Hamming window can be generated internally, and applied to the incoming real or complex data with no time penalty. No external ROM is needed to support these windows. The Blackman-Harris window gives improved dynamic range over the Hamming window when two closely

spaced frequencies are to be detected, and one is of smaller magnitude than the other. It does, however, reduce the actual frequency resolution, and the Hamming window may then be preferable.

Data in and out of the device is represented by 16 bit real and imaginary components, with 16 bit sine and cosine values contained in an internal ROM. Conditional scaling, coupled with word growth through the butterfly data path, gives increased dynamic range. Transforms can be computed with sample sizes of either 256 or 1024 data points. The 256 point option can alternatively be used to simultaneously execute either four 64 point transforms, or sixteen 16 point transforms. The 16 point mode can only be used with a rectangular window, and no overlapping of data blocks is possible.

The device can be configured, either, to perform continuous transforms in a real time application, or as slave processor to a more general purpose signal processing system. In the continuous mode, with transform sizes of 256 points or less, it contains three internal control units which simultaneously allow new data to be loaded, present data to be transformed, and previous results to be dumped. Additional, external, input/output buffering is not needed. The internal input buffer also allows data blocks to be overlapped by either 50% or 75%, apart from the mode with no overlaps.

When 1024 point transforms are to be calculated, without loss of incoming data during the transform time, it is necessary to use an input buffer. This requirement is satisfied by a single PDSP16540 support device.

In any of the real or complex modes it is possible to obtain higher performance by connecting devices in parallel. It is then possible to increase the sampling rate to that of the system clock used for internal operations.

The mode of operation of the device is controlled by 16 bits in a control register. These are loaded through the AUX15:0 port when a control signal DEF is active low. This port is also used to provide the imaginary component of complex input data, and, if complex transforms are to be performed, an external tristate buffer will be needed to isolate the control information. This should only be enabled when DEF is active. DEF is also used to initialise the internal circuitry, and can be a simple power on reset if control parameters need not be subsequently changed.

DATA PRECISION

During each pass of a radix-4 fast Fourier transform it is possible for either component of a particular result to grow by a factor of up to four in the first pass, and 5.242 in subsequent passes. This is between two and three bits in each pass and the data path must allow for this word growth to avoid any possibility of overflow. At the end of the data path the word is again reduced to 16 bits by discarding least significant bits. Any un-necessary word growth to prevent overflow thus results in loss of arithmetic precision, and has a detrimental effect on the dynamic range achievable.

In practice these large word growths only occur when bipolar complex square waves are transformed, and even then will not occur on every pass. The PDSP16510 compromises by allowing a 2 bit word growth during the butterfly calculation in the first pass. This is equivalent to ignoring the most significant bit of the 19 bit final result, which is assumed to be an extra sign bit, and then selecting the next 16 bits for

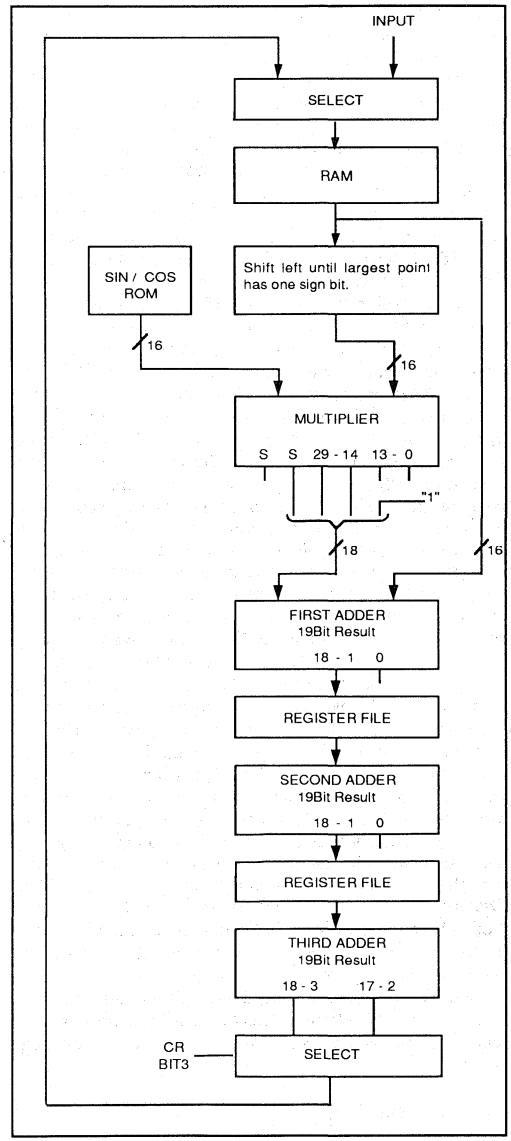


Fig. 3 One of Four Data Paths

storage. In subsequent passes a Control Register Bit allows the user to continue to select these 16 bits, or instead to use the 16 most significant bits. The latter option is equivalent to a 3 bit word growth. The 2 or 3 bit word growth option applies to ALL subsequent passes and is not a per pass option.

If the 2 bit option is selected there is a possibility of overflow occurring in one of the passes. The prediction of overflow is mathematically difficult, and only occurs with specific complex square waves. Scaling down the inputs cannot be guaranteed to prevent overflow because of the

block floating point shifting scheme, which is discussed later. Overflow can NEVER occur if the 3 bit option is chosen, but at the expense of worse dynamic range.

When overflow does occur a flag is raised which can be read by the user (see later discussion on scale tag bits), and the results ignored. In addition all frequency bins are forced to zero to prevent any erroneous system response.

Even with only 2 bit word growth poor dynamic range will be obtained if the data is simply reduced to 16 bits, and becomes worse when the incoming data does not fully occupy all the bits in the word. These problems are overcome in the PDSP16510, however, by a block floating point scheme which compensates for any unnecessary word growth.

During each pass the number of sign bits in the largest result is recorded. Before the next pass, data is shifted left [multiplied by 2], once for every extra sign bit in this recorded sample. At least one component in the block then fully occupies the 16 bit word, and maximum data accuracy is preserved

Up to four shifts are possible before every pass after the first, with a total of fifteen for the complete transform. At the end of the transform the number of left shifts that have occurred is indicated on S3:0. Lack of pins prevents a separate output being available to indicate that overflow has occurred in the 2 bit word growth option. For this reason the maximum number of compensating left shifts in this mode is restricted to 14. State 15 is then used to indicate that overflow has occurred.

The first step in the butterfly calculation multiplies 16 bit data values with 16 bit sine/cosine values, to give 18 bit results. This increased word length preserves accuracy through the following adder network, and has been shown through simulations to be an optimum size for transform sizes up to 1024 points. This is particularly true when the input data is restricted to below 16 bits, as is necessary with practical A/D converters with very high sampling rates. The bottom bit of this 18 bit word is forced to logical one and as such is a compromise between truncation and true rounding. It gives a lower noise floor in the outputs compared to simple truncation.

To prevent any possibility of overflow during the butterfly calculation the word length is allowed to grow by one bit through each of the three adders. The least significant bit is always discarded in the first two adders . Sixteen bits are then chosen from the final adder in the manner discussed earlier, and the number of sign bits in the largest result is recorded for use in the following pass.

Fig. 3 shows one of the four internal data paths which can compute a radix-4 butterfly in twelve system clock cycles. This equates to completing the butterfly in 3 cycles for the complete device.

DATA TRANSFERS

The data transfer mechanism to and from the internal

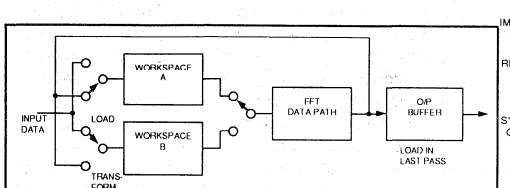


Fig. 4. RAM Organization with 256 Data Points

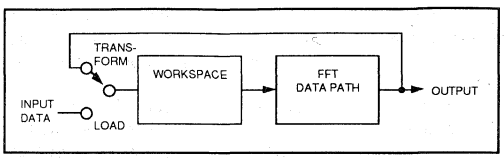


Fig. 5. RAM Organization with 1024 Point Transforms

RAM has been designed for use in a wide variety of applications. The provision of an independent input strobe (DIS), allows data to be loaded without the need for additional external buffering. An independent output strobe (DOS) is also provided. DIS and DOS can thus be tied together, this being particularly useful when the device is performing the inverse transform back to the time domain. Transfer of data occurs internally from DIS to SCLK, so although thay can be of different frequencies, they must be synchronous to each other. In the same way transfer of data also occurs from SCLK to DOS, so while DOS can also be independent of SCLK it must also be synchronous to it. Inputs and outputs are both supported by flag and enabling signals which allow transfers to be properly co-ordinated with the internal transform operation.

In many applications the DIS and DOS inputs can be tied together and fed by the sampling clock. If the output rate must be higher than the input rate, as with multiple devices supporting overlapped data samples, both strobes can still be connected together. The clock supplied should then be twice or four times the sampling clock, and an internal divider can be used to provide the correctly reduced input rate. The provision of a separate DOS pin does, however, allow the output rate to be different to the input rate, and therefore faster than strictly needed. Further output processing at higher rates is then possible if this is advantageous to system requirements.

The internal workspace is double buffered when 256 point transforms are to be performed. A separate output buffer is also provided. These resources, together with separate input and output buses, allow new data to be loaded and old results to be dumped, whilst the present transform is being computed. Additional, external, input buffering is not needed to prevent loss of incoming data whilst a transform is being performed.

When block overlapping is required, internally stored data will be re-used, and a proportionally smaller number of new samples need be loaded. Note that the internal window operator still functions correctly since it is actually applied during the first pass, and not whilst data is being loaded. The internal RAM organisation is shown in Fig. 4. It should be

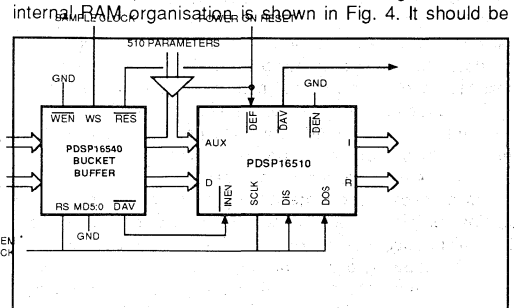


Fig. 6. 1024 Point Transforms with I/P Buffer

noted that the amount of overlap between I/O transfers and transforms is completely under the control of the system, since an input enable signal (INEN) and an output enable (DEN) can be used to initiate transfers.

In the 1024 point mode there is insufficient workspace for input and output buffering in addition to working memory. The device is then configured in a mode with separate load, transform and dump operations. The internal arrangement is shown in Fig. 5. The support of an external input buffer is needed if incoming samples are not to be lost whilst a transform is in progress. This is loaded at the sample clock rate and transferred to the FFT processor as quickly as possible. In this mode the PDSP16510 always expects to receive 1024 words, regardless of the amount of block overlapping. Data stored internally cannot be re-used when block overlapping is required, and data from the external buffer must be re-read as necessary.

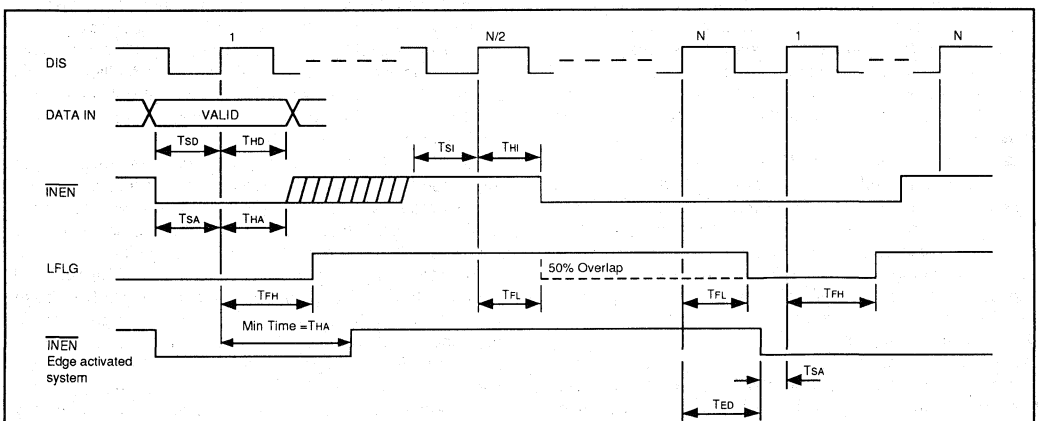
Fig. 6 illustrates a typical 1024 point system with an input buffer which supports complex input data. The input buffer can be provided by a PDSP16540 Bucket Buffer without the need for any external control logic. It supplies RAM for 1024 x 32 complex words, and allows transfers to the FFT Processor at the full system clock rate. The PDSP16540 also supports the standard 50% and 75% data block overlapping, but in addition allows the user to define the amount of overlap to within 32 words.

If no incoming data is to remain un-processed, the user must ensure that the time taken to acquire sufficient data to instigate a new transform is greater than or equal to the transformation time itself. The latter can be calculated from Table 4, once the system clock rate has been defined. When 1024 point transforms are performed, both the time to read data from the input buffer, and also the time to dump data, must be included in the calculation to determine the minimum time in which data can be loaded into the external buffer.

The peak transfer rate is limited by the characteristics of the I/O circuits, but can be greater than the sampling rate which is determined by the transform time. When load and dump operations are not concurrent with transform operations (as in the 1024 point modes), then the maximum I/O rate is equal to the system clock rate, Ø. When other transform sizes are specified, the sampling rate, S, is reduced by a factor F. This is defined below where Ø is in MHz and L is the system clock low time in nanoseconds :

$$S = F\text{Ø}, \quad \text{where } F = \frac{4}{(6+0.001\text{Ø}L)}$$

F is typically 0.66 and applies to all transforms except for those of 1024 points, even if INEN is driven such that concurrent operations do not actually occur (Note also that S must be



Characteristic	Symbol	16510A,A0,B0,C0 Min	Max		Units
Data In set up Time	T_{SD}	10			ns
Data In Hold Time	T_{HD}	0			ns
INEN active going set up	T_{SA}	8			ns
INEN active Hold Time	T_{HA}	0			ns
INEN in-active Hold Time to ensure no load	T_{HI}	2			ns
INEN in-active going set up for no load operation	T_{SI}	8			ns
Delay to LFLG going active (30 pf load)	T_{FH}		10		ns
Delay to LFLG going in-active (30 pf load)	T_{FL}		10		ns
Min time to INEN low in edge mode	T_{ED}	15			ns

Table 1. Advanced Timing Information with Continuous Inputs.

synchronous to SCLK). If this causes a system limitation in a single device application, then the device can be configured for pseudo, Mode 2, multiple device operation. Separate load, transform, and then dump operations will then always occur but DEN must be low when a transform is complete or DAV will never go active. See the section on multiple device operation.

LOADING DATA

Data loading is controlled by three signals; DIS an input strobe, INEN a load enable, and LFLG an output flag. Detailed timing information is given in Table 1. Once sufficient data has been acquired, a transform will automatically commence. This is normally after a complete block has been loaded, except when a single device is performing overlapped transforms of 256 points or less. With 75% overlapping, transforms will commence after 25% of a new block has been loaded, and with 50% overlapping transforms commence after 50% of the data has been loaded. The remainder of the block is provided by data already stored in the internal RAM.

The data strobe is used to load data into the internal workspace RAM, and data must meet the specified set up and hold times with respect to its rising edge. DIS can be a continuous input since the device only loads data when an input enabling signal is active.

An internal synchronisation interval is necessary between the last sample being loaded with the DIS strobe and transforms being started with the system clock. This can be up to twelve system clock periods when data transfers and transforms are overlapped. The transform times given later in Table 4 are maximum values, and include these twelve periods.

The way in which the INEN signal controls data loading is dependent on whether a single or multiple device is to be implemented, and the status of Control Register Bit 12.

When Bit12 is set in a SINGLE device system the INEN signal is simply used as an enable for the DIS strobes. When INEN is low, and provided the relevant set up and hold times have been satisfied, data will be loaded with the rising edge of the DIS strobe. If no gaps occur within the incoming data, INEN can be tied permanently low, provided that the sampling rate has been chosen such that transforms are completed before a new block of data is loaded. For transforms of less than 1024 points, data will then be continually processed without any loss of information. In the 1024 point modes the device will cease loading data when 1024 samples have been loaded, and even if INEN remains low no more data will be accepted until the previous results have been dumped.

In a multiple device system an edge is ALWAYS needed to commence a load operation, and Bit 12 has a different purpose. The edge is provided by INEN going low. Loading will cease when a complete block (or group of blocks with multiple concurrent transforms) of data has been loaded, even if INEN remains low. INEN must go high at some point after the minimum hold time has been satisfied, and then return low AFTER ALL DATA HAS BEEN LOADED, before a new load operation can commence. Low going edges which occur before all data has been loaded will be ignored.

The INEN edge mode is actually provided for the correct operation of multiple device systems, but if Bit 12 in the Control Register is reset in the SINGLE device mode, the edge activated operation will still be possible. With all but 256 point complex transforms, the single device edge mode of operation is identical to that of a multiple device system. With 256 point transforms, and their concurrent derivatives, the location of the low going edge in the data stream is dependent on the amount of block overlapping. The low going edge transition must be provided after 64 samples have been loaded with 75% overlapping, and after 128 samples have been loaded with 50% overlapping. With no overlapping the edge must be provided after 256 samples have been loaded.

In a single device system with Bit 12 set, INEN can be taken high to inhibit the load operation when gaps occur in the data stream. In the INEN edge activated mode gaps in the data stream can only be accommodated if the DIS clock is externally inhibited. Taking INEN high will not inhibit the loading of data in this mode.

With gaps in the data stream the peak sampling rates can be higher than continuous sampling rates. When data loading is not coincident with transform operations the peak rate can equal that of the system clock, otherwise it is reduced by the factor, F, given on the opposite page.

When Control Register Bit 12 is set in any multiple device mode, the DEF high going edge will also initiate a load operation after it has been internally synchronised to the rising DIS edge. If the first device in a multiple device system is programmed in this manner, the transform sequence will automatically start when DEF goes in-active. The other devices need the INEN edge as usual, and must have Bit 12 reset. A fuller explanation of the use of Bit 12 in a multiple device mode is given in the section on I/O In Multiple Device Systems. Note that the use of Bit 12 in a single device system (Control Register Bits 10:9 = 00) is completely different to its use in a multiple device mode.

The LFLG output goes active in response to the DIS rising edge used to load the first data sample, and indicates that a load operation is occurring. In an edge activated system the LFLG output will go high as the result of the first high going DIS edge after INEN has gone low. In the simple INEN enabling mode, internal logic counts the number of valid inputs and detects when the programmed block length has been reached. LFLG then goes low and will go high again in response to the next valid DIS strobe. LFLG will go low when DEF is active and will go high in response to the first INEN enabled DIS edge after DEF has gone in- active.

The active going LFLG edge does not normally have any system significance, but in the block overlapping modes the in-active going edge will occur when 50% or 75% of the data has been loaded. By driving the INEN input on one device with the LFLG output from a previous device, this edge can be used to partition data between several devices in a multiple device system. It can also be used to provide an address marker for a user defined input buffer, when executing 1024 point transforms with a single device. It is not needed, however, when the input buffer is provided by the PDSP16540.

DUMPING DATA

Data output is controlled by an output strobe [DOS], a dump enable signal [DEN], and a Data Available signal [DAV]. The DAV signal is used to indicate that the internal output buffer contains transformed data, and the DEN input is used to control the outputting of that data. The output buffer within the device is clocked by the DOS input, and must be primed

with a number of DOS strobes (see "user notes - stopping DOS") once a transform is complete in order to transfer data to the output pins. DAV will not go active until this priming has occurred.

The state of the DEN input at the end of a transform is used to control the transition of the active going edge of the DAV output with respect to the DOS strobes. The latter are then used to transfer data from the device to the next system component. If the DEN input is tied low in a single device system, the active going DAV transition will be internally synchronised to the rising edge of a DOS clock. If DEN is not tied low it must be guaranteed to be low at the end of the internal transform operation for this synchronization to occur. Since there is no external indication of this event, the user must take care to only allow DEN to go high whilst DAV is active, if this DAV synchronous mode is needed.

SYNCHRONIZED DAV OPERATION

In the DAV synchronised mode the first rising edge of the DOS clock, after DAV has gone active, must be used to transfer the first transformed sample from the output pins to the next system component. It should be noted that the output buffer will have been primed before the active DAV transition, since DOS must be a continuous clock, and there is then no delay before the first output becomes valid. The DAV output can be used as a clock enable for this next device, and transfers will continue in normal sequential order until the required data has been dumped. DAV will then go inactive in response to the last DOS edge which was used to transfer data to the next device.

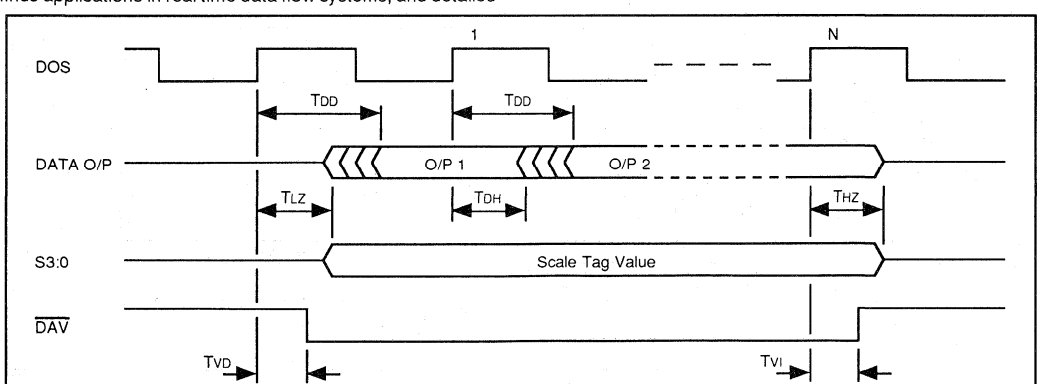
This mode of automatically dumping data when it is ready finds applications in real time data flow systems, and detailed timing is given in Table 2. It should be noted that the DOS input MUST be continually present before DAV goes active. If this is not the case the DAV output will not go active at the correct time, and the internal output circuitry will not be primed. Once DAV is active, however, it is possible for DOS to be irregular, and DEN can be used to inhibit the action of the output strobe as discussed previously. For the correct operation of the device the user must ensure that DOS becomes continuous and DEN remains low once DAV goes in-active.

When continuously transforming data such that new outputs are internally available before the previous block has been completely dumped, then DAV would normally stay active and give no indication that one block dump had been finished and another block started. Additional internal circuitry is, however, provided to ensure that DAV goes inactive for one DOS high time, thus supplying an inter block marker.

ASYNCHRONOUS DAV MODE

If DEN is not active in a single device when the transform is complete, then the device will wait for DEN to go active before any data is dumped. This mode is suitable for applications in which output processing is under the control of a remote host, such as a general purpose digital signal processor. The DAV output will then go active as soon as the output buffer is full, and will not be synchronised to the DOS edge. In such systems the DOS strobe may not necessarily be present at this time. Table 3 gives the relevant timing information.

In this host controlled dump mode the PDSP16510 waits for the host to activate the DEN input after DAV has gone active. DEN then functions as an enable for the host produced data strobes on the DOS pin. DEN may either stay active for the complete transfer, or may be used to enable each DOS



Characteristic	Symbol	16510A,A0,B0,C0 Min	Max		Units
Output Enable Time	T_{LZ}		15		ns
Output Disable Time	T_{HZ}		15		ns
Data Delay Time (30 pf load)	T_{DD}		15		ns
Data Hold Time	T_{DH}	2			ns
$\overline{DAV}$ active Delay Time (30 pf load)	T_{VD}	1	10		ns
$\overline{DAV}$ in active Delay Time (30 pf load)	T_{VI}	1	10		ns

Table 2. Output Timing with DEN tied low. (Advanced Data)

input. When DEN and DOS are both active an internal read operation occurs, and an address generator is incremented. DAV goes in-active in response to the DOS edge needed to read the last output, unless Bit 15 in the Control Register is set. In this case DAV goes in-active when the next INEN edge is received for reasons given later.

In host controlled systems the time to dump data could be longer than the transform time. The dump time in such a system will dictate the maximum sampling rate that can be used without the loss of incoming data. In the 1024 point mode, when the loss of data is not important, the PDSP16510 is designed to not accept new data until the previous results have been dumped. Such a system needs no input buffer, and INEN can be permanently tied low if the edge activated mode is not in use. If the loss of data is to be avoided an input buffer is needed and the host must have received all the results before a new block of data has been loaded into the buffer.

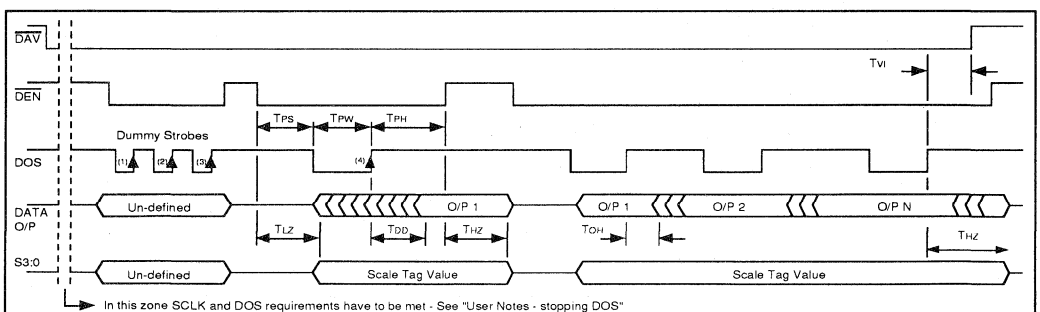
For 256 point transforms, with host controlled dumping, it is still possible to overlap load and dump operations. The maximum dump times, however, must be less than the load times to avoid data corruption. Previously converted outputs will be actually corrupted, rather than inputs simply not being used.

If the loss of incoming data is not important, the device can be forced to do separate load, transform, and then dump operations. The corruption of results will then never occur, no matter what dump time is taken. This can be achieved by ensuring that INEN is not active between loading a block of data and completing the dump of the results from that data. The same ends can be achieved if the INEN edge activated mode (Bit 12 reset) is used, and the inverted DAV edge is used to drive the INEN input. This then initializes a new load operation only when the previous dump has been completed.

Results are transferred from the device with the rising edge of the DOS strobe when DEN is active. This is consistent with using the device in a data flow architecture, as is commonly employed in data processing systems. In a typical microprocessor based system, however, data is normally expected to become valid before the end of the data strobe produced by the processor. It is thus necessary for the user to provide a 'dummy' data strobe in order to transfer data to the outputs which can then be read by the host during the next data strobe. In addition further ' dummy ' strobes are needed each time DAV goes active in order to prime the output circuitry. The actual output sequence is given in Table 3 for a single device systemand is described more fully in "user notes - stopping DOS".

GENERAL DUMP CONSIDERATIONS

The tri-state drivers on the output buses are only enabled when both DAV and DEN are active. When DEN is tied permanently low the output bus will start to become valid from the DOS edge which also generates the DAV output. The next DOS edge can then be used to transfer the first output to the next device. When DEN is driven low in response to the DAV output, the outputs start to become valid when DEN goes low. The Scale Tag outputs become valid at the same time as data, and when enabled will continue to indicate the correct value until all frequency bins have been dumped. If at any time during the dump operation DEN goes in- active, then both the



Characteristic	Symbol	16510A,A0,B0,C0 Min	Max		Units
$\overline{DEN}$ Set Up Time	T_{PS}	10			ns
Host Strobe Width	T_{PW}	10			ns
$\overline{DEN}$ Hold Time	T_{PH}	5			ns
$\overline{DAV}$ in-active going Delay (30 pf load)	T_{VI}		10		ns
Output Enable Time (see Fig 13)	T_{LZ}		10		ns
Output Data Delay Time (30 pf load)	T_{DD}		15		ns
Output Disable Time (see Fig 13)	T_{HZ}		10		ns
Read Cycle Time	T_{RC}	25			ns
Old Data Hold Time	T_{OH}	2			ns

Table 3. Host Controlled Output Timing. (Advanced Data)

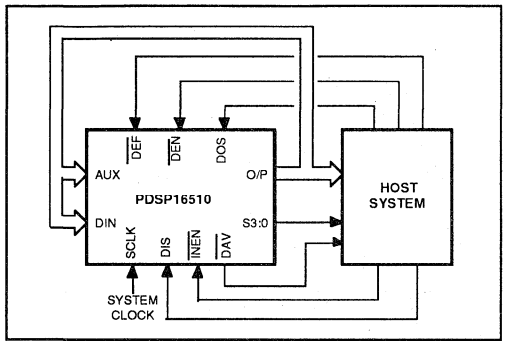


Fig. 7. Host Controlled System

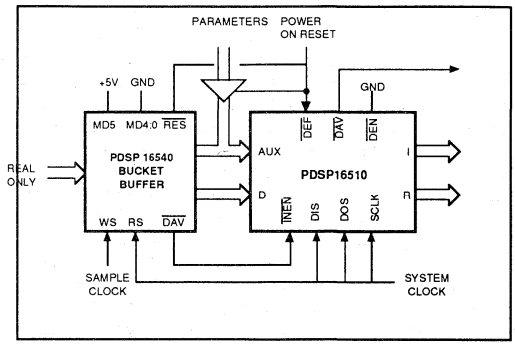


Fig 8. 1024 Point Real Transforms

data and scale tag outputs will go high impedance after the delay shown in Table 3.

Valid transformed data is actually available within the device from DAV going active until INEN again goes active, and a new set of data is loaded. The output tristate drivers, however, normally go high impedance when DAV goes inactive once a dump operation has been completed. In order to support systems in which it may be necessary to read the transformed data more than once, a Control Register Bit is provided which keeps the DAV output active until a further INEN edge is received. The user must then keep track of how many outputs have been dumped before INEN is generated to start a new load operation.

The DAV output can be delayed by an amount equivalent to the pipeline delay through the PDSP16330. This option is invoked by setting a control bit, and allows DAV to indicate that polar data is available at the output of the PDSP16330. When the option is used the tri-state outputs will be enabled when data is actually available and DEN is active, and not when DAV eventually goes active.

Two Control Register Bits allow a range of dump size options to be supported. In some applications the results of interest may only lie in the lower 25 or 50% of the frequency bins, the sampling rate having been chosen to prevent aliasing, and the transform size having been selected to give the required frequency resolution. In other systems it is only necessary to output the second half of a given sized transform. This is useful when filtering is to be performed in the frequency domain using Overlap /Discard Fast Convolutions. With this method FIR filters with N taps can be implemented in the frequency domain using 50% overlapped transforms on 2N samples. After multiplication in the frequency domain with the required frequency response, the inverse transform is performed and the first half of each output is discarded. Since only half the results are dumped, the dump clock need not be twice the rate of the clock used to load data.

FULL CO - PROCESSOR OPERATION

A single device can be configured as a co-processor to a host system in which both the loading and dumping of data is under the control of the host. Such a system is shown in Figure 7, in which DEN is a host provided enable for host read operations, and INEN is an enable for host write operations. DIS and DOS are host data strobes.

The host loads a block of data into the PDSP16510, using DIS enabled by INEN, which is then automatically transformed. The DAV output provides a flag indicating that the transform is complete, and results are then read by the host using DOS enabled by DEN. A new set of inputs is not normally loaded until the previous results are complete. If, however, 1024 point transforms are not to be performed, loading new data could coincide with dumping previous results. This, however, would require a host system with separate input and output buses, and which also allowed coincident transfers. As discussed previously, transferring results must take no longer than loading new data to prevent corruption of the outputs.

In the system illustrated by Figure 7, the host also controls the mode of operation of the FFT processor. The DEF signal is produced from an address decode, and the control parameters are loaded from the host bus by connecting the AUX inputs to the data outputs.

REAL ONLY TRANSFORMS WITH A SINGLE DEVICE

In the simplest case real transforms can, of course, be computed by forcing zero levels on the imaginary input pins. The device can, however, be configured to internally perform two simultaneous real transforms instead of a single complex transform. The block floating point logic will then use data from both blocks when it determines the number of shifts to be applied. This dual transform technique is used to increase the maximum permissible sampling rates, but since an additional data pass is required in order to un-scramble the transformed data, the actual performance is not quite double that possible with a complex transform of the same size. The 4 x 64 point complex mode becomes an 8 x 64 real mode, but the change from 16 x 16 complex transforms to 32 x 16 real transforms is not supported.

When a real transform is performed the algorithm produces complex results for each of the incoming data blocks, but each result only represents the first half of the frequency domain data. This does not cause any loss of information since the two halves are mirror images of each other. As with complex transforms, it is necessary for a different system configuration to be used when 1024 point transforms are required. These are considered later, and the following only applies to 256 or 64 point transforms.

In a single device system, performing non overlapped transforms on data from a SINGLE source, only the Real input pins are used, and the Imaginary inputs are redundant except when configuring the device. By setting Control Register Bits 8:6 to 101, however, it is possible for a single device to accept data from two independent sources using the real and imaginary inputs. Maximum sampling rates will then only be half those possible when a single source is used, if no incoming data is to remain un-processed. With two sources a transform must be completed in the time to load parallel blocks, otherwise incoming data will be lost. With one source a transform need not be finished until two data blocks have been acquired. In this dual input mode results from data on the real inputs always precede those from the imaginary inputs.
If block overlapping is needed, it is always necessary to load pairs of data blocks simultaneously, using both the real and imaginary inputs. With dual sources of data this presents no problem, and Control Bits 8:6 should be set to 110 or 111 for the relevant amount of overlapping. If data is from a single source an external FIFO is needed to provide a simple delay for a block of data. Decodes 001 through 100 from Control Bits 8:6 must be used to select the required overlap.

The output of the FIFO must provide data for the real inputs. Continuous inputs can still be accepted, and each block will initially occur on the imaginary inputs, and then occur again on the real inputs as an output from the FIFO. The data output sequence will consist of the results from a pair of inputs, followed by the results obtained after the required overlap. Thus with 50% overlapping the sequence is 1 & 2 followed by 1.5 & 2.5 followed by 3 & 4 followed by 3.5 & 4.5 etc., where 1 2 3 4 are the sequential inputs to the external FIFO, 1.5 is the overlap between 1 & 2, and 2.5 is the overlap between 2 & 3.

When eight simultaneous 64 point transforms are performed, the sampling rates given in Table 5 assume that data is from a common source. The data outputs will be in the correct sequence from 1 to 8, corresponding to inputs 1 through 8 in normal order from a single source. When data is from two sources the sampling rates will be halved, and the output sequence will be 1A 1B 2A 2B 3A 3B 4A 4B, where A and B are the dual simultaneous sources on the real and imaginary inputs respectively. If data block overlapping is used in either of the above cases, the eight outputs will be followed by results from the same basic eight blocks but time displaced to give the required overlap. If more than two sources are to be handled the user must provide appropriate buffering and multiplexing, and the sampling rates must be proportionally reduced.

When two 1024 point transforms are performed with a single device, on data from a single source, the input buffer must be arranged to acquire two blocks before initialising a transfer to the device. In order to improve the maximum sampling rates possible, data should be read simultaneously from each half of the buffer, and loaded into the real and imaginary inputs. This halves the transfer time from the buffer to the device, but requires the device to expect dual inputs.

Configuration		Clock Periods
16 X 16PT	COMP	420
4 X 64PT	COMP	624
256PT	COMP	816
1024PT	COMP	3907
8 X 64PT	REAL	816
2 X 256PT	REAL	1032
2 X 1024PT	REAL	4699

Table 4. Computation Times in Clock Periods

Thus if block overlapping is not needed Control Register Bits 8:6 should be set to 101.

This fast transfer mode is supported by a special option on the PDSP16540 Bucket Buffer. It will acquire two 1024 point non overlapping blocks using the sampling clock, and then transfer the results to the FFT processor at the full system clock rate. Figure 8 shows the system arrangement. It does not support block overlapping.

With 1024 point transforms all block overlaps are handled by the buffer logic, and not by the internal RAM, but the device must still be programmed to expect the required overlap if the external buffer makes use of the in-active LFLG edge to mark the overlap point. To achieve the performance given in Table 5 with 50% overlaps, the buffer must provide sufficient storage for at least 2.5 data blocks. With 75% overlaps it must provide storage for 2.75 blocks. This extra storage allows transfers between devices to be only needed when a complete new block has been acquired for 50% overlaps, and when half a new block has been acquired for 75% overlaps. If storage is restricted to two data blocks, only half the sampling rates given will be possible. Transfers between devices must then occur when a half or a quarter of a new block has been acquired. Since the minimum time between transfers must be no less than the transform time itself, the sampling rates must be proportionally reduced to prevent loss of data.

SINGLE DEVICE SAMPLING RATES

In a single device system the maximum sampling rate is dependent on the transform size, the data overlap, and whether real or complex data is applied. Table 4 gives the times taken to complete the transforms for the various block sizes, which include an allowance for synchronisation between the DIS strobe and the system clock. If continuous data is to be transformed, the time to acquire a new block of data (or partial block with overlapping) must be at least equal to these transform times. Load and dump times must also be added in the 1024 modes. For non continuous transforms the peak rate is limited by the system clock rate and the factor , F,

16 X 16 COMPLEX			4 X 64 COMPLEX			256 COMPLEX			1024 COMPLEX			8 X 64 REAL			2 X 256 REAL			2 X 1024 REAL		
0%	50%	75%	0%	50%	75%	0%	50%	75%	0%	50%	75%	0%	50%	75%	0%	50%	75%	0%	50%	75%
23.9	-	-	16.1	8.0	4.0	12.3	6.1	3.0	6.8	3.4	1.7	24.6	12.3	6.1	19.5	9.7	4.3	12.1	6.0	3.0

Table 5 : Guide to MAX Sampling rates (in MHz) possible from a single device system.
SCLK is 40 MHz. Where sampling rate is asynchronous to SCLK, a PDSP16540 (or similar) is assumed on the input.

given previously.

The time taken to dump the transformed data must be no more than the load time, if continuous inputs are to be supported and I/O operations are concurrent with transforms. With block overlapping the dump time must be reduced to the time taken to load the partial block. This dump time must include four extra DOS strobes needed to prime the output circuitry when a transform is complete. These, in effect, can be added to the transform time such that with concurrent I/O and 0%, 50%, or 75% overlapping;

nS or (nS)/2 or (nS)/4 must be gtr than or equal to PK + 4W

where n is the transform size, S is the input DIS period, P is the number of clock periods given in Table 4, K is the system clock period, and W is the DOS period which can be less than S if necessary. Note also that S must be synchronous to SCLK, and if an asynchronous ratio is required then a pdsp16540 input buffer should be used.

When DIS and DOS are produced from a common source the minimum allowable sampling period must be increased to allow for the extra dumping time. Thus when DIS and DOS have equal periods and, for example, there is no overlapping;

(n - 4)S must be greater than or equal to PK

The maximum sampling rates given in Table 5 allow for the extra dumping time.

The load and dump operations are not concurrent with transforms in the 1024 point modes, and an external input buffer will be needed if loss of incoming data is to be avoided.

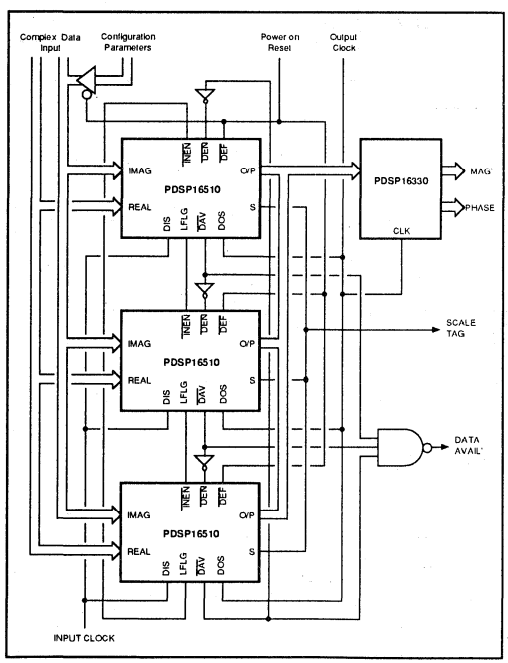


Fig 9. Multiple Device Configuration

This is loaded at the sampling rate and then data is transferred to the PDSP16510 at a user defined rate. The time taken to load this external buffer must be at least equal to the sum of the time to transfer data in and out of the FFT processor and the transform time itself. When data blocks are overlapped by 50% or 75%, no more than one half or one quarter of the block, respectively, must have been loaded in the same time. In the 1024 point modes the dump time can be any user defined value, and need not be increased to allow for block overlapping. The dump time, however , does directly effect the maximum sampling rates which can be accommodated without loss of incoming data.

The maximum sampling rates for 1024 point transforms at any load and dump rate can be calculated from the following relationship:

1024S or 512S or 256S > 1024B + PK + D

for 0%, 50%, or 75% overlapping respectively. S, P, and K were defined opposite. B is the clock period in which data is read from the input buffer and loaded into the device, D is the total dump time allowing for the four extra DOS periods. The periods of the load and dump clocks cannot be less than the system clock period. The maximum sampling rates given in Table 5 assume that a 40 MHz I/O rate is used, and that all results are dumped.

MULTIPLE DEVICE SYSTEMS

In real time applications several devices may be used in parallel in order to increase the sampling rate, but not to increase the transform size. When all outputs are commoned together, and feed a single output processor, then the data dump time must always be less than or equal to the time taken to load the data block (or 50% or 25% of the time with block overlapping). In most configurations with block overlapping the dump rate requirements will limit the maximum input rate, if only one output processor is provided. This can be avoided if the system provides separate output processors for every device. The system clock used for internal calculations then ultimately imposes a limit on the maximum sampling rate possible.

A multiple device system performing complex transforms with a single output processor is shown in Figure 9. The INEN/ LFLG signals are used to co-ordinate the segmentation of data between devices. The in-active going edge of LFLG instigates the load procedure in the next device, and, since this edge can be programmed to occur either 25%, 50%, or 100% through the load operation, it can cause the next device to commence loading before the previous one has finished. In this manner data block overlapping is achieved. When multiple concurrent transforms are performed (for example 4 x 64 or 8 x 64) two LFLG transitions are sometimes needed to support block overlapping. This is fully explained in the section on Mode 1 sampling rates.

In any of the multiple device modes an INEN edge transition is needed to start a new load procedure when the previous one has finished. When the LFLG output from the last device is fed back to the INEN input of the first device, continuous transforms will be executed. This continuous sequence can be started by the rising edge of DEF if Control Register Bit 12 is set in the first device (see section on Loading

Data). This bit must not be set in the other devices. Since all devices are supplied from a common input bus and have a common source of control parameters, this Bit 12 inversion is best mechanized with an Exclusive OR gate in the AUX12 input line of the first device. The input can then be inverted when DEF is active but otherwise not be effected. Once the first device has been started with the DEF edge, the sequence will continue automatically using the LFLG /INEN connection between devices.

In many applications data is transformed continuously after power on, and the concept of a first data sample does not exist. If, however , the opposite is true, the first data sample must be present on the input pins such that it can be loaded with the second rising DIS edge after DEF has gone in-active. The data must meet the set up and hold times given in Table 1, and DEF itself must meet the parameters normally met by the INEN rising edge. The latter requirement is necessary to avoid a possible one DIS cycle variance, due the internal DEF synchronization logic. If the position of the first data sample is not important, it is not necessary for DEF to have any set up specification.

Without the feedback from the last device, the first device would wait for another externally supplied initialising pulse. In such a system with N devices in parallel, then N continuous transforms must be executed before the first device can wait for a new INEN input.

When only one output processor is provided the data outputs from all devices are connected together, and internal logic will enable the tri-state outputs when a device is ready to output data i.e. DAV goes active. When data blocks are overlapped it is possible that the output rate requirements will limit the input sampling rate (see section on Multiple Device Sampling Rates). Additional output processors will remove this restriction, and the correct choice of multiple device operating mode will optimise the sampling rates that can be achieved with a given number of devices.

The synchronisation intervals, necessary to co-ordinate input and output operations with the transform operation, lead, in effect, to some uncertainty in the time needed to complete a transform. Thus a particular device in a multiple device system can effectively complete a transform in less system clock periods than another device in the same system. To prevent one device turning on its output bus before the previous one has finished, it is either necessary to use a faster output rate than would otherwise be required, or to use the inverted DAV output from one device to drive the DEN input of the next. The latter option allows DIS and DOS to be connected together, and ensures that the second device will not output data until the first device has finished.

This method of driving the DEN input from the inverted DAV output from a previous device requires a change to the single device DAV and DEN operation. If DEN is active at the end of a transform in a multiple device system, the DAV output will go active when the output circuit has been primed by the DOS strobes. This operation is identical to that provided for a single device system, and is transparent to the user as long as DEN and DOS are active . If DEN is not active, however, the DAV output will not asynchronously go active as happens in a single device system. Instead DAV will only go active when DEN eventually goes active. Since DEN is the inverted DAV output from a previous device, it is thus never possible for two devices to be actively outputting data. The DAV active going edge remains synchronised to the DOS strobe since the DEN input will only go active when a previous DAV goes in-active. A further change to the output circuitry ensures that the output buffer is primed even though DEN is not active. The first word, however, only progresses as far as the final output latch. The output bus is not enabled, and address increments do not

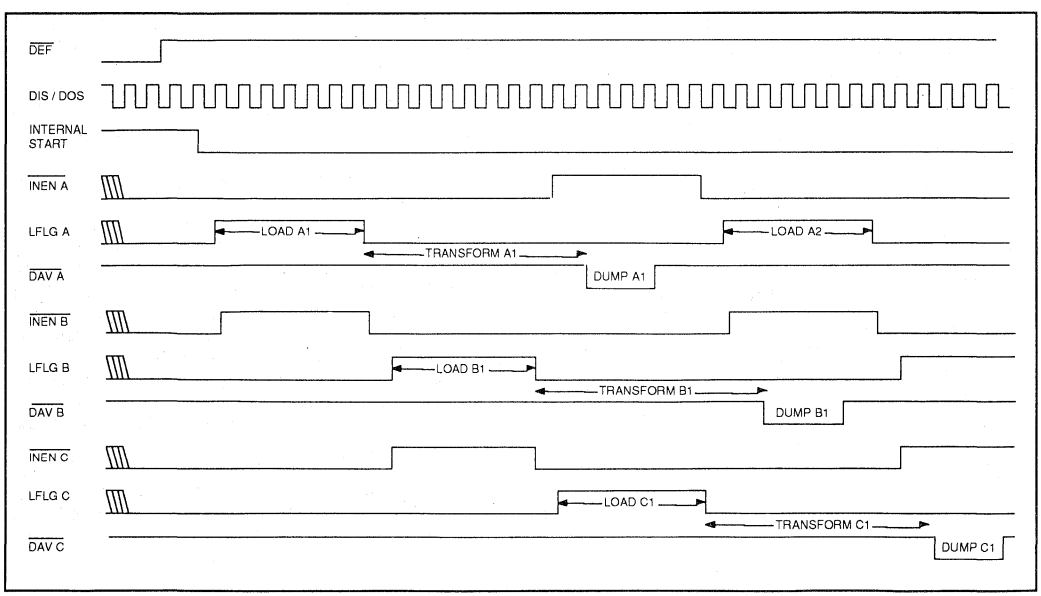


Fig 10. Three Device System with Separate Load, Transform, and Dump Operations

occur, until DEN is finally received. This modification to the internal control logic ensures that the output buffer does not impose unnecessary gaps between consecutive transforms. These gaps would, in turn, force the required DOS frequency to be greater than the DIS frequency (or greater than twice or four times the frequency with 50% and 75% overlaps).

The system illustrated by Figure 9 produces a common DAV output by OR'ing together all the individual, active low, DAV outputs. This is not guaranteed to give an indication when one transform has finished, and the next one has started, since it may simply glitch as one DAV goes in-active and the next one goes active after some delay. This glitch will not cause system problems since it occurs at a point clear of the high going edge of the DOS strobe. To provide a marker for the end of a transform each in-active going DAV edge should set its own latch, which is then reset by a subsequent DOS edge. The output of the latches can then be OR'd together if necessary.

Three multiple device operating modes are actually provided, and are selected with Control Register Bits 10:9. The choice of a particular mode is application dependent, and will effect the maximum sampling rate achievable with a given number of devices.

MULTIPLE DEVICE SAMPLING RATES

MODE 1. (BITS 10:9 = 01)

In this mode transfers in and out of the device are concurrent with transform operations. This mode must not be used for 1024 point transforms due to internal memory size restrictions. When real transforms are performed in this mode, only the real data input is used, regardless of the amount of block overlapping.

The increase in performance is directly related to the number of devices provided, but the input and output rates are limited to FØ where F and Ø are as defined previously. Within this restriction the theoretical performance is given by;

$$NnS > PK+4W, \quad \text{or } 0.5NnS > PK+4W, \quad \text{or } 0.25NnS > PK+4W$$

for 0%, 50%, or 75% overlapping. N is the number of devices, n is the transform size, S is the DIS strobe period, P is the number of system clock periods given in Table 4, K is the system clock period, and W is the DOS strobe period. Note that DIS should be synchronous to SCLK, and also that DOS should be synchronous to SCLK.

If an output processor is provided for every device, two devices with 50% block overlapping or four devices with 75% block overlapping will give the same sampling rates as a single device with no overlapping. If only one output processor is provided, the two or four times increase needed in the output rate over the input rate, usually imposes a limit on the input rate, since the output rate is limited to a factor, F, of SCLK.

In this operating mode the DIS and DOS strobes can often be tied together, since a faster DOS strobe gives no improvement in the sampling rates possible. This remains true even when the output rate must be twice or four times the input rate due to block overlapping. Options can then be used which internally divide the DIS strobe by two or four, and thus allow the input to be driven by the faster DOS strobe.

In this mode the LFLG goes in-active after 25%, 50%, or 100% of the block has been loaded. When multiple transforms are performed concurrently (for example 4 x 64) a LFLG transition occurs at the relevant point whilst the first block in the group is being loaded. LFLG then goes high again and returns low at the overlap point in the last block. This double LFLG transition allows two devices to support 50% block overlapping, since the first transition from the first device can be used to initiate the load procedure in the second device. The second transition from the second device then initiates a new load procedure in the first device. The additional edges from each device have no effect since they occur when the device they are driving is already doing a load operation.

In such a two device system supporting 50% overlaps the inverted DAV from the first device must drive the DEN input of the second device. The data dumping time is then shared equally between both devices. The second device only outputs data when the first has finished, but both dumps must be finished in the time taken to load the group of blocks if only one output processor is provided. Without the DAV/DEN connection one device would only have had the time needed to load half of one sub block in which to dump its data.

In a similar manner four devices will handle 75% overlaps when concurrent multiple transforms are to be computed. The second, third, and fourth devices make use of the first transition, and ignore the second. The first device uses the second transition from the last device, and ignores the first. With the DAV/DEN connection each device will have one quarter of the load time to dump its data when a single output processor is provided .

More than two devices will provide increased performance for multiple transforms with 50% overlapping, and more than four devices will increase the performance with 75% overlapping. External logic is then needed to ensure that each device only uses the correct LFLG transition. Any device should only use the negative LFLG transition from a previous device if its own LFLG is low, and the LFLG output from the previous device plus one is low.

MODE 2 (BITS 10:9 = 10)

This mode is suitable for all transform sizes, since separate load, transform, and then dump operations occur. More devices than required by Mode 1 are necessary to achieve a given sampling rate, but the input and output rates can be any value up to the full system clock rate with the A grade part. As with Mode 1, additional output processors are needed to avoid the sampling rate restriction imposed by block overlapping.

The number of devices, N, needed to achieve a given sample rate can be derived from the following formula:

$$NnS > nS + PK + D \text{ for no overlapping}$$
$$NnS > 2\,X\,[nS + PK + D] \text{ for 50\% overlapping}$$
$$NnS > 4\,X\,[nS + PK + D] \text{ for 75\% overlapping}$$

N is the number of devices, n is the transform size, S is the DIS strobe period, P is the number of system clock periods given in Table 4, K is the system clock period, and D is the total dump time including 4 extra DOS periods as discussed previously. The DIS and DOS periods are any value defined by the user, down to the system clock period with the A grade part. Note that DIS should be synchronous to SCLK, and also DOS

should be synchronous to SCLK.

In this mode increasing the output clock frequency will allow a greater continuous input rate. The provision of separate DIS and DOS pins allows this to be mechanized, and the DOS frequency can be increased to that of the system clock used internally. When the sum of the dump time (including four extra DOS periods for output priming) plus 12 system clock periods (the transform time variation caused by input synchronization) is less than the load time, one device will be guaranteed to have finished dumping before the next one starts. The inverted DAV to DEN connection between devices is then not needed, and all DEN inputs can be grounded.

The LFLG transitions occur at the same times as Mode 1, except that the double transition does not occur with multiple concurrent transforms. Fig. 10 illustrates a timing sequence with three devices. Real transforms still only use the real inputs regardless of the amount of block overlapping.

MODE 3 (BITS 10:9 = 11)

Multiple device Mode 3 is provided in order to improve the performance when block overlapping is needed, and separate output processors are provided. In this mode transfers in and out of the device are never concurrent with transform operations. The device will actually load extra data such that the required data to perform two overlapped transforms is stored internally. The amount of internal RAM prohibits the use of this mode when performing overlapped 1024 point transforms. LFLG will go in-active after a normal data block have been loaded, regardless of the overlap selected. The device, however, continues to load more data. Thus, for example, in the 4 x 64 mode, five 64 point blocks will be loaded. This technique allows each device in the system to complete two or four overlapped transforms (depending on the amount of overlap) before any new data is needed. When doing a straightforward 256 point transform the device will load 256 + 128 data points.

The full benefits are only obtained if more than one output processor is provided, but an extra processor is not always necessary for every device. Sampling rates up to the system clock rate are possible. The equations defining the sampling rates become:

$(N - 1)L > 2PK + 2D$ for 50% overlaps
$(N - 1)L > 4PK + 4D$ for 75% overlaps

where L is the time needed to load a normal block of data but not including the extra data, P is the number of system clock periods given in Table 4, K is the system clock period, and D is the total dump time including 4 extra DOS periods. As before, both DIS and DOS must be synchronous to SCLK.

When real transforms are to be performed on single sourced data, an external FIFO is needed to provide pairs of data blocks. These are loaded simultaneously into the real and imaginary inputs. See the section on real transforms.

OPERATING MODES

The operating mode of the PDSP16510 is determined by the condition of 16 bits in an internal Control Register. The status of these bits is defined by the inputs present on the AUX15:0 pins when the DEF input is active. The DEF input can be a simple power on reset if the operating mode is fixed once power is supplied. The AUX pins are also used to provide the imaginary component of the complex input data. Thus, if complex inputs are needed, the mode definition must be implemented through a tri-state buffer which is only enabled when DEF is active. The imaginary input data must be disabled during this time.

Table 6 lists the functionality of each of the bits in the mode control register, and further explanations are as follows:-

BITS 2:0

These bits define one of 7 options for the sample size and type of data. In the 1024 point options the device will assume the non concurrent operating mode, regardless of whether a single or multiple device system is specified. The internal control logic will then ensure that data is loaded, transformed, and dumped in sequential operations.

For other data set sizes, loading, transforming, and dumping, can all occur simultaneously with a single device; the actual overlap will be dependent on the relative occurrences of the INEN input. Only in Mode 1 can concurrent operations be done with multiple devices.

BIT 3

This bit determines the number of right shifts built into the data path. In either condition only two right shifts occur during the first pass. If the bit is reset, three shifts occur in subsequent passes and the block floating point scheme allows up to fifteen compensating left shifts. If it is set, two shifts occur in every pass and overflow is possible. This is indicated by reducing the number of compensating left shifts to fourteen, and using scale tag value fifteen to indicate that overflow has occurred.

BITS 5:4

These bits define the choice of window operator. If other windows are needed they must be applied externally. The fourth option is used to specify the inverse transform, which does not require the use of a window operator. When 16 x 16 complex transforms are specified by Bits 2:0, only the rectangular window can be used. The use of any of the other options will cause the device to enter an internal test mode.

BITS 8:6

These bits define 0%, 50%, or 75% data block overlapping, and the division factor on the DIS input. Overlapping must not be specified with 16 x 16 complex transforms. Two decodes allow the DIS input to be divided by two or four, when 50% and 75% overlapping is respectively needed. These options allow the DOS and DIS input pins to be still supplied from a common source, even though the output rate must be faster than the input rate. The frequency of this source would be dictated by the output rate requirement, with the input rate internally reduced by the correct amount.

Special decodes are provided to support real only transforms from dual sources, using both the real and auxiliary inputs. When data is from a single source, and no overlaps are needed, only the real input should be used. If 50% or 75% overlaps are needed from a single source of real data, the device always expects blocks to be simultaneously loaded. An external FIFO is then needed to supply data to the real inputs after a delay of one block. Each block is thus loaded twice,

firstly through the Auxiliary inputs and then through the Real inputs.

BIT 10:9

These bits define a single device system, or one of three multiple device possibilities. The choice between the first and second multiple device mode is dependent on the transform size and the sampling rate needed. The third mode should only be used when overlapped multiple transforms with less than 1024 points are to be performed simultaneously. It changes the LFLG logic and allows sampling rates up to the system clock rate to be achieved with multiple output processors.

BIT 11

BITS	Dec'	OPTION
2:0	000	16 x 16 COMPLEX
	001	4 x 64 COMPLEX
	010	256 COMPLEX
	011	1024 COMPLEX
	100	8 X 64 REAL
	101	2 X 256 REAL
	110	2 X 1024 REAL
	111	NOT USED
3	0	SHIFT 3 PLACES AFTER PASS1
	1	ALWAYS SHIFT 2 PLACES
5:4	00	RECTANGULAR
	01	HAMMING WINDOW
	10	BLACKMAN-HARRIS
	11	INVERSE TRANSFORM
8:6	000	NO OVERLAP
	001	50% OVERLAP
	010	50% OVERLAP AND DIS ÷ 2
	011	75% OVERLAP
	100	75% OVERLAP AND DIS ÷ 4
	101	DUAL SOURCE, NO OVERLAP
	110	DUAL SOURCE, 50% OVERLAP
	111	DUAL SOURCE, 75% OVERLAP
10:9	00	SINGLE DEVICE
	01	N DEVICES, CONCURRENT I/O
	10	N DEVICES, LOAD-TRANS-DUMP
	11	SPECIAL MULTIPLE TRANSFORM
11	00	DAV NOT DELAYED
	01	24 CLK DAV DELAY
12	0	INEN EDGE ACTIVATED
	1	INEN IS SIMPLE ENABLE
14:13	00	O/P FIRST QUARTER
	01	O/P FIRST HALF
	10	O/P LAST HALF
	11	O/P ALL RESULTS
15	0	NORMAL DAV
	1	KEEP DAV ACTIVE TILL INEN

Table 6. Mode Control Bit Allocations

When this bit is set the PDSP16510 will not generate DAV until 24 DOS clocks after data was actually valid. In this case the output tri-state drivers will be enabled at the correct time, even though the DAV signal was not externally valid. Host controlled dumping should not be used.

BIT 12

When this bit is set in the single device mode, the INEN input is a simple load enable signal. When it is reset an INEN edge is needed at the end of a load sequence before a new one can commence.

When it is reset in a multiple device mode it has no action, but when it is set it will cause the DEF high going edge to also initiate a load operation.

BIT 14:13

These bits allow four dump size options to be provided. Individual frequency bins are not accessible.

BIT 15

Under normal circumstances DAV would be expected to go invalid when a transform has been dumped. In some applications, however, it may be necessary to read the outputs more than once. When this bit is set, DAV will remain valid until the next INEN input, and will indicate that the transformed data still remains in the internal buffer. As soon as the next INEN is received the transformed data will be overwritten. Whilst DAV remains active the output tri-states will be enabled.

WINDOW OPERATORS

Since only a finite segment of a signal can be observed and processed at any one time, it is impossible to obtain pure spectral lines. Discontinuities are introduced at the boundaries of the observation interval which lead to spectral leakage. Windows are weighting functions applied to the data in order to reduce these discontinuities at the boundaries.

In the time domain the signal has to be observed through a finite window as a matter of accord. This is in fact equivalent to multiplying the signal with a set of uniform weights i.e. a rectangular window operator. In the frequency domain the spectrum of the data will be the spectrum of this weighting function shifted to the sinusoidal frequencies of the components in the data.

The rectangular window has a Fourier Transform which is a SINC(X) function. This has sidelobes which are only 13dB down from the main lobe. This severely limits the dynamic range of the system since a second sinusoid in close proximity would have its main lobe swamped by this side lobe. This would occur if its amplitude was a mere 13dB down from the first sinusoid.

Window operators are thus mathematically constructed to cancel these sidelobes as far as possible. Unfortunately this is normally done at the expense of making the main lobe spread over more frequency bins. This reduces the ability of the system to resolve two frequencies, and can only be overcome by using more data samples. This may not always be possible because of other system constraints.

A common rule of thumb defines the resolution of an FFT system as half the full width of the mainlobe. The width of the mainlobe for a rectangular window is two frequency bins; for the Hamming window it is four bins; for the Blackman-Harris

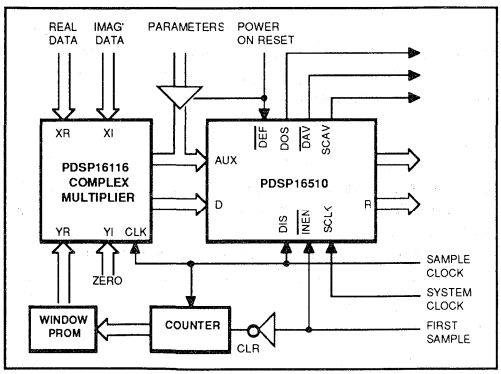


Fig. 11. External Window Generator

window it is six bins.

The latter two windows are actually supported by the PDSP16510. These are constructed on the fly as needed, and take the general form:

A - Bcosx + Ccos2x where x = (2πn)/N, n = 0 to N-1

For Hamming, A = 0.54, B = 0.46, C = 0

For Blackman-Harris, A = 0.42323, B = 0.49755,C=0.07922

These windows can be applied to any of the transform size options, except the 16 x 16 complex variant. When the latter is specified the rectangular window option MUST be selected, or the device will be configured in an internal test mode.

If other operators are required these must be applied externally. This can be conveniently achieved with either a PDSP16112 or a PDSP16116, both of which are complex multipliers but with different accuracies. Fig. 11 shows how either one can be configured to perform two separate multiplications with one input common to both. This arrangement is necessary to perform the window function on complex inputs.

Important features of the windows generated by PDSP16510, and other commonly used windows, are illustrated in Table 7. The results are obtained from the reference quoted, which should be consulted for a full mathematical treatment. The significance of each parameter is outlined below :

Highest Side Lobe Level

The inherent rectangular window has sidelobes which are only 13dB down from the mainlobe. These severely limit the dynamic range. The object of the window is to improve this situation with better side load attenuation.

Mid-Point Loss

In line with the filter concept it is possible to conceive of an additional processing loss for a tone of frequency mid-way between two bins. This is defined as the ratio of the coherent gains of two tones, one at the mid-point and one at the sample point. It is expressed in dB in Table 8.

Overall loss

An overall figure for the reduction in signal to noise ratio can be obtained by adding the mid-point loss to the reciprocal of the equivalent noise power bandwidth in dB. It is a measure of the ability of the window to detect single tones in broadband noise. The variance between windows is less than 1dB.

6.0dB Bandwidth

This figure, expressed in bin widths, represents the ability of the window to resolve two tones and should be as close to unity as possible. As the highest sidelobe level is reduced, this parameter tends to get worse, and a compromise must be used when choosing a window.

Overlap Correlation

In many practical systems the squared magnitudes of successive transforms are averaged to reduce the variance of the measurements. If, however, a windowed FFT is applied to non overlapping partitions of the sequence, data near the boundaries will be ignored since the window exhibits small values at those points. To avoid this loss partitions are usually overlapped by 50% or 75%, which might, at first sight, remove the need to average successive transforms. If non-windowed

Window Operator	Highest Side Lobe	Mid-Point Loss dB	Overall Loss dB	6dB Bandwidth	Overlap Correlation	
					75%	50%
Rectangular	-13	3.92	3.92	1.21	75	50
Hamming	-43	1.78	3.1	1.81	70.7	23.5
Dolph-Chebyshev [C = 3.5]	-70	1.25	3.35	2.17	60.2	11.9
Kaiser-Bessel [C = 3]	-69	1.02	3.55	2.39	53.9	7.4
Blackman	-58	1.1	3.47	2.35	56.7	9
Blackman-Harris [3 term]	-67	1.13	3.45	1.81	57.2	9.6

Table 7. Window Performance (from The use of Windows for Harmonic Analysis. F J Harris. Proc IEEE Vol 66. Jan 1978)

Arithmetic Accuracy	Max Tone WRT Noise	Slot Noise Test	2 Tones with Freq Spread
16 bit,unconditional scaling	60	44	45
24 bit arithmetic with unconditional scaling, 16 bit inputs	88	67	65
16 bit inputs with PDSP16510 block FP	74	61	63
Full 32 bit Floating point with 16 bit inputs	93	82	67

Table 8. Comparative Dynamic Range Measurements

transforms are overlapped by 75% or 50%, then 75% or 50% of the data will be correlated. When windows are applied, however, the data common to both transforms will be operated upon by different portions of the window waveform. The difference in these portions will dictate the amount of correlation between overlapped data. At 50% overlap Table 7 shows that with all windows the data is virtually independent, and successive averaging would still be needed. At 75% overlap figures are obtained which are closer to the 75% correlation obtained with no window.

Examination of Table 7 shows that the Blackman-Harris window gives performance very similar to that of the Kaiser-Bessel and Dolph-Chebyshev windows. The latter two windows can not be computed as they are needed since they are mathematically too complicated. The values are normally precomputed and stored in a ROM; this would need to contain 1M bits to match the accuracy of the rest of the system.

Use of the Hamming window gives worse dynamic range than the more complex windows, but it has less effect on the overlap correlation and it has a smaller main lobe width.

SPECTRAL PERFORMANCE

There are two important parameters in the measurement of spectral response: resolution and dynamic range. Resolution defines how closely two sinusoids can be spaced in frequency and still be identified; dynamic range defines how great the difference in the amplitudes of the sinusoids may be and yet the smaller one still identified. Resolution is determined by the observation time [i.e. the width of the frequency bin] and the window operator that is used. Dynamic range is also determined by the window operator, but in a hardware implementation it is also influenced by the number of bits used to represent the data throughout the calculation.

The hardware effects include the accuracy of the A/D converter, the number of bits representing the window operator and the twiddle factors, and the way the growth in word length is handled as the FFT calculation proceeds. The obvious way to overcome these limitations is to use floating point arithmetic; but in real life the accuracy of the A/D converter is fixed and the sample size is limited. Floating point arithmetic is thus an overkill solution for the majority of applications. This is especially true for transform sizes up to 1024 points, which is the intended application area.

Figures given for the dynamic range of a system must be carefully interpreted, since there is no exact definition of the measurement. Three different ways of measuring dynamic range have been investigated using 1024 point transforms.

The 'best' dynamic range figures will be obtained with single tone measurements, and these results are often quoted to indicate the need for greater bit accuracies. The measure is the ratio of a full scale sinusoid to the average noise level and the results will be essentially independent of the window operator. The results given by the PDSP16510 are compared to various other configurations in the first column of Table 8. With this method the dynamic range is bound to improve as more bits are used to represent the data. Theoretically 6 dB of dynamic range will be obtained for every bit representing the input data, if the internal arithmetic accuracy gives no degradation in performance. In practice this improvement has no significance since the incoming waveforms will be much more complex than a single sinusoid.

An alternative method of determining dynamic range is with a slot noise test. White noise is passed through a narrow-band notch filter, several frequency bins wide, and the FFT computed. There is no noise in the filtered slot at the input to the FFT, but there is noise in the frequency bins corresponding to the width of the notch. Dynamic range is measured as the difference in dB of the average signal power and the average noise power and can be considered to give more useful results. Comparative results from various configurations are also given in the second column of Table 8. The performance with 24 bit data is seen to be little better than that obtained with the PDSP16510. This can be attributed to the scaling scheme, word growth, and rounding method used within the device.

When two nearby tones are to be capable of detection, the window operator will dictate the performance of the system. The final column in Table 8 illustrates the results obtained using two sinusoids of different amplitudes, with the larger one residing mid-way between two frequency bins, and the smaller 5.5 bins away. The two frequencies are five bins apart to avoid the effects of the mainlobe widths. The dB figures given are the difference in amplitude between the two signals when the smaller one is still just detectable as a separate peak from the larger one.

This technique illustrates the performance of the window, since the amount by which sidelobe structure of the larger signal swamps the mainlobe of the smaller signal will determine if the smaller is detected. The theoretical attenuation of the highest sidelobe levels, with respect to the mainlobe, for the window options provided by the PDSP16510 have been given in Table 7, and represent the dynamic range that can be obtained if arithmetic effects are ignored. The results in the final column in Table 8 are the practical results given by the device, and as with the slot noise test indicate that the arithmetic scheme used by the PDSP16510 is equivalent to using 24 bit data. The Blackman Harris window was used in all cases.

USER NOTES - STOPPING DOS

(1) GENERAL DESCRIPTION

The transform is calculated internally fully synchronous to SCLK. However, as all outputs are referenced to DOS, a transfer has to be made between the two clocks. In addition, some dummy DOS strobes are needed to operate the internal control logic, and to advance data from the internal RAMs to the output pins.

The most simple configuration for the device is to have DOS running continuously and for DEN to be permanently active. When this happens the user will just be aware of data appearing on the output pins on the same DOS cycle when DAV goes active. However, there are many situations where either DOS is not continuously running, or DEN is not permanently active. To help explain how to operate the device in these situations, the internal operation of the output circuits must be described. For those who are not going to be interrupting DOS, the remainder of this section can be ignored.

(2) INTERNAL RAM - GENERAL DESCRIPTION.

For single device operation of transforms less than 1024 points, the internal RAM is shared between three separate operations which enable the device to output old transformed results, calculate the current transform, and input new data ready for the next transform. All these operations, along with the internal control logic, are controlled by a 12-cycle state machine. The RAM operations are:

(a) 2 cycles in every 12 are dedicated to reading new information in the input buffer and writing it to the RAM.

(b) 2 cycles in every 12 are dedicated to reading the contents of the RAM and advancing that data to the output buffer.

(c) 8 cycles in every 12 are dedicated to the read and write operations of the transform currently being calculated.

(3) SEQUENCE OF EVENTS

The sequence of events relating to the output control and data flow is as follows :

(3.1) An SCLK rising edge :

(a) An internal flag is raised to indicate that the transform has finished and data is available to be dumped. Data will be present in the internal RAM, and the output address generator will be at the correct address. Access to the RAM at this moment, however, has not been made.

(b) If at this moment the device is programmed to be a single device, and DEN is inactive, then DAV will be made active - ie without the presence of DOS. If DEN is active at this point, or the device is programmed in any multiple device mode, then DAV will remain inactive.

(3.2) Accessing the RAM at this point

At this moment, when DAV has been made active before data appears on the output pins, data is not yet in the output buffer. Internally the precise SCLK cycle at which the RAMs are read and written to the output buffers now has to be waited for. This cycle, as described above occurrs 2 in every 12 SCLK cycles, so at worst case 6 SCLK cycles have to elapse until data is guaranteed to be in the output buffer.

If the DOS rate is similar to the SCLK rate, and the user has been immediately applying DOS pulses (on seeing DAV go active) hoping to get data off the chip, then this will not actually happen.

The next internal flag raised is the one which indicates that the output data has been successfully read from the RAMs and is now in the output buffer.

(3.3) The next DOS rising edge (regardless of DEN status)

The flag indicating that the RAMs have been read is transferred to circuitry operating on DOS. The output enable signal, DEN, does not have to be present at this point.

(3.4) The next DEN-Enabled DOS rising edge (ie the 1st one of this sequence)

The output state machine receives it's first edge.

(3.5) The next DEN-Enabled DSO rising edge (ie the 2nd)

Internal output address generators start to count (ready for fetching the next set of output data).

(3.6) The next DEN-Enabled DOS rising edge (ie the 3rd)

An enable signal is raised for the final data latch in the output buffer.

(3.7) The next DEN-Enabled DOS rising edge (ie the 4th)

(a) The final data in the output buffer latch clocks-through new data and presents it to the output pads.

(b) The output pads come output of high impedance

(c) If DAV was previously inactive, it is now made active.

(4) OUTPUT SCENARIOS

Considering the above sequence, therefore, some single device situations can now be explained :

(4.1) DOS is continuously present, but DEN is inactive (Transform size less than 1024)

In this case, when the transform is complete, as the device is programmed as a single device and DEN is inactive, DAV will be made active. Even though DOS is running, the status of DAV at this point does not rely on it.

The user can now monitor the status of DAV, and after at least 6 SCLK cycles can initiate some further action, eg by external control force DEN active at some later time when the rest of the system is ready to accept the transformed data. Independently of this external control, the next DOS pulse will start to operate the sequence of events as described above (ie point No. 3.3). When DEN is eventually made active, the remainder of the above sequence (points Nos 3.4 to 3.7) is executed, with 4 DEN-Enabled DOS pulses needed before data is observed on the output pins.

If however the user immediately forces DEN active upon monitoring DAV go active and waiting for the required 6 SCLK cycles, then 5 DOS pulses would have to be issued. The first of these 5 would start the sequence of events as described above (3.3), and the fact that it is enabled by DEN would be irrelevant. The required DEN enabled pulses in this situation would be the 2nd, 3rd, 4th and 5th pulses supplied.

(4.2) DOS is not running, and DEN is inactive. (Transform sizes less than 1024)

In this situation, again as the device is programmed to be a single device and DEN is inactive at the point where the transform is complete, DAV will be made active regardless of the state of DOS. The user can now monitor this event on DAV and after waiting a further 6 SCLK cycles, use it to switch on DOS and to make DEN active.

DOS can now be switched on for at least one pulse (but may be more), and the sequence of events as described earlier (from point No 3.3) will start. DEN can then be made active, whereby a further 4 DEN-Enabled DOS pulses will be required before data is seen on the output pins. This is the situation shown in table 3.

Alternatively, DEN and DOS could be made to operate on the same cycle. In this case data will appear on the output pins on the 5th DOS pulse (the first would not actually require the presence of DEN, but the 2nd, 3rd, 4th and 5th would)

(4.3) 1024 point transforms, single device mode.

In the case of 1024 point transforms, the internal RAM is no longer operated in the manner described in section 2. The RAM is instead totally dedicated to one operation at a time. Thus data for a transform will be loaded, and all 12 out of 12 SCLK cycles will be available for the transfer of input data to the RAMs. During the transfrom no transfers from the input to the RAM or from the RAM to the output are possible. This is why DIS and DOS can be equal to SCLK for 1024 point transforms.

If 1024 point transforms are being performed and the device is programmed as a single device, then "asynchronous" operation of DAV is possible as described earlier for transform sizes less than 1024 points. If DEN is inactive at the time the transform has finished calculating, then DAV will be made to go active regardless of the state of DOS. Although 6 SCLK cycles do not have to be waited for as in section 3.2, a transition has to be made from the transform controlling the internal RAM to the output circuits cnotrolling it. This operation plus the time taken to advance data from the RAMs to the output buffer takes exactly 4 SCLK cycles.

Hence the sequence of events is exactly as described in section 3, except that section 3.3 should read 4 SCLK cycles rather than 6. The analysis of sections 4.1 and 4.2 are also true if the 6 SCLK cycle time is substituted with 4 SCLK cycles.

(5) DUMMY DOS STROBES AFTER DEF

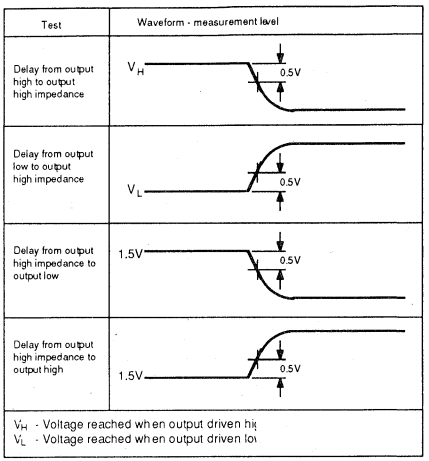
In addition to the dummy DOS strobes needed prior to dumping data, it is necessary to provide at least 4 DOS strobes after DEF has gone inactive, but before DAV goes active. These initialise the internal address counters and do not rely on DEN also being active. They are needed every time DEF has been used to change the operating mode.

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage Vcc	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to Vcc + 0.5V
Output voltage V_{OUT}	-0.5V to Vcc + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HMB)	500V
Storage temperature T_S	-65°C to 150°C
Junction Temperature, Commercial	100°C
Junction temperature, Industrial	115°C
Junction Temperature, Military	155°C
Package power dissipation	5000mW

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as positive into the device.



ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise state)

PDSP16510A C0 Tamb = 0 C to + 70°C. Vcc = 5.0v ± 5%
PDSP16510A B0 Tamb = -40 C to + 85°C. Vcc = 5.0v ± 10%
PDSP16510A A0 Tamb = -55 C to +125°C. Vcc = 5.0v ± 10%

Characteristic	Symbol	Value			Units	Notes
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.0		-	V	SCLK, DIS, DOS, DEN need 3V
Input low voltage	V_{IL}	-		0.8	V	DEN needs 0.7V max
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{CC}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{CC}
Output S/C current	I_{SC}	10		300	mA	V_{CC} = Max

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Max	Conditions
Clock Frequency (MHz)	Ø	DC	40	Max Ø high time is 1msec
Clock High Period (ns)	T_{CH}	13		
Clock Low Period (ns)	T_{CL}	10		
Max DOS, DIS Frequency	$Ø_D$		FØ	Less than 1024 points or Mult Dev Mode 1 Note $F = \frac{4}{6 + 0.001ØT_{CL}}$
Max DIS Frequency	$Ø_D$		Ø	1024 points or Mult Dev Modes 2 and 3
Max DOS Frequency	$Ø_D$		Ø	

SCLK to DIS/DOS RELATIONSHIP
Both DIS and DOS must be synchronous to SCLK. Ideally they should both be produced from SCLK, in which case the SCLK rising edge would either be first or coincident with the DIS and DOS rising edges.
In any event, the rising edge of SCLK must not fall between 2ns and 10ns after the rising edge of either DIS or DOS

ORDERING INFORMATION

PDSP16510A C0 AC	(Commercial -PGA Package)
PDSP16510A C0 GC	(Commercial -Leaded Chip Carrier)
PDSP16510A B0 AC	(Industrial - PGA Package)
PDSP16510A B0 GC	(Industrial - Leaded Chip Carrier)
PDSP16510A A0 AC	(Military - PGA Package)
PDSP16510A A0 GC	(Military - Leaded Chip Carrier)
PDSP16510A/MA/GCPR	(Military - Screened Leaded Chip Carrier. See separate datasheet for details)

PDSP16515A

STAND ALONE FFT PROCESSOR WITH ENHANCED INTERNAL ACCURACY

The PDSP16515A performs Forward or Inverse Fast Fourier Transforms on complex or real data sets containing up to 1024 points. Data and coefficient input are both represented by 16 bits. Data is expanded internally to 18 bits and subject to Block Floating Point arithmetic to preserve a greater dynamic range.

An internal RAM is provided which can hold up to 1024 complex data points. This removes the memory transfer bottleneck, inherent in building block solutions. Its organisation allows the PDSP16515A to simultaneously input new data, transform data stored in the RAM, and to output previous results. No external buffering is needed for transforms containing up to 256 points, and the PDSP16515A can be directly connected to an A/D converter to perform continuous transforms. The user can choose to overlap data blocks by either 0%, 50%, or 75%. Inputs and outputs are synchronous to the 40MHz system clock used for internal operations.

A 1024 point complex transform can be completed in some 98µs, which is equivalent to throughput rates of 450 million operations per second. Multiple devices can be connected in parallel in order to increase the sampling rate up to the 40MHz system clock. Six devices are needed to give the maximum performance with 1024 point transforms.

Either a Hamming or a Blackman-Harris window operator can be internally applied to the incoming real or complex data. The latter gives 67dB side lobe attenuation. The operator values are calculated internally and do not require an external ROM nor do they incur any time penalty.

The increased internal bus size together with block floating arithmetic produce up to 85dB of noise rejection.

The device outputs the real and imaginary components of the frequency bins. These can be directly connected to the PDSP16330 in order to produce magnitude and phase values from the complex data.

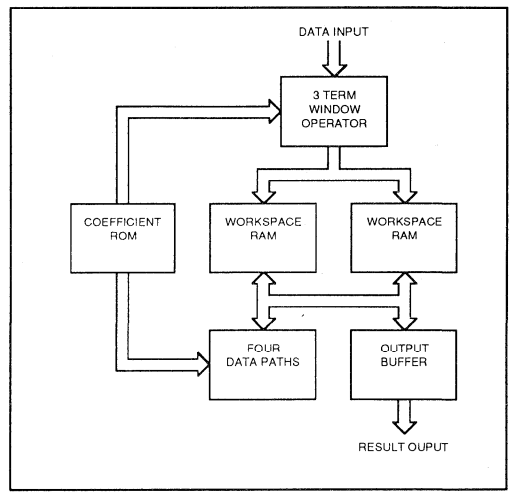


Fig. 1. Block Diagram

FEATURES

- Completely self contained FFT Processor
- Pin and functionally compatible with the PDSP16510A
- Expanded width internal RAM supports up to 1024 complex points
- 18 bit internal data bus with block floating point arithmetic for increased dynamic range
- 450 MIP operation gives 98 microsecond transformation times for 1024 points
- Up to 40MHz sampling rates with multiple devices.
- Up to 85dB noise rejection
- A choice of internal window operators with no external ROM provide up to 67dB side lobe attenuation.
- 84 pin PGA or 132 pin surface mount package

ASSOCIATED PRODUCTS

PDSP16540 Bucket Buffer
PDSP16330 Pythagoras Processor.
PDSP16256 Programmable FIR Filter.
PDSP16350 I/Q Splitter / NCO
PDSP16510A Stand Alone FFT Processor

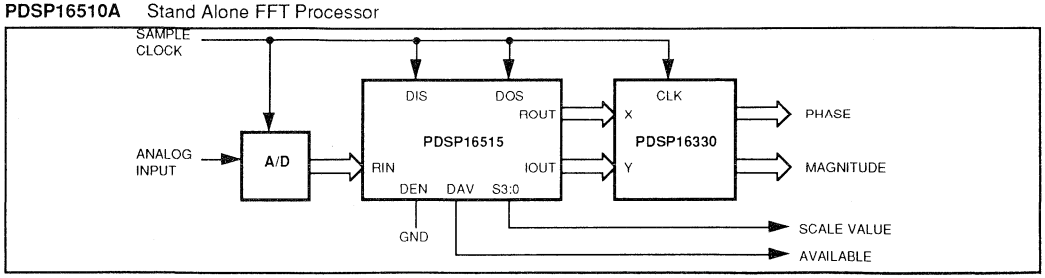
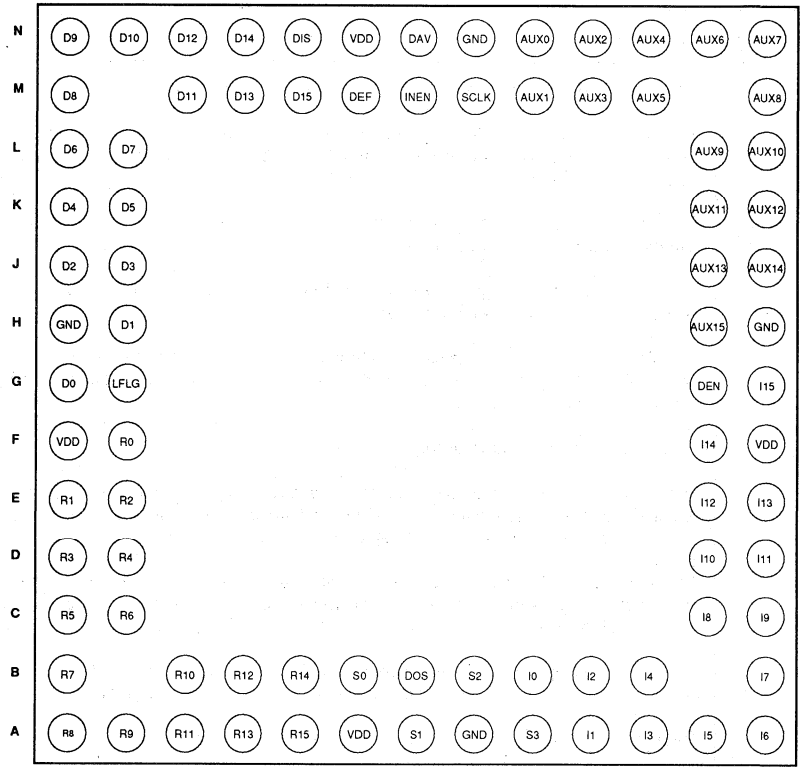


Fig. 2. Typical 256 Point Real Only System Performing Continuous Transforms



Pin Out for 84 PGA Package (AC84) - bottom view

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	VDD	23	AUX13	45	GND	67	D8	89	GND	111	GND
2	GND	24	VDD	46	VDD	68	D7	90	R3	112	S1
3	I7	25	AUX12	47	SCLK	69	D6	91	VDD	113	GND
4	I8	26	GND	48	GND	70	D5	92	R4	114	DOS
5	I9	27	AUX11	49	GND	71	GND	93	GND	115	DOS
6	I10	28	VDD	50	DAV	72	VDD	94	R5	116	VDD
7	VDD	29	GND	51	GND	73	D4	95	R6	117	S2
8	I11	30	AUX10	52	INEN	74	GND	96	R7	118	GND
9	GND	31	AUX9	53	VDD	75	D3	97	R8	119	S3
10	I12	32	AUX8	54	DEF	76	VDD	98	GND	120	GND
11	VDD	33	AUX7	55	GND	77	D2	99	VDD	121	VDD
12	I13	34	VDD	56	DIS	78	GND	100	R9	122	I0
13	GND	35	AUX6	57	VDD	79	D1	101	VDD	123	I1
14	I14	36	VDD	58	D15	80	VDD	102	R10	124	GND
15	VDD	37	AUX5	59	D14	81	D0	103	R11	125	I2
16	I15	38	GND	60	GND	82	LFLG	104	R12	126	I3
17	GND	39	AUX4	61	D13	83	GND	105	R13	127	I4
18	DEN	40	AUX3	62	D12	84	R0	106	GND	128	GND
19	AUX15	41	AUX2	63	D11	85	GND	107	R14	129	VDD
20	GND	42	VDD	64	D10	86	R1	108	R15	130	I5
21	AUX14	43	AUX1	65	VDD	87	VDD	109	DISAB	131	I6
22	GND	44	AUX0	66	D9	88	R2	110	S0	132	VDD

Pin Out for 132 Leaded Chip Carrier (GC132)

SIGNAL	TYPE	DESCRIPTION
D15:0	I	Data input during real only mode. The real component in complex data mode.
AUX15:0	I	When DEF is active AUX15:0 are used to define the operating mode as defined in Table 3. When DEF is in-active AUX15:0 either provide the 16 bit imaginary component of complex input data, or a second set of real only inputs.
R15:0	O	These pins output the real component of the transformed data when DAV and DEN are active. Otherwise they are high impedance.
I15:0	O	These pins output the imaginary component of the transformed data when DAV and DEN are active. Otherwise they are high impedance.
$\overline{DEF}$	I	The high going edge of DEF is used to internally latch the contents of AUX15:0, which then define the operating mode. In the simplest system DEF is a power on reset. When DEF is low the internal control logic is reset.
SCLK	I	System clock used for internal computations.
S3:0	O	These pins indicate the number of shifts towards the binary point which have occurred as the result of the conditional scaling logic. When the data path right shift is restricted to 2 places per pass, state 15 is used to indicate an overflow and only a total of 14 shifts is possible.
LFLG	O	This flag indicates that data is being loaded into the device. It goes active in response to an INEN input, and may be programmed to go in-active after the complete, one quarter, or one half a data block has been loaded.
$\overline{INEN}$	I	The use of this input is mode dependent. It is either used as an active low, load enabling, signal for the DIS strobe, or it is used to initiate a new block load operation.
DIS	I	The rising edge of this input is used to load data into the device.
DOS	I	The rising edge of this input is used to dump data from the device. In most applications it may be tied to the DIS input, even if the output rate must be higher than the input rate because of overlapped data blocks. The DIS input is then internally divided down.
$\overline{DAV}$	O	An active low signal that indicates that a transform is complete. Transformed data will then be output in normal sequential order using DOS. It may be optionally programmed to be delayed by 24 DOS strobes to match the delay through a PDSP16330.
$\overline{DEN}$	I	This input is used to enable the data dump operation when DAV has gone active. If it is tied low the device will automatically dump data when DAV goes active. Otherwise the device will wait for the enabling signal to go low before the dump operation commences.
DISAB	I	Only available in the 132 pin GC package. When high the block floating logic is disabled.
VDD	P	+5V pins
GND	P	Ground pins

NOTE. All references to DEF, INEN, DAV, and DEN within the text do not contain the bar designator, signifying an active low signal. This is considered to be implied by the signal name and is not meant to imply a change in the signal function.

FUNCTIONAL OPERATION

The PDSP16515A performs decimation in time, radix 4, forward or inverse Fast Fourier Transforms. Data is loaded into an internal workspace RAM in normal sequential order, processed, and then dumped in the correct order. With real only input data the processing time can approximately be halved for a given transform size. Two real inputs then replace a single complex input, and are processed in parallel.

Either a Blackman-Harris or a Hamming window can be

generated internally, and applied to the incoming real or complex data with no time penalty. No external ROM is needed to support these windows. The Blackman-Harris window gives improved dynamic range over the Hamming window when two closely spaced frequencies are to be detected, and one is of smaller magnitude than the other. It does, however, reduce the actual frequency resolution, and the Hamming window may then be preferable.

Data in and out of the device is represented by 16 bit real and imaginary components, with 16 bit sine and cosine values contained in an internal ROM. Conditional scaling, coupled with word growth through the butterfly data path, gives increased dynamic range. Transforms can be computed with sample sizes of either 256 or 1024 data points. The 256 point option can alternatively be used to simultaneously execute either four 64 point transforms, or sixteen 16 point transforms. The 16 point mode can only be used with a rectangular window, and no overlapping of data blocks is possible.

The device can be configured, either, to perform continuous transforms in a real time application, or as slave processor to a more general purpose signal processing system. In the continuous mode, with transform sizes of 256 points or less, it contains three internal control units which simultaneously allow new data to be loaded, present data to be transformed, and previous results to be dumped. Additional, external, input/output buffering is not needed. The internal input buffer also allows data blocks to be overlapped by either 50% or 75%, apart from the mode with no overlaps.

When 1024 point transforms are to be calculated, without loss of incoming data during the transform time, it is necessary to use an input buffer. This requirement is satisfied by a single PDSP16540 support device.

In any of the real or complex modes it is possible to obtain higher performance by connecting devices in parallel. It is then possible to increase the sampling rate to that of the system clock used for internal operations.

The mode of operation of the device is controlled by 16 bits in a control register. These are loaded through the AUX15:0 port when a control signal DEF is active low. This port is also used to provide the imaginary component of complex input data, and, if complex transforms are to be performed, an external tristate buffer will be needed to isolate the control information. This should only be enabled when DEF is active. DEF is also used to initialise the internal circuitry, and can be a simple power on reset if control parameters need not be subsequently changed.

DATA PRECISION

During each pass of a radix-4 fast Fourier transform it is possible for either component of a particular result to grow by a factor of up to four in the first pass, and 5.242 in subsequent passes. This is between two and three bits in each pass and the data path must allow for this word growth to avoid any possibility of overflow. At the end of the data path the word is preserved at 18 bits and stored in the internal RAM. Any unnecessary word growth to prevent overflow thus results in loss of arithmetic precision, and has a detrimental effect on the dynamic range achievable.

In practice these large word growths only occur when bipolar complex square waves are transformed, and even then will not occur on every pass. The PDSP16515A compromises by allowing a 2 bit word growth during the butterfly calculation in the first pass. This is equivalent to ignoring the most significant bit of the 19 bit final result, which is assumed to be an extra sign bit, and then selecting the next 18 bits for storage. In subsequent passes a Control Register Bit allows the user to continue to select these 18 bits, or instead to use the 18 most significant bits. The latter option is equivalent to a 3 bit word growth. The 2 or 3 bit word growth option applies to ALL subsequent passes and is not a per pass option.

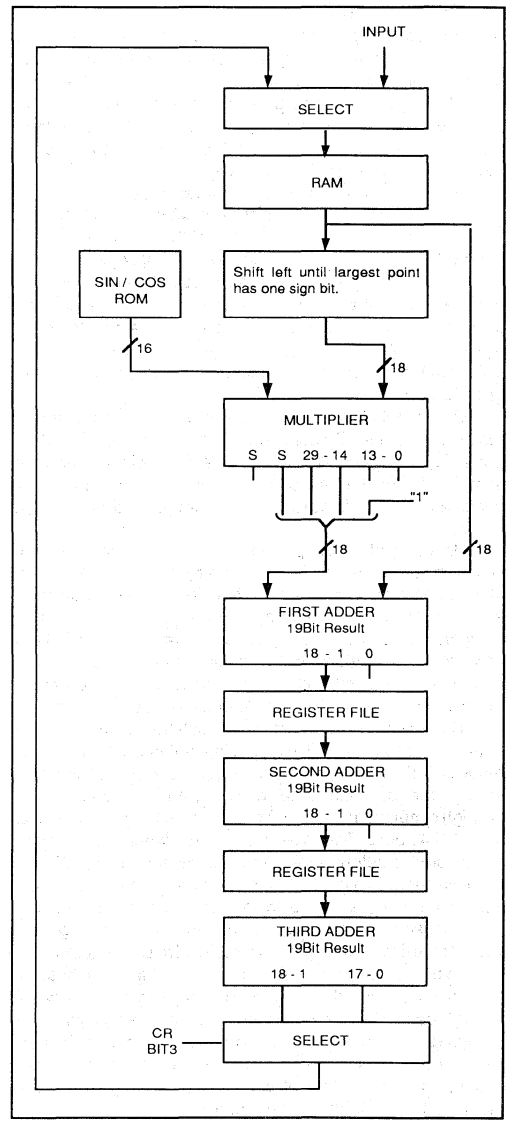


Fig. 3 One of Four Data Paths

If the 2 bit option is selected there is a possibility of overflow occurring in one of the passes. The prediction of overflow is mathematically difficult, and only occurs with specific complex square waves. Scaling down the inputs cannot be guaranteed to prevent overflow because of the block floating point shifting scheme, which is discussed later. Overflow can NEVER occur if the 3 bit option is chosen, but at the expense of worse dynamic range.

When overflow does occur a flag is raised which can be read by the user (see later discussion on scale tag bits), and the results ignored. In addition all frequency bins are forced to zero to prevent any erroneous system response.

Even with only 2 bit word growth poor dynamic range can result and becomes worse when the incoming data does not fully occupy all the bits in the word. These problems are overcome in the PDSP16515A, however, by a block floating point scheme which compensates for any unnecessary word growth.

During each pass the number of sign bits in the largest result is recorded. Before the next pass, data is shifted left [multiplied by 2], once for every extra sign bit in this recorded sample. At least one component in the block then fully occupies the 18 bit word, and maximum data accuracy is preserved

Up to four shifts are possible before every pass after the first, with a total of fifteen for the complete transform. At the end of the transform the number of left shifts that have occurred is indicated on S3:0. Lack of pins prevents a separate output being available to indicate that overflow has occurred in the 2 bit word growth option. For this reason the maximum number of compensating left shifts in this mode is restricted to 14. State 15 is then used to indicate that overflow has occurred.

The first step in the butterfly calculation multiplies 18 bit data values with 16 bit sine/cosine values, to give 18 bit results. This increased word length preserves accuracy through the following adder network, and has been shown through simulations to be an optimum size for transform sizes up to 1024 points. This is particularly true when the input data is restricted to below 16 bits, as is necessary with practical A/D converters with very high sampling rates. The bottom bit of this 18 bit word is forced to logical one and as such is a compromise between truncation and true rounding. It gives a lower noise floor in the outputs compared to simple truncation.

To prevent any possibility of overflow during the butterfly calculation the word length is allowed to grow by one bit through each of the three adders. The least significant bit is always discarded in the first two adders . Eighteen bits are then chosen from the final adder in the manner discussed earlier, and the number of sign bits in the largest result is recorded for use in the following pass.

Fig. 3 shows one of the four internal data paths which can compute a radix-4 butterfly in twelve system clock cycles. This equates to completing the butterfly in 3 cycles for the complete

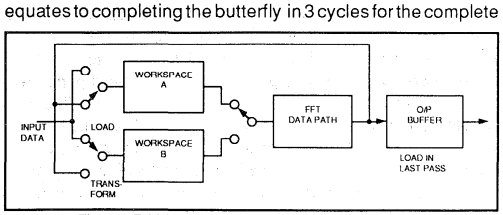


Fig. 4. RAM Organization with 256 Data Points

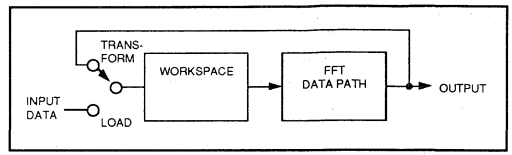


Fig. 5. RAM Organization with 1024 Point Transforms

device.

DATA TRANSFERS

The data transfer mechanism to and from the internal RAM has been designed for use in a wide variety of applications. The provision of an independent input strobe (DIS), allows data to be loaded without the need for additional external buffering. An independent output strobe (DOS) is also provided. DIS and DOS can thus be tied together, this being particularly useful when the device is performing the inverse transform back to the time domain. Transfer of data occurs internally from DIS to SCLK, so although thay can be of different frequencies, they must be synchronous to each other. In the same way transfer of data also occurs from SCLK to DOS, so while DOS can also be independent of SCLK it must also be synchronous to it. Inputs and outputs are both supported by flag and enabling signals which allow transfers to be properly co-ordinated with the internal transform operation.

In many applications the DIS and DOS inputs can be tied together and fed by the sampling clock. If the output rate must be higher than the input rate, as with multiple devices supporting overlapped data samples, both strobes can still be connected together. The clock supplied should then be twice or four times the sampling clock, and an internal divider can be used to provide the correctly reduced input rate. The provision of a separate DOS pin does, however, allow the output rate to be different to the input rate, and therefore faster than strictly needed. Further output processing at higher rates is then possible if this is advantageous to system requirements.

The internal workspace is double buffered when 256 point transforms are to be performed. A separate output buffer is also provided. These resources, together with separate input and output buses, allow new data to be loaded and old results to be dumped, whilst the present transform is being computed. Additional, external, input buffering is not needed to prevent loss of incoming data whilst a transform is being performed.

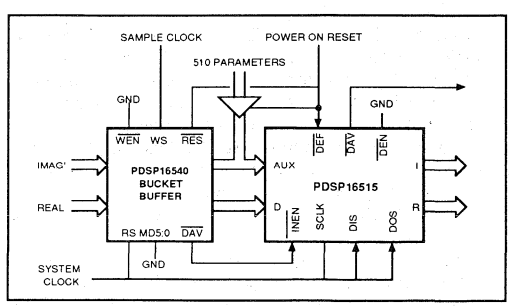


Fig. 6. 1024 Point Transforms with I/P Buffer

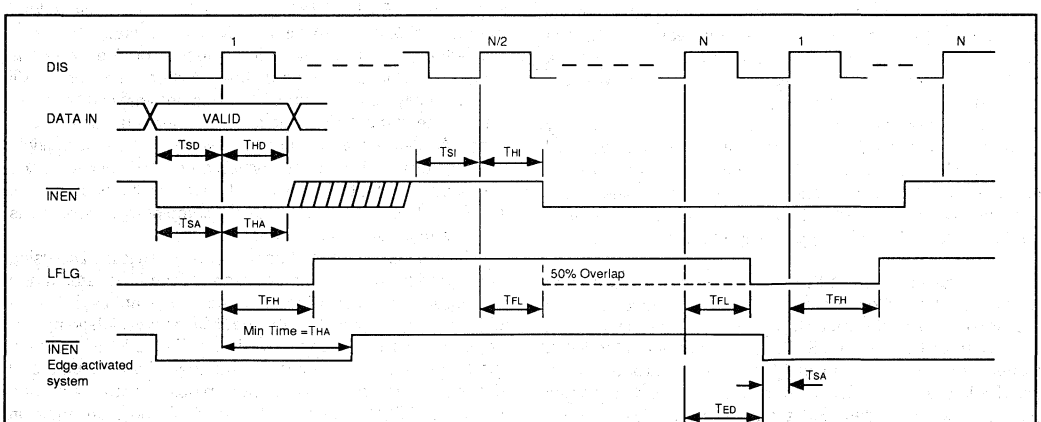
When block overlapping is required, internally stored data will be re-used, and a proportionally smaller number of new samples need be loaded. Note that the internal window operator still functions correctly since it is actually applied during the first pass, and not whilst data is being loaded. The internal RAM organisation is shown in Fig. 4. It should be noted that the amount of overlap between I/O transfers and transforms is completely under the control of the system, since an input enable signal (INEN) and an output enable (DEN) can be used to initiate transfers.

In the 1024 point mode there is insufficient workspace for input and output buffering in addition to working memory. The device is then configured in a mode with separate load, transform and dump operations. The internal arrangement is shown in Fig. 5. The support of an external input buffer is needed if incoming samples are not to be lost whilst a transform is in progress. This is loaded at the sample clock rate and transferred to the FFT processor as quickly as possible. In this mode the PDSP16515A always expects to receive 1024 words, regardless of the amount of block overlapping. Data stored internally cannot be re-used when block overlapping is required, and data from the external buffer must be re-read as necessary.

Fig. 6 illustrates a typical 1024 point system with an input buffer which supports complex input data. The input buffer can be provided by a PDSP16540 Bucket Buffer without the need for any external control logic. It supplies RAM for 1024 x 32 complex words, and allows transfers to the FFT Processor at the full system clock rate. The PDSP16540 also supports the standard 50% and 75% data block overlapping, but in addition allows the user to define the amount of overlap to within 32 words.

If no incoming data is to remain un-processed, the user must ensure that the time taken to acquire sufficient data to instigate a new transform is greater than or equal to the transformation time itself. The latter can be calculated from Table 4, once the system clock rate has been defined. When 1024 point transforms are performed, both the time to read data from the input buffer, and also the time to dump data, must be included in the calculation to determine the minimum time in which data can be loaded into the external buffer.

The peak transfer rate is limited by the characteristics of the I/O circuits, but can be greater than the sampling rate which is determined by the transform time. When load and dump operations are not concurrent with transform operations (as in the 1024 point modes), then the maximum I/O rate is equal to the system clock rate, Ø. When other transform sizes are specified, the sampling rate, S, is reduced by a factor F. This is defined below where Ø is in MHz and L is the system clock low time in nanoseconds :



Characteristic	Symbol	Min	Max		Units
Data In set up Time	T_{SD}	10			ns
Data In Hold Time	T_{HD}	0			ns
INEN active going set up	T_{SA}	8			ns
INEN active Hold Time	T_{HA}	0			ns
INEN in-active Hold Time to ensure no load	T_{HI}	2			ns
INEN in-active going set up for no load operation	T_{SI}	8			ns
Delay to LFLG going active (30 pf load)	T_{FH}		18		ns
Delay to LFLG going in-active (30 pf load)	T_{FL}		18		ns
Min time to INEN low in edge mode	T_{ED}	15			ns

Table 1. Advanced Timing Information with Continuous Inputs.

S = FØ, where F = 4 / (6+0.001ØL)

F is typically 0.66 and applies to all transforms except for those of 1024 points, even if INEN is driven such that concurrent operations do not actually occur (Note also that S must be synchronous to SCLK). If this causes a system limitation in a single device application, then the device can be configured for pseudo, Mode 2, multiple device operation. Separate load, transform, and then dump operations will then always occur, but DEN must be low when a transform is complete or DAV will never go active. See the section on multiple device operation.

LOADING DATA

Data loading is controlled by three signals; DIS an input strobe, INEN a load enable, and LFLG an output flag. Detailed timing information is given in Table 1. Once sufficient data has been acquired, a transform will automatically commence. This is normally after a complete block has been loaded, except when a single device is performing overlapped transforms of 256 points or less. With 75% overlapping, transforms will commence after 25% of a new block has been loaded, and with 50% overlapping transforms commence after 50% of the data has been loaded. The remainder of the block is provided by data already stored in the internal RAM.

The data strobe is used to load data into the internal workspace RAM, and data must meet the specified set up and hold times with respect to its rising edge. DIS can be a continuous input since the device only loads data when an input enabling signal is active.

An internal synchronisation interval is necessary between the last sample being loaded with the DIS strobe and transforms being started with the system clock. This can be up to twelve system clock periods when data transfers and transforms are overlapped. The transform times given later in Table 4 are maximum values, and include these twelve periods.

The way in which the INEN signal controls data loading is dependent on whether a single or multiple device is to be implemented, and the status of Control Register Bit 12.

When Bit12 is set in a SINGLE device system the INEN signal is simply used as an enable for the DIS strobes. When INEN is low, and provided the relevant set up and hold times have been satisfied, data will be loaded with the rising edge of the DIS strobe. If no gaps occur within the incoming data, INEN can be tied permanently low, provided that the sampling rate has been chosen such that transforms are completed before a new block of data is loaded. For transforms of less than 1024 points, data will then be continually processed without any loss of information. In the 1024 point modes the device will cease loading data when 1024 samples have been loaded, and even if INEN remains low no more data will be accepted until the previous results have been dumped.

In a multiple device system an edge is ALWAYS needed to commence a load operation, and Bit 12 has a different purpose. The edge is provided by INEN going low. Loading will cease when a complete block (or group of blocks with multiple concurrent transforms) of data has been loaded, even if INEN remains low. INEN must go high at some point after the minimum hold time has been satisfied, and then return low AFTER ALL DATA HAS BEEN LOADED, before a new load operation can commence. Low going edges which occur before all data has been loaded will be ignored.

The INEN edge mode is actually provided for the correct operation of multiple device systems, but if Bit 12 in the Control Register is reset in the SINGLE device mode, the edge activated operation will still be possible. With all but 256 point complex transforms, the single device edge mode of operation is identical to that of a multiple device system. With 256 point transforms, and their concurrent derivatives, the location of the low going edge in the data stream is dependent on the amount of block overlapping. The low going edge transition must be provided after 64 samples have been loaded with 75% overlapping, and after 128 samples have been loaded with 50% overlapping. With no overlapping the edge must be provided after 256 samples have been loaded.

In a single device system with Bit 12 set, INEN can be taken high to inhibit the load operation when gaps occur in the data stream. In the INEN edge activated mode gaps in the data stream can only be accommodated if the DIS clock is externally inhibited. Taking INEN high will not inhibit the loading of data in this mode.

With gaps in the data stream the peak sampling rates can be higher than continuous sampling rates. When data loading is not coincident with transform operations the peak rate can equal that of the system clock, otherwise it is reduced by the factor, F, given on the opposite page.

When Control Register Bit 12 is set in any multiple device mode, the DEF high going edge will also initiate a load operation after it has been internally synchronised to the rising DIS edge. If the first device in a multiple device system is programmed in this manner, the transform sequence will automatically start when DEF goes in-active. The other devices need the INEN edge as usual, and must have Bit 12 reset. A fuller explanation of the use of Bit 12 in a multiple device mode is given in the section on I/O In Multiple Device Systems. Note that the use of Bit 12 in a single device system (Control Register Bits 10:9 = 00) is completely different to its use in a multiple device mode.

The LFLG output goes active in response to the DIS rising edge used to load the first data sample, and indicates that a load operation is occurring. In an edge activated system the LFLG output will go high as the result of the first high going DIS edge after INEN has gone low. In the simple INEN enabling mode, internal logic counts the number of valid inputs and detects when the programmed block length has been reached. LFLG then goes low and will go high again in response to the next valid DIS strobe. LFLG will go low when DEF is active and will go high in response to the first INEN enabled DIS edge after DEF has gone in- active.

The active going LFLG edge does not normally have any system significance, but in the block overlapping modes the in-active going edge will occur when 50% or 75% of the data has been loaded. By driving the INEN input on one device with the LFLG output from a previous device, this edge can be used to partition data between several devices in a multiple device system. It can also be used to provide an address marker for a user defined input buffer, when executing 1024 point transforms with a single device. It is not needed, however, when the input buffer is provided by the PDSP16540.

DUMPING DATA

Data output is controlled by an output strobe [DOS], a dump enable signal [DEN], and a Data Available signal [DAV]. The DAV signal is used to indicate that the internal output

buffer contains transformed data, and the DEN input is used to control the outputting of that data. The output buffer within the device is clocked by the DOS input, and must be primed with a number of DOS strobes (see "user notes - stopping DOS") once a transform is complete in order to transfer data to the output pins. DAV will not go active until this priming has occurred.

The state of the DEN input at the end of a transform is used to control the transition of the active going edge of the DAV output with respect to the DOS strobes. The latter are then used to transfer data from the device to the next system component. If the DEN input is tied low in a single device system, the active going DAV transition will be internally synchronised to the rising edge of a DOS clock. If DEN is not tied low it must be guaranteed to be low at the end of the internal transform operation for this synchronization to occur. Since there is no external indication of this event, the user must take care to only allow DEN to go high whilst DAV is active, if this DAV synchronous mode is needed.

SYNCHRONIZED DAV OPERATION

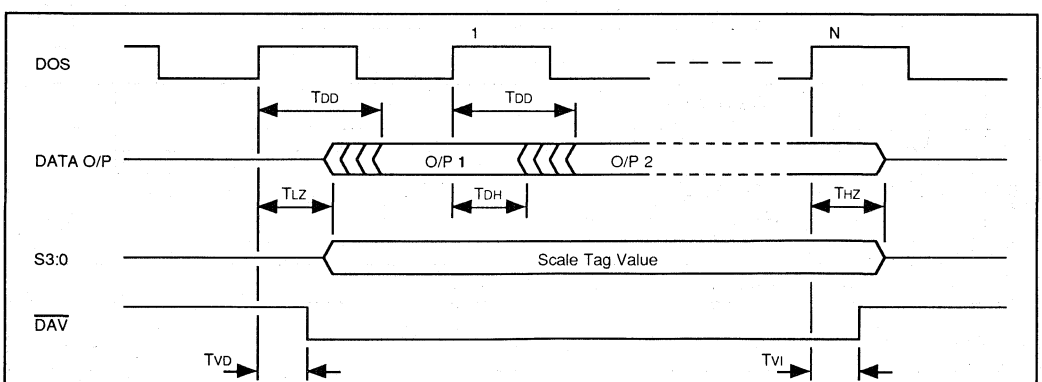
In the DAV synchronised mode the first rising edge of the DOS clock, after DAV has gone active, must be used to transfer the first transformed sample from the output pins to the next system component. It should be noted that the output buffer will have been primed before the active DAV transition, since DOS must be a continuous clock, and there is then no delay before the first output becomes valid. The DAV output can be used as a clock enable for this next device, and transfers will continue in normal sequential order until the required data has been dumped. DAV will then go inactive in response to the last DOS edge which was used to transfer data to the next device.

This mode of automatically dumping data when it is ready finds applications in real time data flow systems, and detailed timing is given in Table 2. It should be noted that the DOS input MUST be continually present before DAV goes active. If this is not the case the DAV output will not go active at the correct time, and the internal output circuitry will not be primed. Once DAV is active, however, it is possible for DOS to be irregular, and DEN can be used to inhibit the action of the output strobe as discussed previously. For the correct operation of the device the user must ensure that DOS becomes continuous and DEN remains low once DAV goes in-active.

When continuously transforming data such that new outputs are internally available before the previous block has been completely dumped, then DAV would normally stay active and give no indication that one block dump had been finished and another block started. Additional internal circuitry is, however, provided to ensure that DAV goes inactive for one DOS high time, thus supplying an inter block marker.

ASYNCHRONOUS DAV MODE

If DEN is not active in a single device when the transform is complete, then the device will wait for DEN to go active before any data is dumped. This mode is suitable for applications in which output processing is under the control of a remote host, such as a general purpose digital signal processor. The DAV output will then go active as soon as the output buffer is full, and will not be synchronised to the DOS edge. In such systems the DOS strobe may not necessarily be present at this time. Table 3 gives the relevant timing



Characteristic	Symbol	Min	Max		Units
Output Enable Time	T_{LZ}		18		ns
Output Disable Time	T_{HZ}		18		ns
Data Delay Time (30 pf load)	T_{DD}		18		ns
Data Hold Time	T_{DH}	2			ns
$\overline{DAV}$ active Delay Time (30 pf load)	T_{VD}	1	15		ns
$\overline{DAV}$ in active Delay Time (30 pf load)	T_{VI}	1	15		ns

Table 2. Output Timing with DEN tied low. (Advanced Data)

information.

In this host controlled dump mode the PDSP16515A waits for the host to activate the DEN input after DAV has gone active. DEN then functions as an enable for the host produced data strobes on the DOS pin. DEN may either stay active for the complete transfer, or may be used to enable each DOS input. When DEN and DOS are both active an internal read operation occurs, and an address generator is incremented. DAV goes in-active in response to the DOS edge needed to read the last output, unless Bit 15 in the Control Register is set. In this case DAV goes in-active when the next INEN edge is received for reasons given later.

In host controlled systems the time to dump data could be longer than the transform time. The dump time in such a system will dictate the maximum sampling rate that can be used without the loss of incoming data. In the 1024 point mode, when the loss of data is not important, the PDSP16515A is designed to not accept new data until the previous results have been dumped. Such a system needs no input buffer, and INEN can be permanently tied low if the edge activated mode is not in use. If the loss of data is to be avoided an input buffer is needed and the host must have received all the results before a new block of data has been loaded into the buffer.

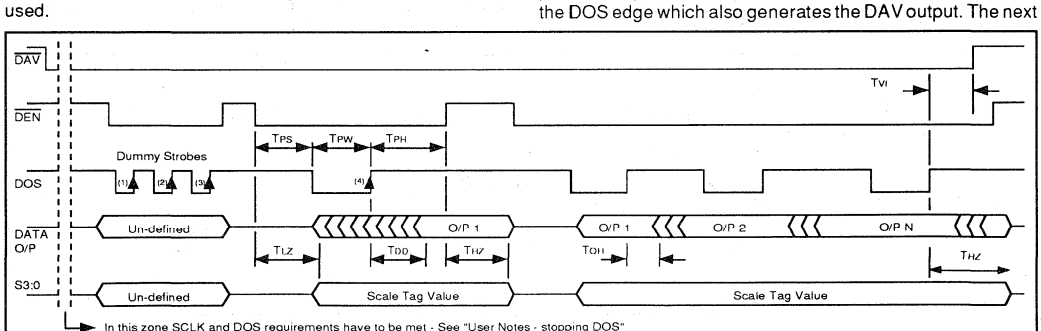
For 256 point transforms, with host controlled dumping, it is still possible to overlap load and dump operations. The maximum dump times, however, must be less than the load times to avoid data corruption. Previously converted outputs will be actually corrupted, rather than inputs simply not being used.

If the loss of incoming data is not important, the device can be forced to do separate load, transform, and then dump operations. The corruption of results will then never occur, no matter what dump time is taken. This can be achieved by ensuring that INEN is not active between loading a block of data and completing the dump of the results from that data. The same ends can be achieved if the INEN edge activated mode (Bit 12 reset) is used, and the inverted DAV edge is used to drive the INEN input. This then initializes a new load operation only when the previous dump has been completed.

Results are transferred from the device with the rising edge of the DOS strobe when DEN is active. This is consistent with using the device in a data flow architecture, as is commonly employed in data processing systems. In a typical microprocessor based system, however, data is normally expected to become valid before the end of the data strobe produced by the processor. It is thus necessary for the user to provide a 'dummy' data strobe in order to transfer data to the outputs which can then be read by the host during the next data strobe. In addition further ' dummy ' strobes are needed each time DAV goes active in order to prime the output circuitry. The actual output sequence is given in Table 3 for a single device systemand is described more fully in "user notes - stopping DOS".

GENERAL DUMP CONSIDERATIONS

The tri-state drivers on the output buses are only enabled when both DAV and DEN are active. When DEN is tied permanently low the output bus will start to become valid from the DOS edge which also generates the DAV output. The next



Characteristic	Symbol	Min	Max		Units
$\overline{DEN}$ Set Up Time	T_{PS}	10			ns
Host Strobe Width	T_{PW}	10			ns
$\overline{DEN}$ Hold Time	T_{PH}	5			ns
$\overline{DAV}$ in-active going Delay (30 pf load)	T_{VI}		15		ns
Output Enable Time (see Fig 13)	T_{LZ}		18		ns
Output Data Delay Time (30 pf load)	T_{DD}		18		ns
Output Disable Time (see Fig 13)	T_{HZ}		18		ns
Read Cycle Time	T_{RC}	25			ns
Old Data Hold Time	T_{OH}	2			ns

Table 3. Host Controlled Output Timing. (Advanced Data)

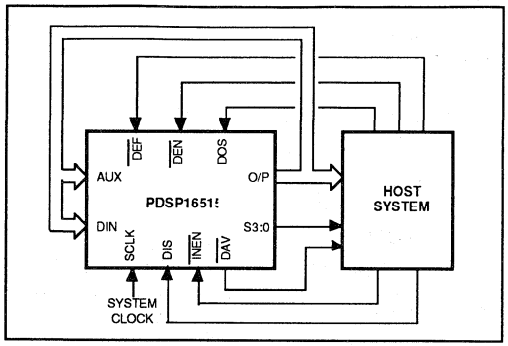


Fig. 7. Host Controlled System

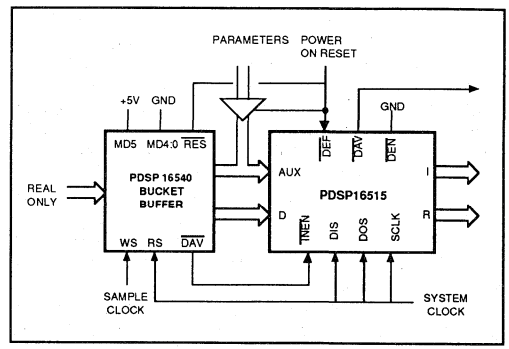


Figure 8. 1024 Point Real Transforms

DOS edge can then be used to transfer the first output to the next device. When DEN is driven low in response to the DAV output, the outputs start to become valid when DEN goes low. The Scale Tag outputs become valid at the same time as data, and when enabled will continue to indicate the correct value until all frequency bins have been dumped. If at any time during the dump operation DEN goes in- active, then both the data and scale tag outputs will go high impedance after the delay shown in Table 3.

Valid transformed data is actually available within the device from DAV going active until INEN again goes active, and a new set of data is loaded. The output tristate drivers, however, normally go high impedance when DAV goes in-active once a dump operation has been completed. In order to support systems in which it may be necessary to read the transformed data more than once, a Control Register Bit is provided which keeps the DAV output active until a further INEN edge is received. The user must then keep track of how many outputs have been dumped before INEN is generated to start a new load operation.

The DAV output can be delayed by an amount equivalent to the pipeline delay through the PDSP16330. This option is invoked by setting a control bit, and allows DAV to indicate that polar data is available at the output of the PDSP16330. When the option is used the tri-state outputs will be enabled when data is actually available and DEN is active, and not when DAV eventually goes active.

Two Control Register Bits allow a range of dump size options to be supported. In some applications the results of interest may only lie in the lower 25 or 50% of the frequency bins, the sampling rate having been chosen to prevent aliasing, and the transform size having been selected to give the required frequency resolution. In other systems it is only necessary to output the second half of a given sized transform. This is useful when filtering is to be performed in the frequency domain using Overlap /Discard Fast Convolutions. With this method FIR filters with N taps can be implemented in the frequency domain using 50% overlapped transforms on 2N samples. After multiplication in the frequency domain with the required frequency response, the inverse transform is performed and the first half of each output is discarded. Since only half the results are dumped, the dump clock need not be twice the rate of the clock used to load data.

FULL CO - PROCESSOR OPERATION

A single device can be configured as a co-processor to a host system in which both the loading and dumping of data is under the control of the host. Such a system is shown in Figure 7, in which DEN is a host provided enable for host read operations, and INEN is an enable for host write operations. DIS and DOS are host data strobes.

The host loads a block of data into the PDSP16515A, using DIS enabled by INEN, which is then automatically transformed. The DAV output provides a flag indicating that the transform is complete, and results are then read by the host using DOS enabled by DEN. A new set of inputs is not normally loaded until the previous results are complete. If, however, 1024 point transforms are not to be performed, loading new data could coincide with dumping previous results. This, however, would require a host system with separate input and output buses, and which also allowed coincident transfers. As discussed previously, transferring results must take no longer than loading new data to prevent corruption of the outputs.

In the system illustrated by Figure 7, the host also controls the mode of operation of the FFT processor. The DEF signal is produced from an address decode, and the control parameters are loaded from the host bus by connecting the AUX inputs to the data outputs.

REAL ONLY TRANSFORMS WITH A SINGLE DEVICE

In the simplest case real transforms can, of course, be computed by forcing zero levels on the imaginary input pins. The device can, however, be configured to internally perform two simultaneous real transforms instead of a single complex transform. The block floating point logic will then use data from both blocks when it determines the number of shifts to be applied. This dual transform technique is used to increase the maximum permissible sampling rates, but since an additional data pass is required in order to un-scramble the transformed data, the actual performance is not quite double that possible with a complex transform of the same size. The 4 x 64 point complex mode becomes an 8 x 64 real mode, but the change from 16 x 16 complex transforms to 32 x 16 real transforms is not supported.

When a real transform is performed the algorithm produces complex results for each of the incoming data

blocks, but each result only represents the first half of the frequency domain data. This does not cause any loss of information since the two halves are mirror images of each other. As with complex transforms, it is necessary for a different system configuration to be used when 1024 point transforms are required. These are considered later, and the following only applies to 256 or 64 point transforms.

In a single device system, performing non overlapped transforms on data from a SINGLE source, only the Real input pins are used, and the Imaginary inputs are redundant except when configuring the device. By setting Control Register Bits 8:6 to 101, however, it is possible for a single device to accept data from two independent sources using the real and imaginary inputs. Maximum sampling rates will then only be half those possible when a single source is used, if no incoming data is to remain un-processed. With two sources a transform must be completed in the time to load parallel blocks, otherwise incoming data will be lost. With one source a transform need not be finished until two data blocks have been acquired. In this dual input mode results from data on the real inputs always precede those from the imaginary inputs. If block overlapping is needed, it is always necessary to load pairs of data blocks simultaneously, using both the real and imaginary inputs. With dual sources of data this presents no problem, and Control Bits 8:6 should be set to 110 or 111 for the relevant amount of overlapping. If data is from a single source an external FIFO is needed to provide a simple delay for a block of data. Decodes 001 through 100 from Control Bits 8:6 must be used to select the required overlap.

The output of the FIFO must provide data for the real inputs. Continuous inputs can still be accepted, and each block will initially occur on the imaginary inputs, and then occur again on the real inputs as an output from the FIFO. The data output sequence will consist of the results from a pair of inputs, followed by the results obtained after the required overlap. Thus with 50% overlapping the sequence is 1 & 2 followed by 1.5 & 2.5 followed by 3 & 4 followed by 3.5 & 4.5 etc., where 1 2 3 4 are the sequential inputs to the external FIFO, 1.5 is the overlap between 1 & 2, and 2.5 is the overlap between 2 & 3.

When eight simultaneous 64 point transforms are performed, the sampling rates given in Table 5 assume that data is from a common source. The data outputs will be in the correct sequence from 1 to 8, corresponding to inputs 1 through 8 in normal order from a single source. When data is from two sources the sampling rates will be halved, and the output sequence will be 1A 1B 2A 2B 3A 3B 4A 4B, where A and B are the dual simultaneous sources on the real and imaginary inputs respectively. If data block overlapping is used in either of the above cases, the eight outputs will be followed by results from the same basic eight blocks but time displaced to give the required overlap. If more than two sources are to be handled the user must provide appropriate buffering and multiplexing, and the sampling rates must be proportionally reduced.

When two 1024 point transforms are performed with a single device, on data from a single source, the input buffer must be arranged to acquire two blocks before initialising a transfer to the device. In order to improve the maximum sampling rates possible, data should be read simultaneously from each half of the buffer, and loaded into the real and imaginary inputs. This halves the transfer time from the buffer to the device, but requires the device to expect dual inputs. Thus if block overlapping is not needed Control Register Bits 8:6 should be set to 101.

This fast transfer mode is supported by a special option on the PDSP16540 Bucket Buffer. It will acquire two 1024 point non overlapping blocks using the sampling clock, and then transfer the results to the FFT processor at the full system clock rate. Figure 8 shows the system arrangement. It does not support block overlapping.

With 1024 point transforms all block overlaps are handled by the buffer logic, and not by the internal RAM, but the device must still be programmed to expect the required overlap if the external buffer makes use of the in-active LFLG edge to mark the overlap point. To achieve the performance given in Table 5 with 50% overlaps, the buffer must provide sufficient storage for at least 2.5 data blocks. With 75% overlaps it must provide storage for 2.75 blocks. This extra storage allows transfers between devices to be only needed when a complete new block has been acquired for 50% overlaps, and when half a new block has been acquired for 75% overlaps. If storage is restricted to two data blocks, only half the sampling rates given will be possible. Transfers between devices must then occur when a half or a quarter of a new block has been acquired. Since the minimum time between transfers must be no less than the transform time itself, the sampling rates must be proportionally reduced to prevent loss of data.

Configuration		Clock Periods
16 X 16PT	COMP	456
4 X 64PT	COMP	660
256PT	COMP	852
1024PT	COMP	3943
8 X 64PT	REAL	852
2 X 256PT	REAL	1068
2 X 1024PT	REAL	4735

Table 4. Computation Times in Clock Periods

SINGLE DEVICE SAMPLING RATES

In a single device system the maximum sampling rate is dependent on the transform size, the data overlap, and whether real or complex data is applied. Table 4 gives the times taken to complete the transforms for the various block sizes, which include an allowance for synchronisation

16 X 16 COMPLEX			4 X 64 COMPLEX			256 COMPLEX			1024 COMPLEX			8 X 64 REAL			2 X 256 REAL			2 X 1024 REAL		
0%	50%	75%	0%	50%	75%	0%	50%	75%	0%	50%	75%	0%	50%	75%	0%	50%	75%	0%	50%	75%
23.9	-	-	16.1	8.0	4.0	12.3	6.1	3.0	6.8	3.4	1.7	24.6	12.3	6.1	19.5	9.7	4.3	12.1	6.0	3.0

Table 5 : Guide to MAX Sampling rates (in MHz) possible from a single device system.
SCLK is 40 MHz. Where sampling rate is asynchronous to SCLK, a pdsp16540 (or similar) is assumed on the input.

between the DIS strobe and the system clock. If continuous data is to be transformed, the time to acquire a new block of data (or partial block with overlapping) must be at least equal to these transform times. Load and dump times must also be added in the 1024 modes. For non continuous transforms the peak rate is limited by the system clock rate and the factor , F, given previously.

The time taken to dump the transformed data must be no more than the load time, if continuous inputs are to be supported and I/O operations are concurrent with transforms. With block overlapping the dump time must be reduced to the time taken to load the partial block. This dump time must include four extra DOS strobes needed to prime the output circuitry when a transform is complete. These, in effect, can be added to the transform time such that with concurrent I/O and 0%, 50%, or 75% overlapping;

nS or (nS)/2 or (nS)/4 must be gtr than or equal to PK + 4W

where n is the transform size, S is the input DIS period, P is the number of clock periods given in Table 4, K is the system clock period, and W is the DOS period which can be less than S if necessary. Note also that S must be synchronous to SCLK, and if an asynchronous ratio is required then a pdsp16540 input buffer should be used.

When DIS and DOS are produced from a common source the minimum allowable sampling period must be increased to allow for the extra dumping time. Thus when DIS and DOS have equal periods and, for example, there is no overlapping;

(n - 4)S must be greater than or equal to PK

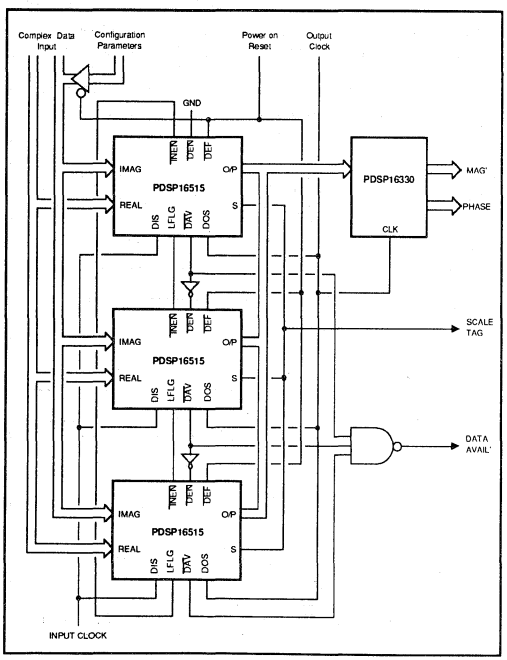


Figure 9. Multiple Device Configuration

The maximum sampling rates given in Table 5 allow for the extra dumping time.

The load and dump operations are not concurrent with transforms in the 1024 point modes, and an external input buffer will be needed if loss of incoming data is to be avoided. This is loaded at the sampling rate and then data is transferred to the PDSP16515A at a user defined rate. The time taken to load this external buffer must be at least equal to the sum of the time to transfer data in and out of the FFT processor and the transform time itself. When data blocks are overlapped by 50% or 75%, no more than one half or one quarter of the block, respectively, must have been loaded in the same time. In the 1024 point modes the dump time can be any user defined value, and need not be increased to allow for block overlapping. The dump time, however , does directly effect the maximum sampling rates which can be accommodated without loss of incoming data.

The maximum sampling rates for 1024 point transforms at any load and dump rate can be calculated from the following relationship:

1024S or 512S or 256S > 1024B + PK + D

for 0%, 50%, or 75% overlapping respectively. S, P, and K were defined opposite. B is the clock period in which data is read from the input buffer and loaded into the device, D is the total dump time allowing for the four extra DOS periods. The periods of the load and dump clocks cannot be less than the system clock period. The maximum sampling rates given in Table 5 assume that a 40 MHz I/O rate is used, and that all results are dumped.

MULTIPLE DEVICE SYSTEMS

In real time applications several devices may be used in parallel in order to increase the sampling rate, but not to increase the transform size. When all outputs are commoned together, and feed a single output processor, then the data dump time must always be less than or equal to the time taken to load the data block (or 50% or 25% of the time with block overlapping). In most configurations with block overlapping the dump rate requirements will limit the maximum input rate, if only one output processor is provided. This can be avoided if the system provides separate output processors for every device. The system clock used for internal calculations then ultimately imposes a limit on the maximum sampling rate possible.

A multiple device system performing complex transforms with a single output processor is shown in Figure 9. The INEN/ LFLG signals are used to co-ordinate the segmentation of data between devices. The in-active going edge of LFLG instigates the load procedure in the next device, and, since this edge can be programmed to occur either 25%, 50%, or 100% through the load operation, it can cause the next device to commence loading before the previous one has finished. In this manner data block overlapping is achieved. When multiple concurrent transforms are performed (for example 4 x 64 or 8 x 64) two LFLG transitions are sometimes needed to support block overlapping. This is fully explained in the section on Mode 1 sampling rates.

In any of the multiple device modes an INEN edge

transition is needed to start a new load procedure when the previous one has finished. When the LFLG output from the last device is fed back to the INEN input of the first device, continuous transforms will be executed. This continuous sequence can be started by the rising edge of DEF if Control Register Bit 12 is set in the first device (see section on Loading Data). This bit must not be set in the other devices. Since all devices are supplied from a common input bus and have a common source of control parameters, this Bit 12 inversion is best mechanized with an Exclusive OR gate in the AUX12 input line of the first device. The input can then be inverted when DEF is active but otherwise not be effected. Once the first device has been started with the DEF edge, the sequence will continue automatically using the LFLG /INEN connection between devices.

In many applications data is transformed continuously after power on, and the concept of a first data sample does not exist. If, however , the opposite is true, the first data sample must be present on the input pins such that it can be loaded with the second rising DIS edge after DEF has gone in-active. The data must meet the set up and hold times given in Table 1, and DEF itself must meet the parameters normally met by the INEN rising edge. The latter requirement is necessary to avoid a possible one DIS cycle variance, due the internal DEF synchronization logic. If the position of the first data sample is not important, it is not necessary for DEF to have any set up specification.

Without the feedback from the last device, the first device would wait for another externally supplied initialising pulse. In such a system with N devices in parallel, then N continuous transforms must be executed before the first device can wait for a new INEN input.

When only one output processor is provided the data outputs from all devices are connected together, and internal logic will enable the tri-state outputs when a device is ready to output data i.e. DAV goes active. When data blocks are overlapped it is possible that the output rate requirements will limit the input sampling rate (see section on Multiple Device Sampling Rates). Additional output processors will remove this restriction, and the correct choice of multiple device operating mode will optimise the sampling rates that can be achieved with a given number of devices.

The synchronisation intervals, necessary to co-ordinate input and output operations with the transform operation, lead, in effect, to some uncertainty in the time needed to complete a transform. Thus a particular device in a multiple device system can effectively complete a transform in less system clock periods than another device in the same system. To prevent one device turning on its output bus before the previous one has finished, it is either necessary to use a faster output rate than would otherwise be required, or to use the inverted DAV output from one device to drive the DEN input of the next. The latter option allows DIS and DOS to be connected together, and ensures that the second device will not output data until the first device has finished.

This method of driving the DEN input from the inverted DAV output from a previous device requires a change to the single device DAV and DEN operation. If DEN is active at the end of a transform in a multiple device system, the DAV output will go active when the output circuit has been primed by the DOS strobes. This operation is identical to that provided for a single device system, and is transparent to the user as long as DEN and DOS are active . If DEN is not active, however, the DAV output will not asynchronously go active as happens in a single device system. Instead DAV will only go active when DEN eventually goes active. Since DEN is the inverted DAV output from a previous device, it is thus never possible for two devices to be actively outputtng data. The DAV active going

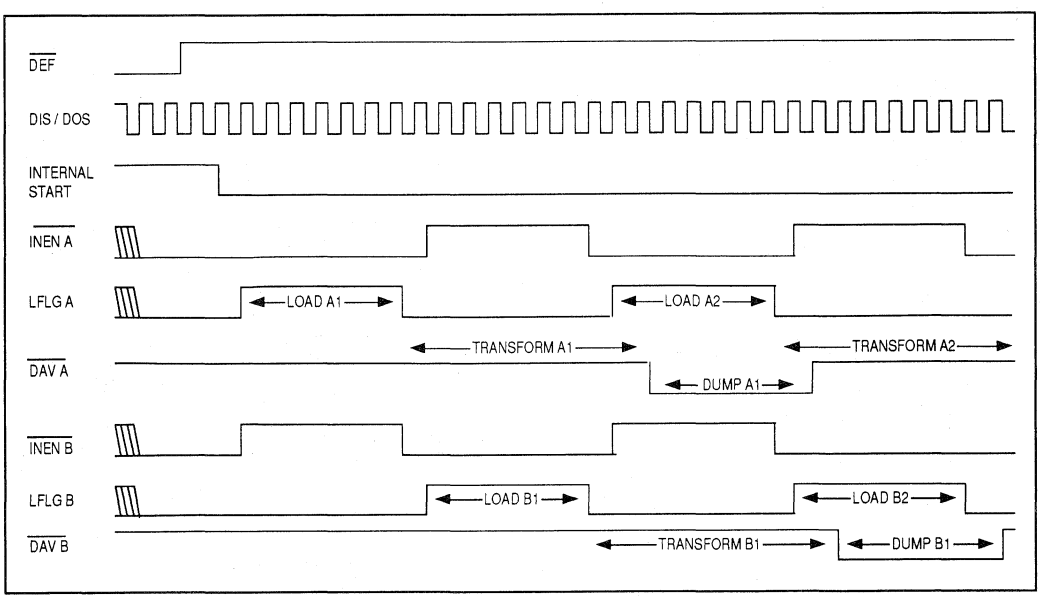


Figure 10. Three Device System with Separate Load, Transform, and Dump Operations

edge remains synchronised to the DOS strobe since the DEN input will only go active when a previous DAV goes in-active. A further change to the output circuitry ensures that the output buffer is primed even though DEN is not active. The first word, however, only progresses as far as the final output latch. The output bus is not enabled, and address increments do not occur, until DEN is finally received. This modification to the internal control logic ensures that the output buffer does not impose unnecessary gaps between consecutive transforms. These gaps would, in turn, force the required DOS frequency to be greater than the DIS frequency (or greater than twice or four times the frequency with 50% and 75% overlaps).

The system illustrated by Figure 9 produces a common DAV output by OR'ing together all the individual, active low, DAV outputs. This is not guaranteed to give an indication when one transform has finished, and the next one has started, since it may simply glitch as one DAV goes in-active and the next one goes active after some delay. This glitch will not cause system problems since it occurs at a point clear of the high going edge of the DOS strobe. To provide a marker for the end of a transform each in-active going DAV edge should set its own latch, which is then reset by a subsequent DOS edge. The output of the latches can then be OR'd together if necessary.

Three multiple device operating modes are actually provided, and are selected with Control Register Bits 10:9. The choice of a particular mode is application dependent, and will effect the maximum sampling rate achievable with a given number of devices.

MULTIPLE DEVICE SAMPLING RATES

MODE 1. (BITS 10:9 = 01)

In this mode transfers in and out of the device are concurrent with transform operations. This mode must not be used for 1024 point transforms due to internal memory size restrictions. When real transforms are performed in this mode, only the real data input is used, regardless of the amount of block overlapping.

The increase in performance is directly related to the number of devices provided, but the input and output rates are limited to FØ where F and Ø are as defined previously. Within this restriction the theoretical performance is given by;

$$NnS > PK+4W, \text{ or } 0.5NnS > PK+4W, \text{ or } 0.25NnS > PK+4W$$

for 0%, 50%, or 75% overlapping. N is the number of devices, n is the transform size, S is the DIS strobe period, P is the number of system clock periods given in Table 4, K is the system clock period, and W is the DOS strobe period. Note that DIS should be synchronous to SCLK, and also that DOS should be synchronous to SCLK.

If an output processor is provided for every device, two devices with 50% block overlapping or four devices with 75% block overlapping will give the same sampling rates as a single device with no overlapping. If only one output processor is provided, the two or four times increase needed in the output rate over the input rate, usually imposes a limit on the input rate, since the output rate is limited to a factor, F, of SCLK.

In this operating mode the DIS and DOS strobes can often be tied together, since a faster DOS strobe gives no improvement in the sampling rates possible. This remains true even when the output rate must be twice or four times the input rate due to block overlapping. Options can then be used which internally divide the DIS strobe by two or four, and thus allow the input to be driven by the faster DOS strobe.

In this mode the LFLG goes in-active after 25%, 50%, or 100% of the block has been loaded. When multiple transforms are performed concurrently (for example 4 x 64) a LFLG transition occurs at the relevant point whilst the first block in the group is being loaded. LFLG then goes high again and returns low at the overlap point in the last block. This double LFLG transition allows two devices to support 50% block overlapping, since the first transition from the first device can be used to initiate the load procedure in the second device. The second transition from the second device then initiates a new load procedure in the first device. The additional edges from each device have no effect since they occur when the device they are driving is already doing a load operation.

In such a two device system supporting 50% overlaps the inverted DAV from the first device must drive the DEN input of the second device. The data dumping time is then shared equally between both devices. The second device only outputs data when the first has finished, but both dumps must be finished in the time taken to load the group of blocks if only one output processor is provided. Without the DAV/DEN connection one device would only have had the time needed to load half of one sub block in which to dump its data.

In a similar manner four devices will handle 75% overlaps when concurrent multiple transforms are to be computed. The second, third, and fourth devices make use of the first transition, and ignore the second. The first device uses the second transition from the last device, and ignores the first. With the DAV/DEN connection each device will have one quarter of the load time to dump its data when a single output processor is provided .

More than two devices will provide increased performance for multiple transforms with 50% overlapping, and more than four devices will increase the performance with 75% overlapping. External logic is then needed to ensure that each device only uses the correct LFLG transition. Any device should only use the negative LFLG transition from a previous device if its own LFLG is low, and the LFLG output from the previous device plus one is low.

MODE 2 (BITS 10:9 = 10)

This mode is suitable for all transform sizes, since separate load, transform, and then dump operations occur. More devices than required by Mode 1 are necessary to achieve a given sampling rate, but the input and output rates can be any value up to the full system clock rate. As with Mode 1, additional output processors are needed to avoid the sampling rate restriction imposed by block overlapping.

The number of devices, N, needed to achieve a given sample rate can be derived from the following formula:

$$NnS > nS + PK + D \text{ for no overlapping}$$
$$NnS > 2 X [nS + PK + D] \text{ for 50\% overlapping}$$
$$NnS > 4 X [nS + PK + D] \text{ for 75\% overlapping}$$

N is the number of devices, n is the transform size, S is the DIS strobe period, P is the number of system clock periods given in Table 4, K is the system clock period, and D is the total dump time including 4 extra DOS periods as discussed previously. The DIS and DOS periods are any value defined by the user,

down to the system clock period. Note that DIS should be synchronous to SCLK, and also DOS should be synchronous to SCLK.

In this mode increasing the output clock frequency will allow a greater continuous input rate. The provision of separate DIS and DOS pins allows this to be mechanized, and the DOS frequency can be increased to that of the system clock used internally. When the sum of the dump time (including four extra DOS periods for output priming) plus 12 system clock periods (the transform time variation caused by input synchronization) is less than the load time, one device will be guaranteed to have finished dumping before the next one starts. The inverted DAV to DEN connection between devices is then not needed, and all DEN inputs can be grounded.

The LFLG transitions occur at the same times as Mode 1, except that the double transition does not occur with multiple concurrent transforms. Fig. 10 illustrates a timing sequence with three devices. Real transforms still only use the real inputs regardless of the amount of block overlapping.

MODE 3 (BITS 10:9 = 11)

Multiple device Mode 3 is provided in order to improve the performance when block overlapping is needed, and separate output processors are provided. In this mode transfers in and out of the device are never concurrent with transform operations. The device will actually load extra data such that the required data to perform two overlapped transforms is stored internally. The amount of internal RAM prohibits the use of this mode when performing overlapped 1024 point transforms.

LFLG will go in-active after a normal data block have been loaded, regardless of the overlap selected. The device, however, continues to load more data. Thus, for example, in the 4 x 64 mode, five 64 point blocks will be loaded. This technique allows each device in the system to complete two or four overlapped transforms (depending on the amount of overlap) before any new data is needed. When doing a straightforward 256 point transform the device will load 256 + 128 data points.

The full benefits are only obtained if more than one output processor is provided, but an extra processor is not always necessary for every device. Sampling rates up to the system clock rate are possible. The equations defining the sampling rates become:

$(N - 1)L > 2PK + 2D$ for 50% overlaps
$(N - 1)L > 4PK + 4D$ for 75% overlaps

where L is the time needed to load a normal block of data but not including the extra data, P is the number of system clock periods given in Table 4, K is the system clock period, and D is the total dump time including 4 extra DOS periods. As before, both DIS and DOS must be synchronous to SCLK.

When real transforms are to be performed on single sourced data, an external FIFO is needed to provide pairs of data blocks. These are loaded simultaneously into the real and imaginary inputs. See the section on real transforms.

OPERATING MODES

The operating mode of the PDSP16515A is determined by the condition of 16 bits in an internal Control Register. The status of these bits is defined by the inputs present on the AUX15:0 pins when the DEF input is active. The DEF input can be a simple power on reset if the operating mode is fixed once power is supplied. The AUX pins are also used to provide the imaginary component of the complex input data. Thus, if complex inputs are needed, the mode definition must be implemented through a tri-state buffer which is only enabled when DEF is active. The imaginary input data must be disabled during this time.

Table 6 lists the functionality of each of the bits in the mode control register, and further explanations are as follows:-

BITS 2:0

These bits define one of 7 options for the sample size and type of data. In the 1024 point options the device will assume the non concurrent operating mode, regardless of whether a single or multiple device system is specified. The internal control logic will then ensure that data is loaded, transformed, and dumped in sequential operations.

For other data set sizes, loading, transforming, and dumping, can all occur simultaneously with a single device; the actual overlap will be dependent on the relative occurrences of the INEN input. Only in Mode 1 can concurrent operations be done with multiple devices.

BIT 3

This bit determines the number of right shifts built into the data path. In either condition only two right shifts occur during the first pass. If the bit is reset, three shifts occur in subsequent passes and the block floating point scheme allows up to fifteen compensating left shifts. If it is set, two shifts occur in every pass and overflow is possible. This is indicated by reducing the number of compensating left shifts to fourteen, and using scale tag value fifteen to indicate that overflow has occurred.

BITS 5:4

These bits define the choice of window operator. If other windows are needed they must be applied externally. The fourth option is used to specify the inverse transform, which does not require the use of a window operator. When 16 x 16 complex transforms are specified by Bits 2:0, only the rectangular window can be used. The use of any of the other options will cause the device to enter an internal test mode.

BITS 8:6

These bits define 0%, 50%, or 75% data block overlapping, and the division factor on the DIS input. Overlapping must not be specified with 16 x 16 complex transforms.

Two decodes allow the DIS input to be divided by two or four, when 50% and 75% overlapping is respectively needed. These options allow the DOS and DIS input pins to be still supplied from a common source, even though the output rate must be faster than the input rate. The frequency of this source would be dictated by the output rate requirement, with the input rate internally reduced by the correct amount.

Special decodes are provided to support real only transforms from dual sources, using both the real and auxiliary inputs. When data is from a single source, and no overlaps are needed, only the real input should be used. If 50% or 75%

overlaps are needed from a single source of real data, the device always expects blocks to be simultaneously loaded. An external FIFO is then needed to supply data to the real inputs after a delay of one block. Each block is thus loaded twice, firstly through the Auxiliary inputs and then through the Real inputs.

BIT 10:9

These bits define a single device system, or one of three multiple device possibilities. The choice between the first and second multiple device mode is dependent on the transform size and the sampling rate needed. The third mode should only be used when overlapped multiple transforms with less than 1024 points are to be performed simultaneously. It changes the LFLG logic and allows sampling rates up to the system clock rate to be achieved with multiple output processors.

BITS	Dec'	OPTION
2:0	000	16 x 16 COMPLEX
	001	4 x 64 COMPLEX
	010	256 COMPLEX
	011	1024 COMPLEX
	100	8 X 64 REAL
	101	2 X 256 REAL
	110	2 X 1024 REAL
	111	NOT USED
3	0	SHIFT 3 PLACES AFTER PASS1
	1	ALWAYS SHIFT 2 PLACES
5:4	00	RECTANGULAR
	01	HAMMING WINDOW
	10	BLACKMAN-HARRIS
	11	INVERSE TRANSFORM
8:6	000	NO OVERLAP
	001	50% OVERLAP
	010	50% OVERLAP AND DIS ÷ 2
	011	75% OVERLAP
	100	75% OVERLAP AND DIS ÷ 4
	101	DUAL SOURCE, NO OVERLAP
	110	DUAL SOURCE, 50% OVERLAP
	111	DUAL SOURCE, 75% OVERLAP
10:9	00	SINGLE DEVICE
	01	N DEVICES, CONCURRENT I/O
	10	N DEVICES, LOAD-TRANS-DUMP
	11	SPECIAL MULTIPLE TRANSFORM
11	0	DAV NOT DELAYED
	1	24 CLK DAV DELAY
12	0	INEN EDGE ACTIVATED
	1	INEN IS SIMPLE ENABLE
14:13	00	O/P FIRST QUARTER
	01	O/P FIRST HALF
	10	O/P LAST HALF
	11	O/P ALL RESULTS
15	0	NORMAL DAV
	1	KEEP DAV ACTIVE TILL INEN

Table 6. Mode Control Bit Allocations

BIT 11

When this bit is set the PDSP16515A will not generate DAV until 24 DOS clocks after data was actually valid. In this case the output tri-state drivers will be enabled at the correct time, even though the DAV signal was not externally valid. Host controlled dumping should not be used.

BIT 12

When this bit is set in the single device mode, the INEN input is a simple load enable signal. When it is reset an INEN edge is needed at the end of a load sequence before a new one can commence.

When it is reset in a multiple device mode it has no action, but when it is set it will cause the DEF high going edge to also initiate a load operation.

BIT 14:13

These bits allow four dump size options to be provided. Individual frequency bins are not accessible.

BIT 15

Under normal circumstances DAV would be expected to go invalid when a transform has been dumped. In some applications, however, it may be necessary to read the outputs more than once. When this bit is set, DAV will remain valid until the next INEN input, and will indicate that the transformed data still remains in the internal buffer. As soon as the next INEN is received the transformed data will be overwritten. Whilst DAV remains active the output tri-states will be enabled.

WINDOW OPERATORS

Since only a finite segment of a signal can be observed and processed at any one time, it is impossible to obtain pure spectral lines. Discontinuities are introduced at the boundaries of the observation interval which lead to spectral leakage. Windows are weighting functions applied to the data in order to reduce these discontinuities at the boundaries.

In the time domain the signal has to be observed through a finite window as a matter of accord. This is in fact equivalent to multiplying the signal with a set of uniform weights i.e. a rectangular window operator. In the frequency domain the spectrum of the data will be the spectrum of this weighting function shifted to the sinusoidal frequencies of the components in the data.

The rectangular window has a Fourier Transform which is a SINC(X) function. This has sidelobes which are only 13dB down from the main lobe. This severely limits the dynamic range of the system since a second sinusoid in close proximity would have its main lobe swamped by this side lobe. This would occur if its amplitude was a mere 13dB down from the first sinusoid.

Window operators are thus mathematically constructed to cancel these sidelobes as far as possible. Unfortunately this is normally done at the expense of making the main lobe spread over more frequency bins. This reduces the ability of the system to resolve two frequencies, and can only be overcome by using more data samples. This may not always be possible because of other system constraints.

A common rule of thumb defines the resolution of an FFT

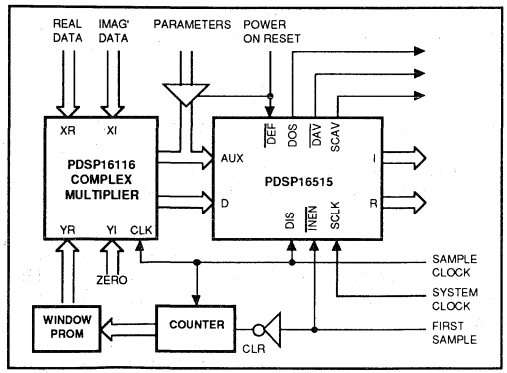


Fig. 11. External Window Generator

system as half the full width of the mainlobe. The width of the mainlobe for a rectangular window is two frequency bins; for the Hamming window it is four bins; for the Blackman-Harris window it is six bins.

The latter two windows are actually supported by the PDSP16515A. These are constructed on the fly as needed, and take the general form:

$A - B\cos x + C\cos 2x$ where $x = (2\pi n)/N$, $n = 0$ to $N-1$

For Hamming, $A = 0.54$, $B = 0.46$, $C = 0$

For Blackman-Harris, $A = 0.42323$, $B = 0.49755$, $C = 0.07922$

These windows can be applied to any of the transform size options, except the 16 x 16 complex variant. When the latter is specified the rectangular window option MUST be selected, or the device will be configured in an internal test mode.

If other operators are required these must be applied externally. This can be conveniently achieved with either a PDSP16112 or a PDSP16116, both of which are complex multipliers but with different accuracies. Fig. 11 shows how either one can be configured to perform two separate multiplications with one input common to both. This arrangement is necessary to perform the window function on complex inputs.

Important features of the windows generated by PDSP16515A, and other commonly used windows, are illustrated in Table 7. The results are obtained from the reference quoted, which should be consulted for a full mathematical treatment. The significance of each parameter is outlined below :

Highest Side Lobe Level

The inherent rectangular window has sidelobes which are only 13dB down from the mainlobe. These severely limit the dynamic range. The object of the window is to improve this situation with better side load attenuation.

Mid-Point Loss

In line with the filter concept it is possible to conceive of an additional processing loss for a tone of frequency mid-way between two bins. This is defined as the ratio of the coherent gains of two tones, one at the mid-point and one at the sample point. It is expressed in dB in Table 8.

Overall loss

An overall figure for the reduction in signal to noise ratio can be obtained by adding the mid-point loss to the reciprocal of the equivalent noise power bandwidth in dB. It is a measure of the ability of the window to detect single tones in broadband noise. The variance between windows is less than 1dB.

6.0dB Bandwidth

This figure, expressed in bin widths, represents the ability of the window to resolve two tones and should be as close to unity as possible. As the highest sidelobe level is reduced, this parameter tends to get worse, and a compromise must be used when choosing a window.

Overlap Correlation

In many practical systems the squared magnitudes of successive transforms are averaged to reduce the variance of the measurements. If, however, a windowed FFT is applied to non overlapping partitions of the sequence, data near the boundaries will be ignored since the window exhibits small

Window Operator	Highest Side Lobe	Mid-Point Loss dB	Overall Loss dB	6dB Bandwidth	Overlap Correlation	
					75%	50%
Rectangular	-13	3.92	3.92	1.21	75	50
Hamming	-43	1.78	3.1	1.81	70.7	23.5
Dolph-Chebyshev [C = 3.5]	-70	1.25	3.35	2.17	60.2	11.9
Kaiser-Bessel [C = 3]	-69	1.02	3.55	2.39	53.9	7.4
Blackman	-58	1.1	3.47	2.35	56.7	9
Blackman-Harris [3 term]	-67	1.13	3.45	1.81	57.2	9.6

Table 7. Window Performance (from The use of Windows for Harmonic Analysis. F J Harris. Proc IEEE Vol 66. Jan 1978)

Arithmetic Accuracy	Max Tone WRT Noise	Slot Noise Test	2 Tones with Freq Spread
16 bit,unconditional scaling	60	44	45
24 bit arithmetic with unconditional scaling, 16 bit inputs	88	67	65
16 bit inputs with PDSP16515A block FP	85	67	65
Full 32 bit Floating point with 16 bit inputs	93	82	67

Table 8. Comparative Dynamic Range Measurements

values at those points. To avoid this loss partitions are usually overlapped by 50% or 75%, which might, at first sight, remove the need to average successive transforms. If non-windowed transforms are overlapped by 75% or 50%, then 75% or 50% of the data will be correlated. When windows are applied, however, the data common to both transforms will be operated upon by different portions of the window waveform. The difference in these portions will dictate the amount of correlation between overlapped data. At 50% overlap Table 7 shows that with all windows the data is virtually independent, and successive averaging would still be needed. At 75% overlap figures are obtained which are closer to the 75% correlation obtained with no window.

Examination of Table 7 shows that the Blackman-Harris window gives performance very similar to that of the Kaiser-Bessel and Dolph-Chebyshev windows. The latter two windows can not be computed as they are needed since they are mathematically too complicated. The values are normally pre-computed and stored in a ROM; this would need to contain 1M bits to match the accuracy of the rest of the system.

Use of the Hamming window gives worse dynamic range than the more complex windows, but it has less effect on the overlap correlation and it has a smaller main lobe width.

SPECTRAL PERFORMANCE

There are two important parameters in the measurement of spectral response: resolution and dynamic range. Resolution defines how closely two sinusoids can be spaced in frequency and still be identified; dynamic range defines how great the difference in the amplitudes of the sinusoids may be and yet the smaller one still identified. Resolution is determined by the observation time [i.e. the width of the frequency bin] and the window operator that is used. Dynamic range is also determined by the window operator, but in a hardware implementation it is also influenced by the number of bits used to represent the data throughout the calculation.

The hardware effects include the accuracy of the A/D converter, the number of bits representing the window operator and the twiddle factors, and the way the growth in word length is handled as the FFT calculation proceeds. The obvious way to overcome these limitations is to use floating point arithmetic; but in real life the accuracy of the A/D converter is fixed and the sample size is limited. Floating point arithmetic is thus an overkill solution for the majority of applications. This is especially true for transform sizes up to 1024 points, which is the intended application area.

Figures given for the dynamic range of a system must be carefully interpreted, since there is no exact definition of the measurement. Three different ways of measuring dynamic range have been investigated using 1024 point transforms.

The 'best' dynamic range figures will be obtained with single tone measurements, and these results are often quoted to indicate the need for greater bit accuracies. The measure is the ratio of a full scale sinusoid to the average noise level and the results will be essentially independent of the window operator. The results given by the PDSP16515A are compared to various other configurations in the first column of Table 8. With this method the dynamic range is bound to improve as more bits are used to represent the data. Theoretically 6 dB of dynamic range will be obtained for every bit representing the input data, if the internal arithmetic accuracy gives no degradation in performance. In practice this improvement has no significance since the incoming waveforms will be much more complex than a single sinusoid.

An alternative method of determining dynamic range is with a slot noise test. White noise is passed through a narrow-band notch filter, several frequency bins wide, and the FFT computed. There is no noise in the filtered slot at the input to the FFT, but there is noise in the frequency bins corresponding to the width of the notch. Dynamic range is measured as the difference in dB of the average signal power and the average noise power and can be considered to give more useful results. Comparative results from various configurations are also given in the second column of Table 8. The performance with 24 bit data is seen to be little better than that obtained with the PDSP16515A. This can be attributed to the scaling scheme, word growth, and rounding method used within the device.

When two nearby tones are to be capable of detection, the window operator will dictate the performance of the system. The final column in Table 8 illustrates the results obtained using two sinusoids of different amplitudes, with the larger one residing mid-way between two frequency bins, and the smaller 5.5 bins away. The two frequencies are five bins apart to avoid the effects of the mainlobe widths. The dB figures given are the difference in amplitude between the two signals when the smaller one is still just detectable as a separate peak from the larger one.

This technique illustrates the performance of the window, since the amount by which sidelobe structure of the larger signal swamps the mainlobe of the smaller signal will determine if the smaller is detected. The theoretical attenuation of the highest sidelobe levels, with respect to the mainlobe, for the window options provided by the PDSP16515A have been given in Table 7, and represent the dynamic range that can be obtained if arithmetic effects are ignored. The results in the final column in Table 8 are the practical results given by the device, and as with the slot noise test indicate that the arithmetic scheme used by the PDSP16515A is equivalent to using 24 bit data. The Blackman Harris window was used in all cases.

USER NOTES - STOPPING DOS

GENERAL DESCRIPTION

The transform is calculated internally fully synchronous to SCLK. However, as all outputs are referenced to DOS, a transfer has to be made between the two clocks. In addition, some dummy DOS strobes are needed to operate the internal control logic, and to advance data from the internal RAMs to the output pins.

The most simple configuration for the device is to have DOS running continuously and for DEN to be permanently active. When this happens the user will just be aware of data appearing on the output pins on the same DOS cycle when DAV goes active. However, there are many situations where either DOS is not continuously running, or DEN is not permanently active. To help explain how to operate the device in these situations, the internal operation of the output circuits must be described. For those who are not going to be interrupting DOS, the remainder of this section can be ignored.

INTERNAL RAM - GENERAL DESCRIPTION.

For single device operation of transforms less than 1024 points, the internal RAM is shared between three separate operations which enable the device to output old transformed results, calculate the current transform, and input new data ready for the next transform. All these operations, along with the internal control logic, are controlled by a 12-cycle state machine. The RAM operations are :

(a) 2 cycles in every 12 are dedicated to reading new information in the input buffer and writing it to the RAM.

(b) 2 cycles in every 12 are dedicated to reading the contents of the RAM and advancing that data to the output buffer.

(c) 8 cycles in every 12 are dedicated to the read and write operations of the transform currently being calculated.

SEQUENCE OF EVENTS

The sequence of events relating to the output control and data flow is as follows :

(3.1) An SCLK rising edge :

(a) An internal flag is raised to indicate that the transform has finished and data is available to be dunped. Data will be present in the internal RAM, and the output address generator will be at the cortrect address. Access to the RAM at this moment, however, has not been made.

(b) If at this moment the device is programmed to be a single device, and DEN is inactive, then DAV will be made active - ie without the presence of DOS. If DEN is active at this point, or the device is programmed in any multiple device mode, then DAV will remain inactive.

(3.2) Accessing the RAM at this point

At this moment, when DAV has been made active before data appears on the output pins, data is not yet in the output buffer. Internally the precise SCLK cycle at which the RAMs are read and written to the output buffers now has to be waited for. This cycle, as described above ocurrs 2 in every 12 SCLK cycles, so at worst case 6 SCLK cycles have to elapse until data is guaranteed to be in the output buffer.

If the DOS rate is similar to the SCLK rate, and the user has been immediately applying DOS pulses (on seeing DAV go active) hoping to get data off the chip, then this will not actually happen.

The next internal flag raised is the one which indicates that the output data has been successfully read from the RAMs and is now in the output buffer.

(3.3) The next DOS rising edge (regardless of DEN status) :

The flag indicating that the RAMs have been read is transferred to circuitry operating on DOS. The output enable signal, DEN, does not have to be present at this point.

(3.4) The next DEN-Enabled DOS rising edge (ie the 1st one of this sequence)

The output state machine receives it's first edge.

(3.5) The next DEN-Enabled DSO rising edge (ie the 2nd)

Internal output address generators start to count (ready for fetching the next set of output data).

(3.6) The next DEN-Enabled DOS rising edge (ie the 3rd)

An enable signal is raised for the final data latch in the output buffer.

(3.7) The next DEN-Enabled DOS rising edge (ie the 4th)

(a) The final data in the output buffer latch clocks-through new data and presents it to the output pads.

(b) The output pads come oput of high impedance.

(c) If DAV was previously inactive, it is now made active.

OUTPUT SCENARIOS

Considering the above sequence, therefore, some single device situations can now be explained :

(4.1) DOS is continuously present, but DEN is inactive (Transform size less than 1024)

In this case, when the transform is complete, as the device is programmed as a single device and DEN is inactive, DAV will be made active. Even though DOS is running, the status of DAV at this point does not rely on it.

The user can now monitor the status of DAV, and after at least 6 SCLK cycles can initiate some further action, eg by external control force DEN active at some later time when the rest of the system is ready to accept the transformed data. Independently of this external control, the next DOS pulse will start to operate the sequence of events as described above (ie point No. 3.3). When DEN is eventually made active, the remainder of the above sequence (points Nos 3.4 to 3.7) is executed, with 4 DEN-Enabled DOS pulses needed before data is observed on the output pins.

If however the user immediately forces DEN active upon monitoring DAV go active and waiting for the required 6 SCLK cycles, then 5 DOS pulses would have to be issued. The first of these 5 would start the sequence of events as described above (3.3), and the fact that it is enabled by DEN would be irrelevant. The required DEN enabled pulses in this situation would be the 2nd, 3rd, 4th and 5th pulses supplied.

(4.2) DOS is not running, and DEN is inactive. (Transform sizes less than 1024)

In this situation, again as the device is programmed to be a single device and DEN is inactive at the point where the transform is complete, DAV will be made active regardless of the state of DOS. The user can now monitor this event on DAV and after waiting a further 6 SCLK cycles, use it to switch on DOS and to make DEN active.

DOS can now be switched on for at least one pulse (but may be more), and the sequence of events as described earlier (from point No 3.3) will start. DEN can then be made active, whereby a further 4 DEN-Enabled DOS pulses will be required before data is seen on the output pins. This is the situation shown in table 3.

Alternatively, DEN and DOS could be made to operate on the same cycle. In this case data will appear on the output pins on the 5th DOS pulse (the first would not actually require the presence of DEN, but the 2nd, 3rd, 4th and 5th would)

(4.3) 1024 point transforms, single device mode.

In the case of 1024 point transforms, the internal RAM is no longer operated in the manner described in section 2. The RAM is instead totally dedicated to one operation at a time. Thus data for a transform will be loaded, and all 12 out of 12 SCLK cycles will be available for the transfer of input data to the RAMs. During the transfrom no transfers from the input to the RAM or from the RAM to the output are possible. This is why DIS and DOS can be equal to SCLK for 1024 point transforms.

If 1024 point transforms are being performed and the device is programmed as a single device, then "asynchronous" operation of DAV is possible as described earlier for transform sizes less than 1024 points. If DEN is inactive at the time the transform has finished calculating, then DAV will be made to go active regardless of the state of DOS. Although 6 SCLK cycles do not have to be waited for as in section 3.2, a transition has to be made from the transform controlling the internal RAM to the output circuits cntrolling it. This operation plus the time taken to advance data from the RAMs to the output buffer takes exactly 4 SCLK cycles.

Hence the sequence of events is exactly as described in section 3, except that section 3.3 should read 4 SCLK cycles rather than 6. The analysis of sections 4.1 nad 4.2 are also true if the 6 SCLK cycle time is substituted with 4 SCLK cycles.

DUMMY DOS STROBES AFTER DEF

In addition to the dummy DOS strobes needed prior to dumping data, it is necessary to provide at least 4 DOS strobes after DEF has gone inactive, but before DAV goes active. These initialise the internal address counters and do not rely on DEN also being active. They are needed every time DEF has been used to change the operating mode.

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage Vcc	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to Vcc + 0.5V
Output voltage V_{OUT}	-0.5V to Vcc + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HMB)	500V
Storage temperature T_S	-65°C to 150°C
Junction Temperature, Commercial	100°C
Junction temperature, Industrial	115°C
Junction Temperature, Military	155°C
Package power dissipation	5000mW

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as positive into the device.

Test	Waveform - measurement
Delay from output high to output high impedance	V_H 0.5V
Delay from output low to output high impedance	V_L 0.5V
Delay from output high impedance to output low	1.5V 0.5V
Delay from output high impedance to output high	1.5V 0.5V

V_H - Voltage reached when output driven high
V_L - Voltage reached when output driven low

ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise state)

PDSP16515A C0 Tamb = 0 C to + 70°C. Vcc = 5.0v ± 5%
PDSP16515A B0 Tamb = -40 C to + 85°C. Vcc = 5.0v ± 10%
PDSP16515A A0 Tamb = -55 C to +125°C. Vcc = 5.0v ± 10%

Characteristic	Symbol	Value			Units	Notes
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.0		-	V	SCLK, DIS, DOS, DEN need 3V
Input low voltage	V_{IL}	-		0.8	V	DEN needs 0.7V max
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{CC}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{CC}
Output S/C current	I_{SC}	10		300	mA	V_{CC} = Max

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Max	Conditions
Clock Frequency (MHz)	Ø	DC	50	Max Ø high time is 1msec
Clock High Period (ns)	T_{CH}	8		
Clock Low Period (ns)	T_{CL}	8		
Max DOS, DIS Frequency	$Ø_D$		FØ	Less than 1024 points or Mult Dev Mode 1 Note $F = \frac{4}{6 + 0.001ØT_{CL}}$
Max DIS Frequency	$Ø_D$		40	1024 points or Mult Dev Modes 2 and 3
Max DOS Frequency	$Ø_D$		40	D15, DOS must be derived from Ø

SCLK to DIS/DOS RELATIONSHIP

Both DIS and DOS must be synchronous to SCLK. Ideally they should both be produced from SCLK, in which case the SCLK rising edge would either be first or coincident with the DIS and DOS rising edges.

In any event, the rising edge of SCLK must not fall between 2ns and 10ns after the rising edge of either DIS or DOS

ORDERING INFORMATION

PDSP16515A C0 AC	(Commercial - PGA Package)
PDSP16515A C0 GC	(Commercial - Leaded Chip Carrier)
PDSP16515A B0 AC	(Industrial - PGA Package)
PDSP16515A B0 GC	(Industrial - Leaded Chip Carrier)
PDSP16515A A0 AC	(Military - PGA Package)
PDSP16515A A0 GC	(Military - Leaded Chip Carrier)
PDSP16515A/MA/GCPR	(Military - Screened Leaded Chip Carrier. See separate datasheet for details)

VP16256

PROGRAMMABLE FIR FILTER

The VP16256 contains sixteen multiplier - accumulators, which can be multi cycled to provide from 16 to 128 stages of digital filtering. It accepts 16 bit data and coefficients, and accumulates results upto 32 bits.

In 16 tap mode the device samples data at the 25MHz system clock rate. If a lower sample rate is acceptable then the number of stages can be increased in powers of two upto a maximum of 128. Each time the number of stages is doubled, the sample clock rate must be halved with respect to the system clock. With 128 stages the sample clock is therefore one eighth of the system clock.

In all speed modes devices can be cascaded to provide filters of any length, only limited by the possibility of accumulator overflow. The 32 bit results are passed between cascaded devices without any intermediate scaling and subsequent loss of precision.

The device can be configured as either, one long filter, or two separate filters with half the number of taps in each. Both networks can have independent inputs and outputs.

Both single and cascaded devices can be operated in decimate by two mode. The output rate is then half the input rate, but twice the number of stages are possible at a given sample rate. A single device with a 20MHz clock would then, for example, provide a 128 stage low pass filter, with a 5MHz input rate and 2.5MHz output rate.

Coefficients are stored internally and can be down loaded from a host system or an EPROM. The latter requires no additional support, and is used in stand alone applications. A full set of coefficients is then automatically loaded at power on, or at the request of the system. A single EPROM can be used to provide coefficients for upto 16 devices.

FEATURES

- Sixteen MACs in a single device
- Basic mode is 16 tap filter with 25MHz sample rates
- 16 bit data and 32 bit accumulators
- Programmable to give up to 128 taps with sampling rates proportionally reducing to 3.13MHz
- Can be configured as one long filter or two half length filters
- Decimate by two option will double the filter length
- Coefficients supplied from a host system or a local EPROM
- 208 pin plastic power QFP package

APPLICATIONS

- High Performance Digital Filters
- Pulse Compression for Radar & Sonar
- Matrix Multiplication
- Correlation

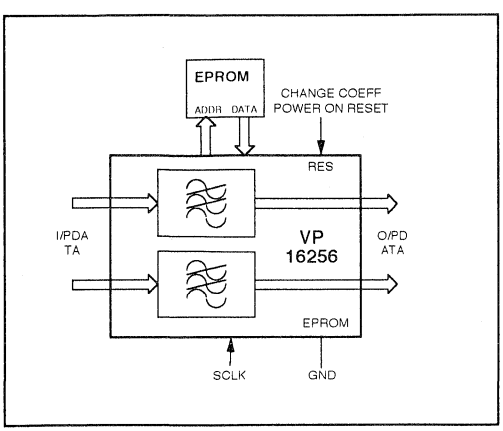


Fig. 1 Dual Filter

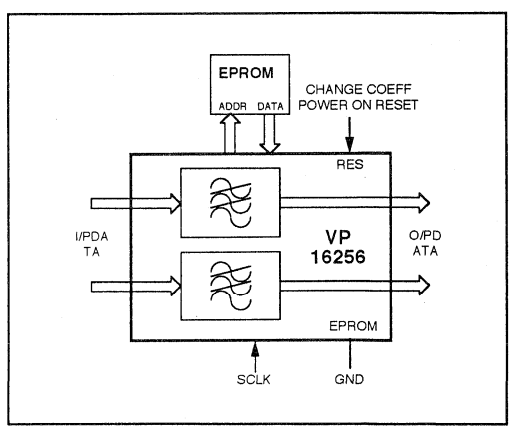


Fig. 2 Typical System Application

SIGNAL	DESCRIPTION
DA15:0	16 bit data input bus to Network A.
DB15:0	Delayed data output bus in the single filter mode. Connected to the data input bus of the next device in a cascaded chain. Input to Network B in the dual filter modes.
X31:0	Expansion input bus in the single filter mode. Connected to the previous filter output in a cascaded chain. The inputs are not used on a single device system or on the Termination device in a cascaded chain. The output from Network B in the dual modes.
F31:0	In single filter mode this bus holds the main device output. In dual mode it holds the output from Network A.
FEN	Filter enable. The first high present on an SCLK rising edge defines the first data sample. The signal must stay active whilst valid data is being received.
DFEN	Delayed filter enable. This output is connected to the Filter Enable input of the next device in a cascaded chain, when moving towards the termination device. It is used to coordinate the control logic within each device.
SWAP	Selects either the upper or lower set of coefficients for Bank Swap. A low selects the lower bank, a high the upper bank.
FRUN	When high this signal allows continuous filter operations to occur without the need for the initial FEN edge. If the device is not a single or interface device then this pin must be tied low.
$\overline{\text{DCLR}}$	A low on this signal on the SCLK rising edge will clear all the internal accumulators. DCLR need only remain low for a single cycle, signal BUSY will indicate when the internal clearing is complete. After a clear the device must be re-synchronised to the data stream using FEN. It is recommended the FEN is taken low at the same time as clear. FEN may then be taken high to synchronise the data stream once BUSY has returned low.
C15:0	16 bit coefficient input bus. In the Byte mode of operation, C15:8 have alternative uses as explained in the text.
A7:0	Coefficient address bus. In the EPROM mode A7:0 are address outputs for an EPROM. In the remote host mode they are inputs from the host. A7 is not used when coefficients are loaded as 16 bit words.
CCS	This pin is similar in operation to A7:0 and provides a higher order address bit. When low the coefficients are loaded, when high the control register is loaded.
$\overline{\text{WEN}}$	In the remote mode this pin is an input which when low enables the load operation. In the EPROM mode it is an output which provides the write enable for other slave devices.
$\overline{\text{CS}}$	This pin is always an input and must also be low for the internal write operation to occur.
$\overline{\text{BYTE}}$	When this pin is tied low, coefficients are loaded as two bytes. When the pin is high they are loaded as 16 bit words. In the EPROM mode this pin is ignored.
$\overline{\text{EPROM}}$	When this pin is tied low coefficients are loaded as bytes from an external EPROM. The device outputs an address on A7:0. When the pin is high coefficients must be loaded from a remote master. They can then be transferred individually rather than as a complete set.
SCLK	The main system clock, all operations are synchronous with this clock. The clock rate must be either 1, 2, 4, or 8 times the required data sampling rate. The factor used depends on the required filter length.
CLKOP	This output when used to enable SCLK can provide a data sampling clock. It has the effect of dividing the SCLK rate by 1, 2, 4 or 8 depending on the filter mode selected.
$\overline{\text{OEN}}$	Tri-state enable for the F bus. When high the outputs will be high impedance. OEN is registered onto the device and does not therefore take effect until the first SCLK rising edge

SIGNAL	DESCRIPTION
BUSY	A high on this signal indicates that the device is completing internal operations and is not yet able to accept new data. The signal is used during automatic EPROM loading, reset and accumulator clearing.
$\overline{RES}$	When this pin is low the control logic and accumulators are reset. In the EPROM mode it will initiate a load sequence when it goes high.

NOTE unused busses (e.g. X31:0 when the device is configured in single or termination mode) can be set to any value. They should however be maintained at a valid logic level to avoid an increase in power consumption.

To ensure correct input voltage thresholds are maintained all the VDD and GND pins must be connected to adequate power and ground planes.

Pad	Sig	Pad	Sig	Pad	Sig	Pad	Sig	Pad	Sig
1	VDD	43	F28	85	GND	127	A5	169	GND
2	F0	44	F29	86	C2	128	A6	170	X7
3	F1	45	GND	87	VDD	129	GND	171	X8
4	GND	46	F30	88	C3	130	A7	172	VDD
5	F2	47	F31	89	C4	131	DB0	173	X9
6	F3	48	VDD	90	C5	132	VDD	174	GND
7	VDD	49	FEN	91	C6	133	DB1	175	X10
8	F4	50	DFEN	92	VDD	134	GND	176	X11
9	F5	51	DCLR	93	C7	135	DB2	177	X12
10	GND	52	GND	94	GND	136	DB3	178	VDD
11	F6	53	SWAP	95	C8	137	DB4	179	X13
12	F7	54	GND	96	C9	138	VDD	180	X14
13	VDD	55	OEN	97	C10	139	DB5	181	GND
14	F8	56	CLKOP	98	GND	140	GND	182	X15
15	GND	57	VDD	99	C11	141	DB6	183	X16
16	F9	58	DA0	100	C12	142	DB7	184	X17
17	F10	59	VDD	101	C13	143	VDD	185	VDD
18	VDD	60	DA1	102	VDD	144	DB8	186	X18
19	F11	61	GND	103	C14	145	VDD	187	GND
20	F12	62	DA2	104	VDD	146	DB9	188	X19
21	GND	63	VDD	105	C15	147	DB10	189	X20
22	F13	64	DA3	106	GND	148	GND	190	X21
23	F14	65	DA4	107	GND*	149	DB11	191	VDD
24	F15	66	VDD	108	WEN	150	DB12	192	X22
25	VDD	67	DA5	109	CCS	151	VDD	193	GND
26	F16	68	GND	110	CS	152	DB13	194	X23
27	F17	69	DA6	111	VDD	153	DB14	195	X24
28	GND	70	DA7	112	RES	154	GND	196	X25
29	F18	71	DA8	113	GND	155	DB15	197	X26
30	F19	72	DA9	114	SCLK	156	VDD	198	GND
31	VDD	73	VDD	115	GND	157	GND	199	X27
32	F20	74	DA10	116	VDD	158	BUSY	200	VDD
33	F21	75	GND	117	BYTE	159	X0	201	X28
34	F22	76	DA11	118	EPROM	160	VDD	202	X29
35	F23	77	DA12	119	A0	161	X1	203	X30
36	VDD	78	DA13	120	VDD	162	GND	204	GND
37	F24	79	DA14	121	A1	163	X2	205	X31
38	F25	80	VDD	122	GND	164	VDD	206	VDD
39	GND	81	DA15	123	A2	165	X3	207	FRUN
40	F26	82	GND	124	A3	166	X4	208	GND
41	VDD	83	C0	125	A4	167	X5		
42	F27	84	C1	126	VDD	168	X6		

Fig. 3 Device Pinout (208 pin PQUAD - GH208)

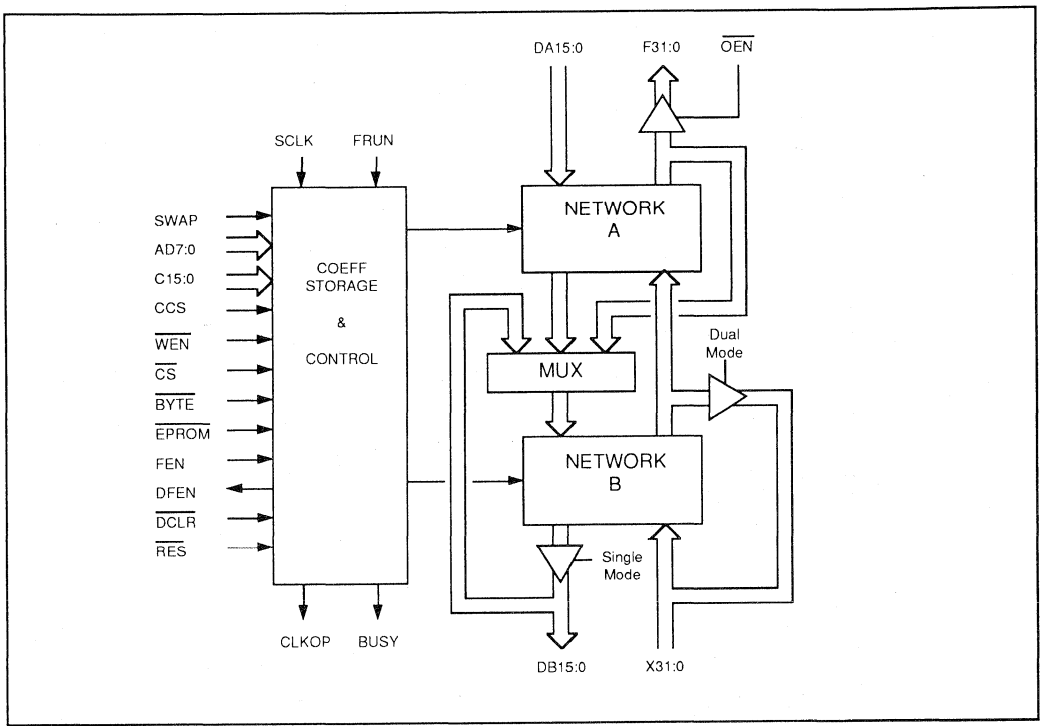


Fig. 4 Block Diagram

OPERATIONAL OVERVIEW

The VP16256 is an application specific FIR filter for use in high performance digital signal processing systems. Sampling rates can be upto 25MHz The device provides the filter function without any software development, and the options are simply selected by loading a control register. The device can be user configured as either a single filter, or as two separate filters. The latter can provide two independent filters for the in-phase and quadrature channels after IQ splitting, or can provide two filters in cascade for greater stop band rejection.

The device operates from a system clock, with rates up to 25MHz. This clock must be 1, 2, 4, or 8 times the required sampling frequency, with the higher multiplication rates producing longer filter networks at the expense of lower sampling rates. Devices can be connected in cascade to produce longer filter lengths. This can be accomplished without the need for any additional external data delays, and all the single device options remain available.

Continuous inputs are accepted, and continuous results produced after the internal pipeline delay. Connection can be made directly to an A/D converter. The filter operation can be synchronised to a Filter Enable signal whose active going edge marks the first data sample. The internal multiplier - accumulator array can be cleared with a dedicated input. This is necessary if erroneous results obtained during the normal data 'flush through' are not permissible.

Coefficients can be loaded from a host system using a conventional peripheral interface and separate data bus. Alternatively, they can be loaded as a complete set from a byte wide EPROM. The device produces addresses for the EPROM and a BUSY output indicates that the transfer is occurring. Up to sixteen devices can have their coefficients supplied from a single EPROM. These devices need not necessarily be part of the same filter network.

Each of the filter networks shown in Fig. 4 contains eight systolic multiplier accumulator stages, an example with four stages is shown in Fig. 5. Input data flows through the delay lines and is presented for multiplication with the required coefficient. This is added to either the last result from this accumulator or the result from the previous accumulator. The filter results progress along the adders at the data sample rate. If the sample rate equals SCLK divided by four, for example, then the accumulated result is passed onto the next stage every forth cycle. The structure described is highly efficient when used to calculate filtered results from continuous input data.

A comprehensive digital filter design program is available for PC compatible machines. This will optimise the filter coefficients for the filter type required and number of taps available at the selected sample rate within the VP16256 device. An EPROM file can be automatically generated in Motorola S-record format.

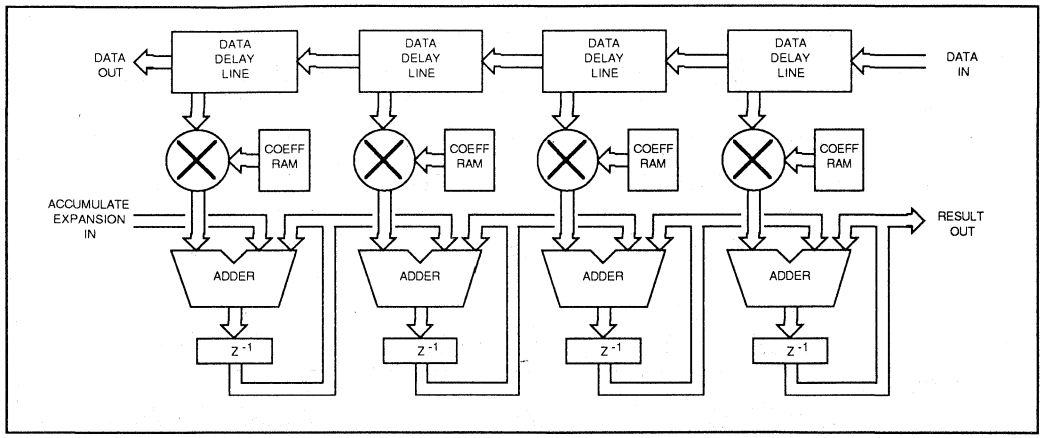


Fig. 5 Filter Network Diagram

SINGLE FILTER OPTIONS

When operating as a single filter the device accepts data on the 16 bit DA bus at the selected sample rate, see Figs 6 and 7. Results are presented on the 32 bit F bus, which may be tristated using the OEN input. Signal OEN is registered onto the device and does not therefore take effect until the first SCLK rising edge. Devices may be cascaded this allows filters with more taps than available from a single device. To accomplish this two further busses are utilised. The DB bus presents the input data to the next device in cascade after the appropriate delay, while, partial results are accepted on the X bus.

Single filter mode is selected by setting control register bit 15 to a one. The required filter length is then selected using control register bits 14 and 13 as summarised in Table 3. The options define the number of times each multiplier - accumulator is used per sample clock period. This can be once, twice, four times, or eight times.

In addition a normal/decimate bit (CR12) allows the filter length to be doubled at any sample rate. This is possible when the filter coefficients are selected to produce a low pass filter, since the filtered output would then not contain the higher frequency components present in the input. The Nyquist criterion, specifying that the sampling rate must be at least double the highest frequency component, can still then be satisfied even though the sampling rate has been halved.

CR 14	CR 13	CR 12	Input Rate	Output Rate	Filter Length	Setup Latency
0	0	0	SCLK	SCLK	16 Taps	16
0	0	1	SCLK	SCLK/2	32 Taps	17
0	1	0	SCLK/2	SCLK/2	32 Taps	16
0	1	1	SCLK/2	SCLK/4	64 Taps	18
1	0	0	SCLK/4	SCLK/4	64 Taps	20
1	0	1	SCLK/4	SCLK/8	128 Taps	24
1	1	0	SCLK/8	SCLK/8	128 Taps	24

Table 3. Single Filter Options

The system clock latency for a single device is shown in Table 3. This is defined as the delay from a particular data sample being available on the input pins to the first result including that input appearing on the output pins. It does not include the delay needed to gather N samples, for an N tap filter, before a mathematically correct result is obtained.

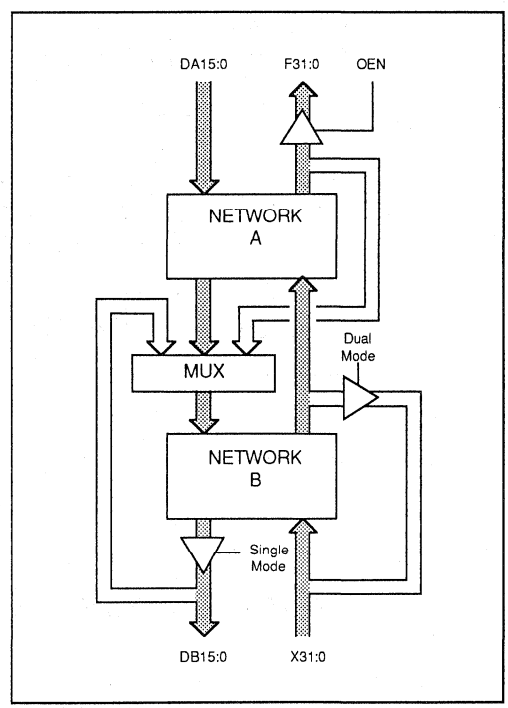
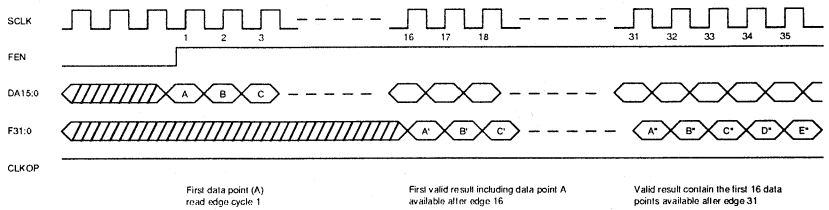
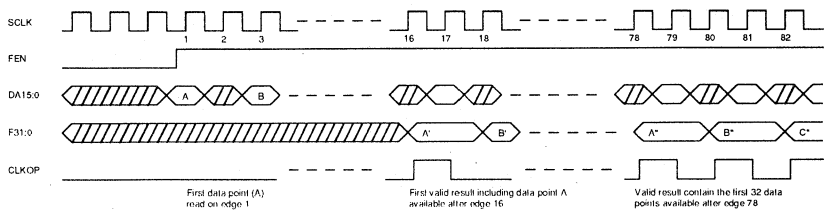


Fig. 6 Single Filter Bus Utilisation

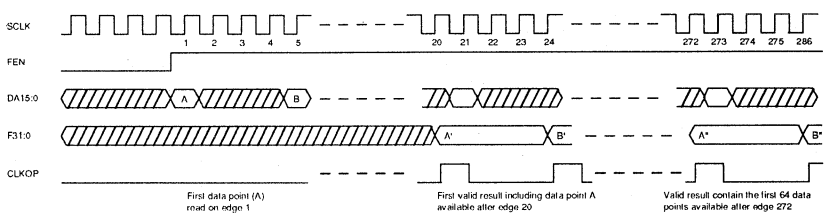
SPEED MODE 0 (Data input and output at the full SCLK rate) CR14:13 = 00, CR12 = 0



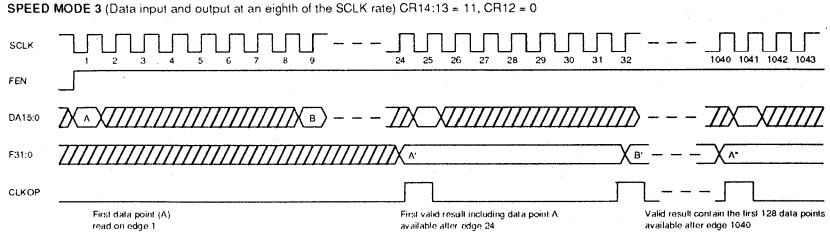
SPEED MODE 1 (Data input and output at half the SCLK rate) CR14:13 = 01, CR12 = 0



SPEED MODE 2 (Data input and output at a quarter of the SCLK rate) CR14:13 = 10, CR12 = 0



SPEED MODE 3 (Data input and output at an eighth of the SCLK rate) CR14:13 = 11, CR12 = 0



SPEED MODE 1 Decimating (Data input at half the SCLK rate and output at a quarter of the SCLK rate) CR14:13 = 01, CR12 = 1

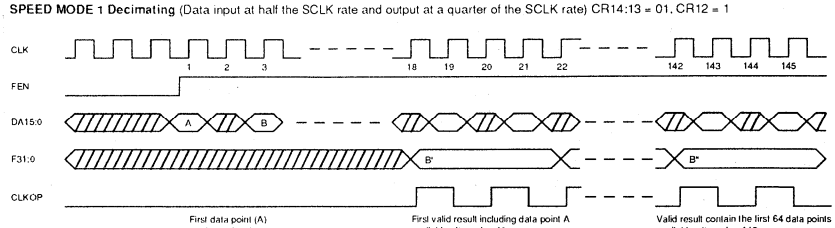


Fig. 7 Single Filter Timing Diagrams

DUAL INDEPENDENT FILTER OPTIONS

When operating as two independent filters the device accepts 16 bit data on both the DA and DB buses at the selected sample rate, see Fig. 8. Results are available from both the F and X buses. The F bus may be tristated using the OEN input. Signal OEN is registered onto the device and does not therefore take effect until the first SCLK rising edge

Each filter must be configured in the same manner, and multiple device expansion is not possible due to the pin reorganization. The latter requirement can, of course, still be satisfied by several devices configured as single filters.

Dual independent filter mode is selected by setting control register bits 15 and 4 to a zero. The required filter length is selected using control register bits 14 and 13 as summarised in Table 4, which also shows the resulting latency. As in single filter mode normal or decimate by two operation can be selected using control register bit 12.

CR 14 13 12	Input Rate	Output Rate	Filter Length	Setup Latency	
				Ind	Cas
0 0 0	SCLK	SCLK	8 Taps	16	27
0 0 1	SCLK	SCLK/2	16 Taps	17	-
0 1 0	SCLK/2	SCLK/2	16 Taps	16	28
0 1 1	SCLK/2	SCLK/4	32 Taps	18	-
1 0 0	SCLK/4	SCLK/4	32 Taps	20	36
1 0 1	SCLK/4	SCLK/8	64 Taps	24	-
1 1 0	SCLK/8	SCLK/8	64 Taps	24	40

Table 4. Dual Filter Options

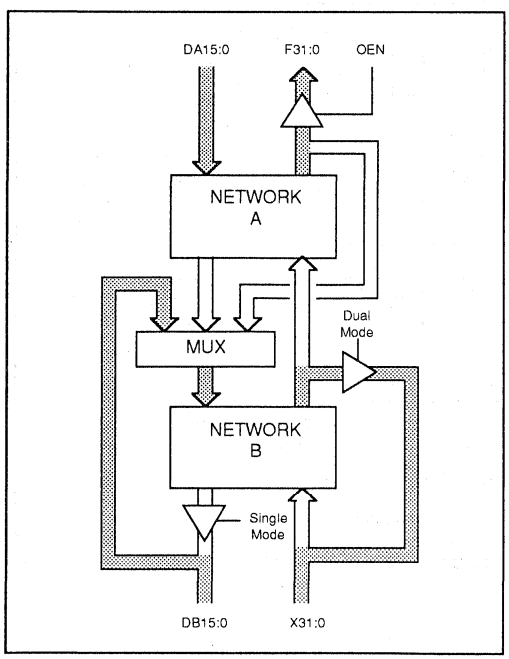


Fig. 8 Dual Independent Filter Bus Utilisation

DUAL CASCADED FILTER OPTIONS

When operating as two cascaded filters the device accepts 16 bit data on the DA bus at the selected sample rate. Results are presented on the 32 bit X bus, see Fig. 9. Each filter must be configured in the same manner. Multiple device expansion is not possible in this mode.

Dual cascaded filter mode is selected by setting control register bit 15 to a zero and bit 4 to a one. The required filter length is selected using control register bits 14 and 13 as summarised in Table 4, which also shows the resulting latency. The decimate by two option is not available in this mode.

The data for the second filter network is extracted as the middle 16 bits from the first networks accumulated result. For successful operation the first filter network must have unity gain. See the section on filter accuracy for more details.

The cascade option is used to increase the stop band rejection in a practical filter application. Theoretically, increasing the number of taps in an FIR filter will increase the stop band rejection, but this assumes floating point calculations with no accuracy limitations. In practice, with fixed point arithmetic, better performance is achieved with two smaller filters in series.

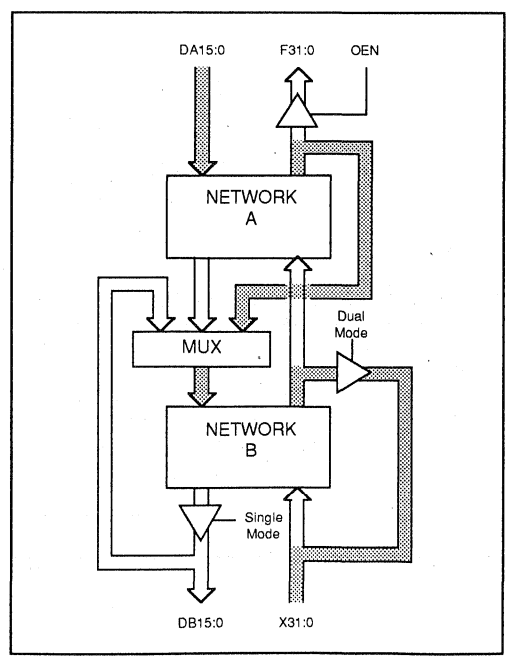


Fig. 9 Dual Cascaded Filter Bus Utilisation

FILTER ACCURACY

Input data and coefficients are both represented by 16bit two's complement numbers. The coefficients are converted to twelve bits by rounding towards zero. This is achieved as follows. If the coefficient is positive then the least significant 4 bits are discarded. If the coefficient is negative then the logical 'OR' of the least significant 4 bits are added to the remainder of the word. Twelve bit coefficients can be used directly provided the least significant four bits are set to zero.

The FIR filter results are calculated using a multiplier accumulator structure as shown in Fig. 10. The truncation and word growth allowed for in the data path are explained in Fig. 11. The 16 bit data and 12 bit coefficient inputs, (each with one sign bit before the binary point), are presented to the multiplier. This produces a 28 bit result with two bits before the binary point. Producing the full 28 bit result ensures that if both the data and coefficients are set to -1 a valid result is generated. Prior to entering the accumulator the least significant 4 bits of the multiplier result are truncated and the resulting 24 bits sign extended to 32 bits. The final accumulator result is 32 bits with 10 bits before the binary point. Thus 9 bits of word growth are allowed within the accumulator. All accumulator bits are made available on the output pins.

In cascade mode the middle 16 bits from the network A accumulator are fed round to the network B data inputs, see Fig. 11.

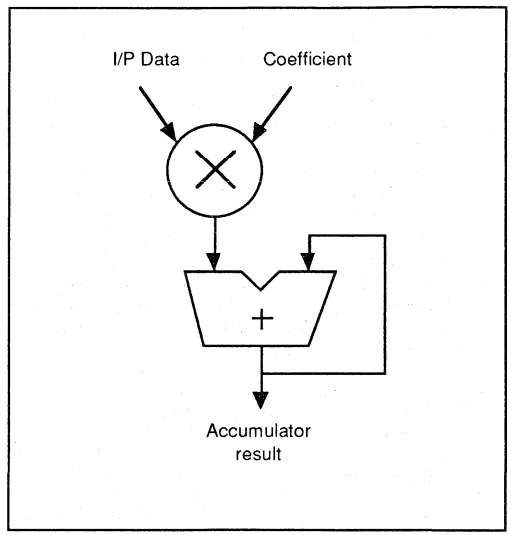


Fig. 10 Multiplier Accumulator

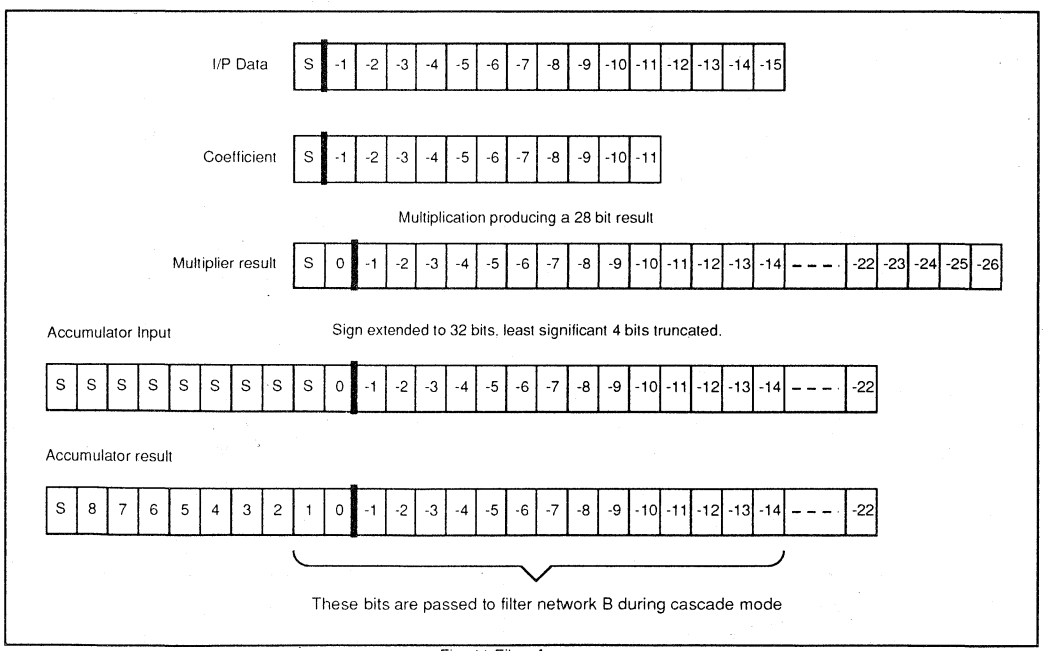


Fig. 11 Filter Accuracy

CASCADING DEVICES

When the filter requirements are beyond the capabilities of a single device, it is possible to connect several devices in cascade increasing the number of taps available at the required sample rate. Within each device all filter length, decimate, and bank swap options are still possible, but each device in the chain must be similarly programmed and configured as a single filter.

The number of devices which can be cascaded is only limited by the possibility of overflow in the 32 bit intermediate accumulations. If more than sixteen devices are cascaded in auto EPROM load mode, then an additional EPROM will be needed.

In modes where the data sample rate does not equal the clock rate. Then the cascade arrangement shown in Fig. 12 is utilised. Delayed data is passed from device to device in one direction, while intermediate results flow in the opposite direction. The interface device both accepts the input data and produces the final result. It is not necessary for each device to know its exact position in the chain, but the device which receives the input data and produces the final result must be identified, as must the device which terminates the chain. The former is known as the Interface device and the latter as the Termination device, all others are Intermediate devices. Control Register bits CR11:10 are used to define these positions as shown in Table 6.

The control logic in each of the devices must be synchronised with respect to the Interface device. This is achieved by connecting the Delayed Filter Enable output (DFEN) to the Filter Enable input (FEN) of the next device in the chain. The Interface device, itself, needs a Filter Enable signal produced by the system, unless the Free Run pin is pulled high. Even when the latter is true, the Filter Enable connection must be made between the remaining devices in the chain.

When devices are cascaded such that the data sample rate equals the clock rate, (Control register bits 14:13 = 00), then a different cascade configuration must be used. This is shown in Fig. 13. The number of devices which can be cascaded is, again, only limited by the 32 bit accumulators.

In this mode the delayed data is passed from device to device in the same direction as the intermediate results. The device which accepts the input data is now at the opposite end of the chain to the device which produces the final result. The control logic in each of the devices must be synchronised this is achieved by connecting all the device FEN inputs to the global Filter enable.

AVAILABLE OPTIONS

No more than 128 coefficients can be stored internally. This limits the filter length / decimate / bank swap options to those which do not require more than that number of coefficients. Thus when a filter with 128 taps is to be implemented in a single device, it is not possible to decimate or bank swap. When a filter with 64 taps is implemented, decimate or bank swap are possible, but not both. With all other filter lengths, all decimate and bank swap configurations are possible.

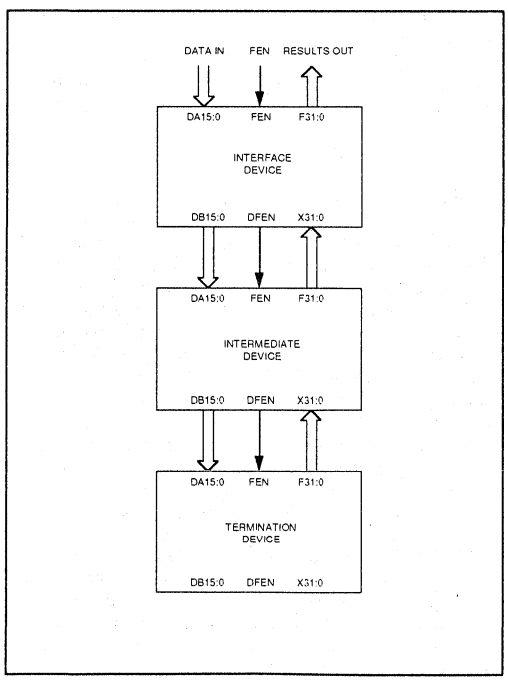


Fig. 12 Three Device Cascaded System

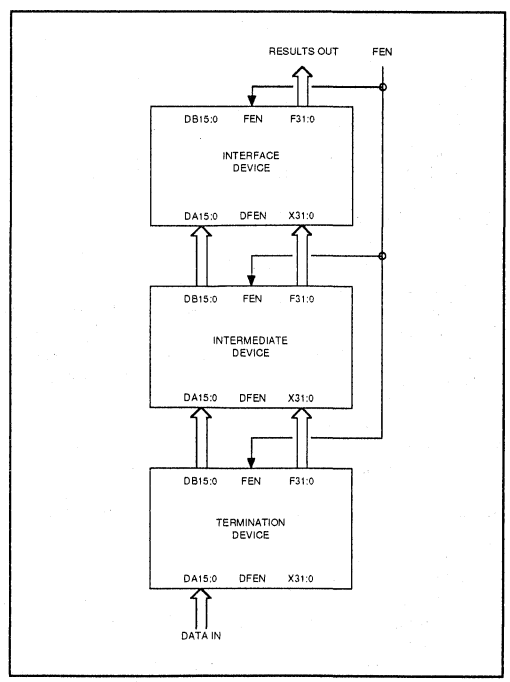


Fig. 13 Full Speed Cascaded System

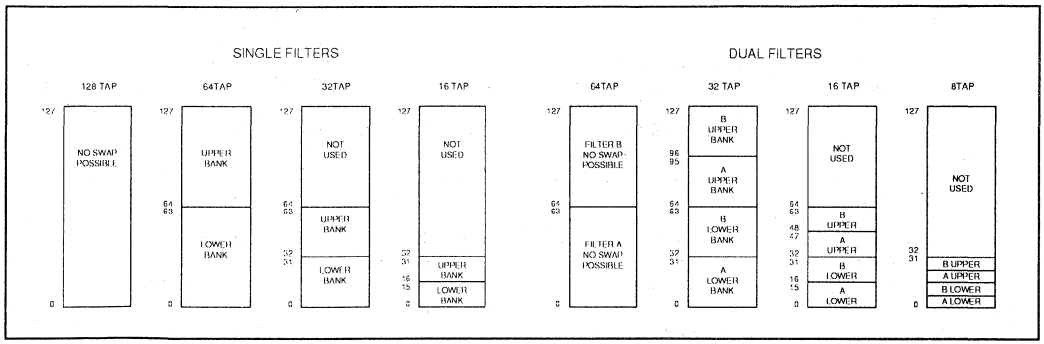


Fig. 14 Coefficient Memory Map

FILTER CONTROL

Two control modes are available selected by input signal FRUN. When FRUN is tied high the device will commence operation once the coefficients have been loaded. The CLKOP signal indicating when new input data is required and that new results are available, see Fig. 7. When FRUN is tied low filter operation will not commence until a high has been detected on signal FEN. This mode allows synchronisation to an existing data stream. Signal FEN should be taken high when the first valid data sample is available so that both are read into the device on the next SCLK rising edge.

During device reset the RES signal must be held low for a minimum of 16 SCLK cycles. After a reset the control register returns to it's default state of 8C80 Hex. This places the device into the following mode :

- Single filter
- Sample rate equal to the clock rate
- Non-decimating
- A single device (Not in a cascade chain)
- Bank swap selected by bit in the control register

COEFFICIENT BANK SWAP

A Bank Swap feature is provided which allows ALL coefficients to be simultaneously replaced with a different set. A bit in the Control Register (CR7) allows the swap to be controlled by either input signal SWAP or Control Register bit (CR6). The latter is useful if the device is controlled by a microprocessor, when driving a separate pin would entail additional address decoding logic and an external latch.

If the pin or control register bit is low, the coefficients used will be those loaded into the lower banks illustrated in Fig. 14. When the pin or bit is high, the upper banks are used.

The actual swap will occur when the next sampling clock active going transition occurs. This can be up to seven system clocks later than the swap transition, and is filter length dependent. The first valid filtered output will then occur after the pipeline latancies given in Tables 3 and 4.

By setting a bit in the Control Register it is possible to bank swap on every data sampling clock. This function does not depend on the status of the SWAP pin or bit, and the lower bank will be initially selected after FEN goes active. The option can be used to implement filters with complex coefficients.

LOADING COEFFICIENTS

When the device is to operate in a stand alone application then the coefficients can be down loaded as a complete set from a previously programmed EPROM. Alternatively if the system contains a microprocessor they can be individually transferred from a remote master under software control. In any mode the system clock must be present and stable during the transfer, and the addressing scheme is such that the least significant address specifies the coefficient applied to the first multiplier seen by incoming data.

The addresses used during the load operation are those illustrated in Fig. 14. The Control Register is loaded when CCS is high. In BYTE mode address A0 is used to select the portion of control register loaded, otherwise the address bits are redundant. When an EPROM is used to provide coefficients, this redundancy causes the number of locations needed for any device to be double that for the coefficients alone.

AUTO EPROM LOAD

When the EPROM pin is tied low, the VP16256 assumes the role of a master device in the system and controls the loading of coefficients from an external EPROM, see Fig.15. A load sequence commences when the RESET input goes inactive, and will continue until every coefficient has been loaded. The BUSY pin goes high to indicate that a load sequence is occurring and the filter output is invalid. The device will not commence a filter operation until the Filter Enable edge is received (FEN) after BUSY has gone low. This requirement can be avoided if the Free Run pin (FRUN) is tied high.

The address bus pins become outputs on the Master device, and produce a new address every four system clock periods. This four clock interval, minus output delays and the data set up time, defines the available EPROM access time.

The coefficients are always loaded as bytes. The state of the BYTE pin on the master device is ignored. This arrangement also allows the eight, most significant, coefficient bus pins (C15:8) to be used for other purposes as described later. Since the 16 bit coefficients are loaded in two bytes the A0 pin specifies the required byte. The maximum number of stored coefficients is 128, eight address outputs are therefore provided for the EPROM. These eight outputs from the Master

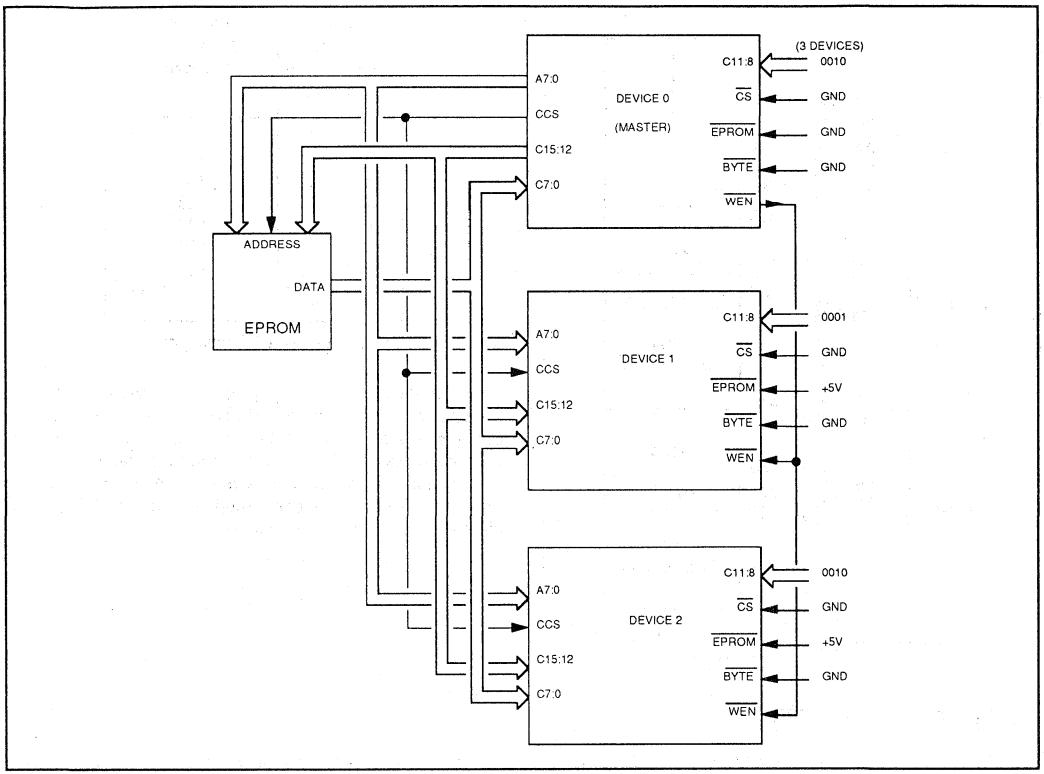


Fig. 15 Three device auto EPROM load

must also drive the address inputs on the slave devices.

When the filter length is less than the maximum, the VP16256 will only transfer the correct number of coefficients, and one or more significant address bits will remain low. Sufficient coefficients are always loaded to allow for a possible Bank Swap to occur, and the EPROM allocation must allow for this even if the feature is not to be used. Table 5 shows the number of coefficients loaded for each of the modes.

If several devices are cascaded, only one device assumes the role of the Master by having its EPROM pin grounded. It produces a Write Enable signal for the other devices, plus four higher order address outputs on C15:12. The extra address bits on C15:12 define separate areas of EPROM, containing coefficients for up to fifteen additional devices. The least significant block of memory must always be allocated to the Master device. The additional devices need not in practice be all part of the same cascaded chain, but can consist of several independent filters. They must, however, all have their BYTE pins tied low.

When one EPROM is supplying information for several devices, some means of selectively enabling each additional device must be provided. This is achieved by using the C11:8 pins on the slave devices as binary coded inputs to define one to fifteen extra devices. These coded inputs always correspond to the block address used for the segment of EPROM allocated to that device. Code 'all zeros' must not be used since the Master device has implied use of the bottom segment. This is necessary since the C11:8 pins are alternatively used on the Master device to define the number of devices supported by the EPROM.

In addition to providing the most significant addresses to the EPROM, the C15:12 address outputs from the master device must also drive the C15:12 inputs on the slave devices. These C15:12 inputs are internally compared to the C11:8 inputs to decide if that device is currently to be loaded. This approach avoids the need for external decoders and makes the Chip Enable input redundant. This input, however, must be tied low on every device in an EPROM supported system.

The Control Coefficient pin (CCS) is used to define when the control register is to be loaded. It becomes an output on the Master device which provides an EPROM address bit next in significance above A7:0, and also drives the CCS inputs on the slave devices. This output is high for the first two EPROM transfers in order to access the control information, and then remains low whilst the coefficients are loaded. This control information is thus not stored adjacent to the coefficients within the EPROM, and in fact the EPROM must provide twice the storage necessary to contain the coefficients alone. All but two of the bytes in the additional half are redundant. See Fig.16 for the EPROM memory map.

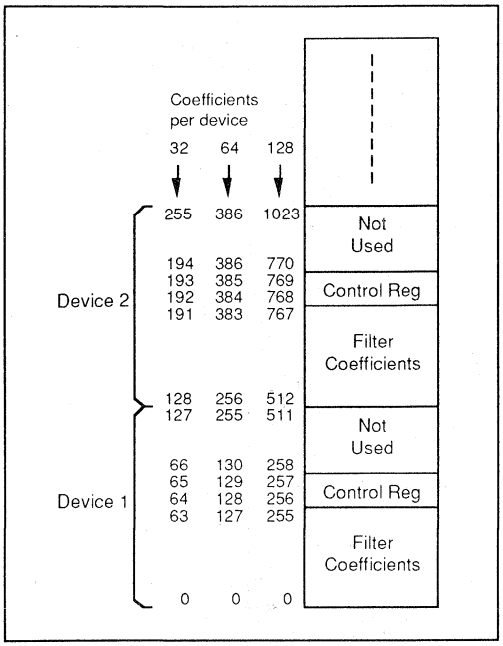


Fig. 16 EPROM Memory Map

Control Register 14 13 12	Number of Coefficients Loaded
0 0 0	32
0 0 1	64
0 1 0	64
0 1 1	128
1 0 0	128
1 0 1	128
1 1 0	128
1 1 1	Invalid Mode

Table 5. Number of Coefficients loaded

NOTE the EPROM memory map Fig. 16 assumes that, for the 32 and 64 coefficient per device options, that the unused address pins are unconnected. If all address pins are connected as shown in Fig. 15 then the 128 coefficients per device memory map column should be used. Only those coefficients required will be read, hence the upper portions of the coefficient address space will be ignored.

USING A REMOTE MASTER

When a remote master is used to load coefficients, the EPROM pin must be tied high and a conventional peripheral interface is then provided. It is not possible, however, to read coefficients already stored. The master supplies an address and data bus, and writes to the VP16256 occur under the control of synchronous Chip Enable and Write Strobe inputs. The Coefficient Control Register pin (CCS) must be driven by a master address line higher in significance than A7:0. Both the WEN and CS signals must be low for the load operation to occur. When loading the control register the CS signal must be held low for a further 2 cycles see Fig. 17. Since the internal write operation is actually performed with the system clock, it is necessary for the clock to be present during the transfer.

The BYTE input defines whether coefficients are loaded as a single 16 bit word or two 8 bytes. The latter saves on connections to the remote master. Address bits A7:0 are used in BYTE mode. 16 bit word mode uses bits A6:0, A7 being redundant. When writing in byte mode the least significant byte (A0 = 0) must be written first followed by the most significant byte (A0 = 1).

In the byte mode of working the internal comparison between C15:12 and C11:8 is made, regardless of the state of the EPROM pin. For this reason pins C15:8 should all be tied low when a remote master is used with byte transfers. This ensures that the internal comparison gives equality and allows the load operation to occur.

The address and coefficient busses plus the Write Enable and CS signals must all meet the specified set up and hold times with respect to the system clock, see Fig 17. This synchronous interface is optimum for the majority of high end applications, when individual coefficients must be updated at sample clock rates. If, for convenience reasons, the coefficients are loaded under software control from a general purpose microprocessor, the Write Enable will probably be asynchronous to the system clock used by the VP16256. In this case external synchronising logic is needed, see Fig.18.

Fig. 19 shows the recommended loading sequence and filter operation initiation. The simplest technique is to reset the device prior to loading a set of coefficients. Coefficients may be loaded once BUSY returns low or 22 cycles after RESET is taken high.

When loading a device from a remote master the control register must be loaded first followed by the filter coefficients. Fig. 19 shows the required loading sequence, two examples are given one for byte mode the other for word mode. A gap of at least one cycle must be left after loading the control register before loading the first coefficient.

Filter operations are started by presenting the first data word at the same time as raising signal FEN.

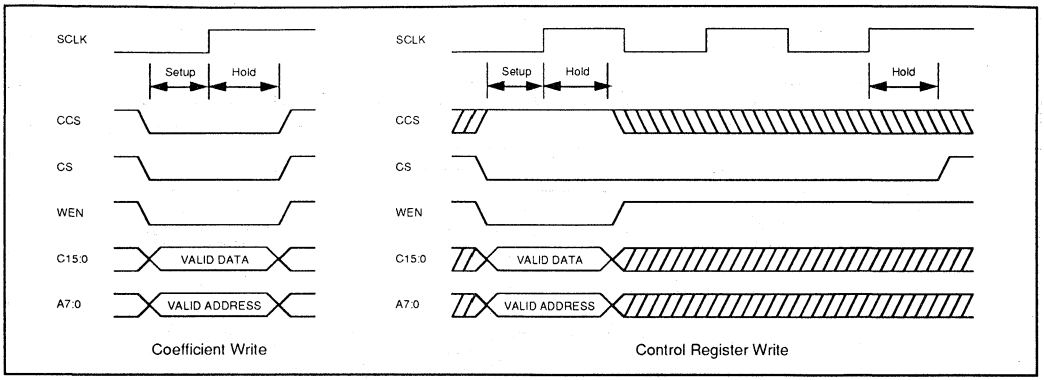


Fig. 17 Remote Master Setup & Hold Timings

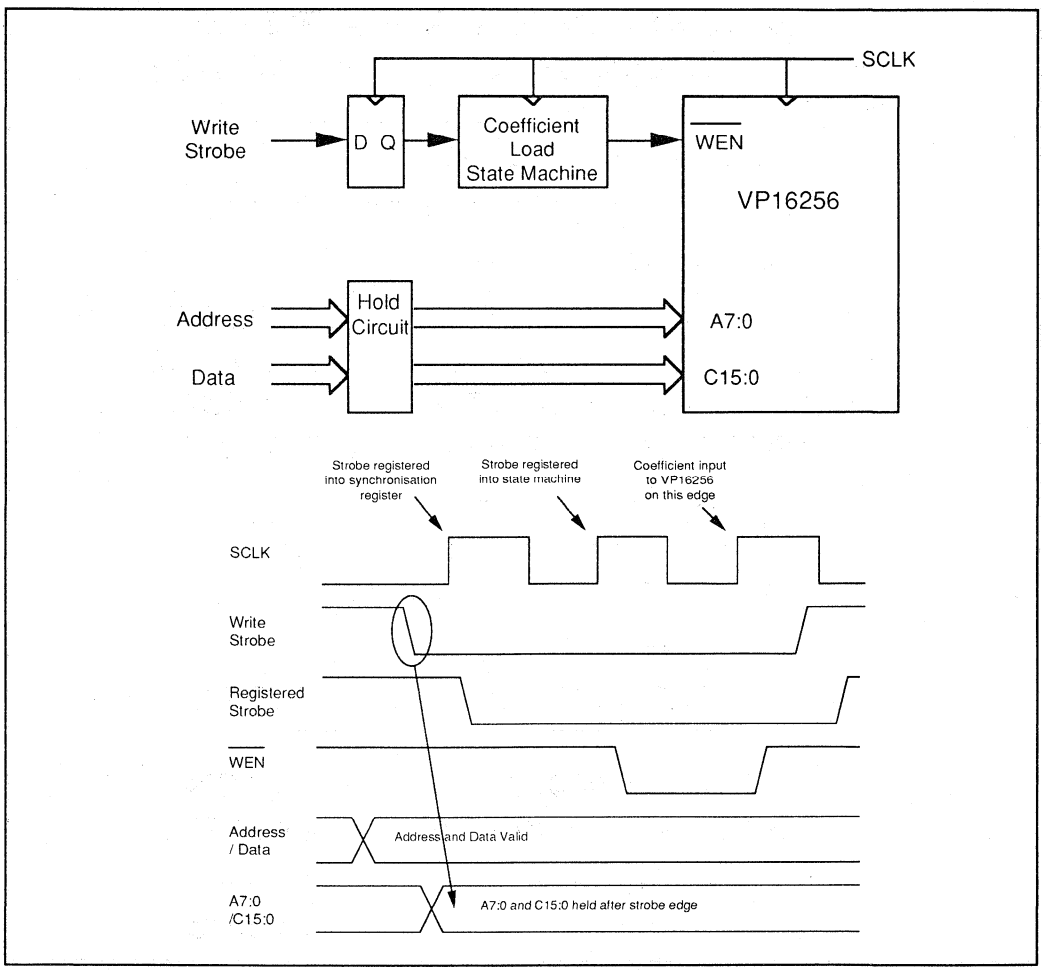


Fig. 18 Remote Master Synchronisation

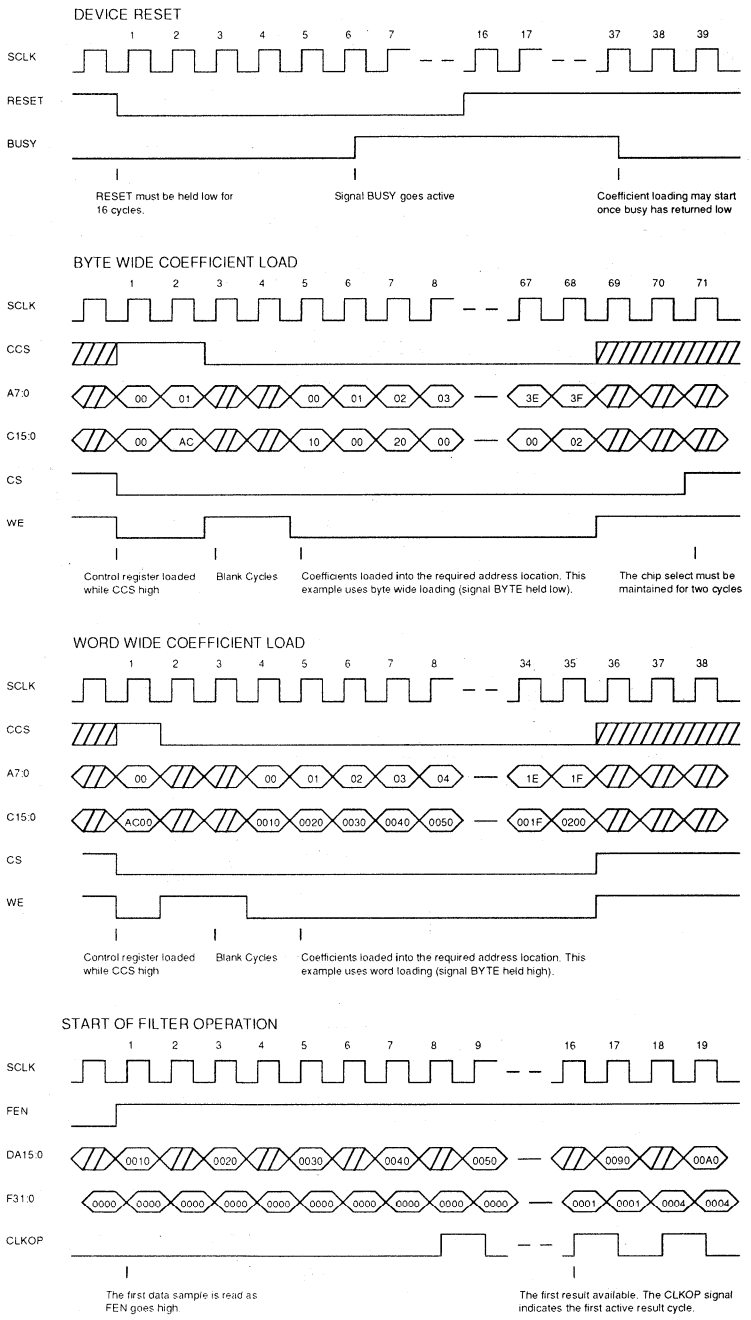


Fig. 19 Device Startup

CONTROL REGISTER

The internal operation of the VP16256 is controlled by the status of a 16 bit control register. In the dual filter modes both networks are controlled by the same register. The significance of the various bits are shown in Table 6. Tables 7 and 8 define the control register bit interdependence for the filter and bank swapping modes.

The control register is double buffered. This allows the writing of a new control word without affecting the current operation of the device. To activate the new control register after it has been written to the device the bank swap signal must be toggled. After a reset the active control register is loaded directly and bank swap need not be used.

Control Register Bits		Function
15	4	
0	0	Two independent filters
0	1	Two filters in cascade
1	X	Single Filter

Table 7 Control Register Filter Mode Bits

Control Register Bits			Function
7	6	5	
0	X	0	Control by input pin
1	0	0	Lower bank selected
1	1	0	Upper bank selected
X	X	1	Swap on every sample clock

Table 8 Control Register Bank Swap bits

Bits	Decode	Function
15	0	Dual filter mode
15	1	Single filter mode
14:13	00	Sample rate is the system clock
14:13	01	Sample rate is half the system clock
14:13	10	Sample rate is quarter the system clock
14:13	11	Sample rate is eighth the system clock
12	0	Output rate equals the input rate
12	1	Decimate bt two
11:10	00	Intermediate device
11:10	01	Interface device
11:10	10	Termination device
11:10	11	Single device
9:8	00	These bits MUST be at logical zero
7	0	Bank swap is controlled by input pin
7	1	Bank swap is controlled by Bit 6
6	0	Lower bank if Bit 7 is set
6	1	Upper bank if Bit 7 is set
5	0	Normal Bank Swap
5	1	Bank swap on every sample clock
4	0	Two independent filters
4	1	Two filters in cascade
3:0		These bits MUST be at logical zero

Table 6. Control Register Bit Allocation

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage Vcc	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to Vcc + 0.5V
Output voltage V_{OUT}	-0.5V to Vcc + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HBM)	500V
Storage temperature T_S	-65°C to 150°C
Ambient temperature with power applied T_{AMB}	-55°C to +125°C
Junction temperature with power applied T_J	150°C
Package power dissipation	3000mW
Thermal resistances	
Junction to Case σ_{JC}	5°C/W

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device
5. Vcc = Max, Outputs Unloaded, Clock Freq = Max
6. The σ_{JC} data assumes that heat is extracted from the top face of the package.

ELECTRICAL CHARATERISTICS

Operating Conditions (unless otherwise stated)

Commercial: T_{AMB} = 0°C to +70°C $T_{J(MAX)}$ = 100°C Vcc = 5.0V±5% Ground = 0V

Static Charateristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage (CMOS)	V_{IH}	3.5		-	V	SCLK input only
Input low voltage (CMOS)	V_{IL}	-		1.0	V	SCLK input only
Input high voltage (TTL)	V_{IH}	2.0		-	V	All other inputs
Input low voltage (TTL)	V_{IL}	-		0.8	V	All other inputs
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{CC}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{CC}
Output S/C current	I_{OS}	10		300	mA	V_{CC} = Max

Switching Characteristic	Commercial		Industrial		Military		Units	Conditions
	Min.	Max.	Min.	Max.	Min.	Max.		
Input signal setup to clock rising edge	8	-	8	-	8	-	ns	
Input signal hold after clock rising edge	4	-	4	-	4	-	ns	
OEN setup to clock rising edge	20	-	20	-	20	-	ns	
OEN hold after clock rising edge	4	-	4	-	4	-	ns	
Clock rising edge to output signal valid	5	26	5	28	5	28	ns	30pF
Clock Frequency	-	25	-	20	-	20	MHz	
Clock High Time	18	-	20	-	20	-	ns	
Clock Low Time	11	-	12	-	12	-	ns	
Clock to data valid from high impedance	-	30	-	30	-	30	ns	see Fig. 20
Clock to data high impedance	-	30	-	30	-	30	ns	see Fig. 20
Vcc Current	-	320	-	250	-	250	mA	see Note 5

Test	Waveform - measurement level
Delay from output high to output high impedance	V_H, 0.5V
Delay from output low to output high impedance	V_L, 0.5V
Delay from output high impedance to output low	1.5V, 0.5V
Delay from output high impedance to output high	1.5V, 0.5V

V_H - Voltage reached when output driven high
V_L - Voltage reached when output driven low

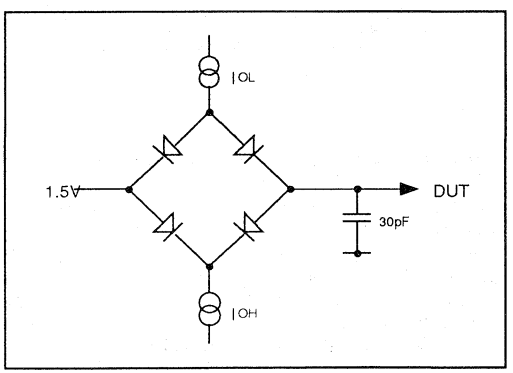


Fig. 20 Three state delay measurement load.

ORDERING INFORMATION

VP16256/CG/GH1R 25MHz, Commercial plastic power package

Section 9
DSP Evaluation Board

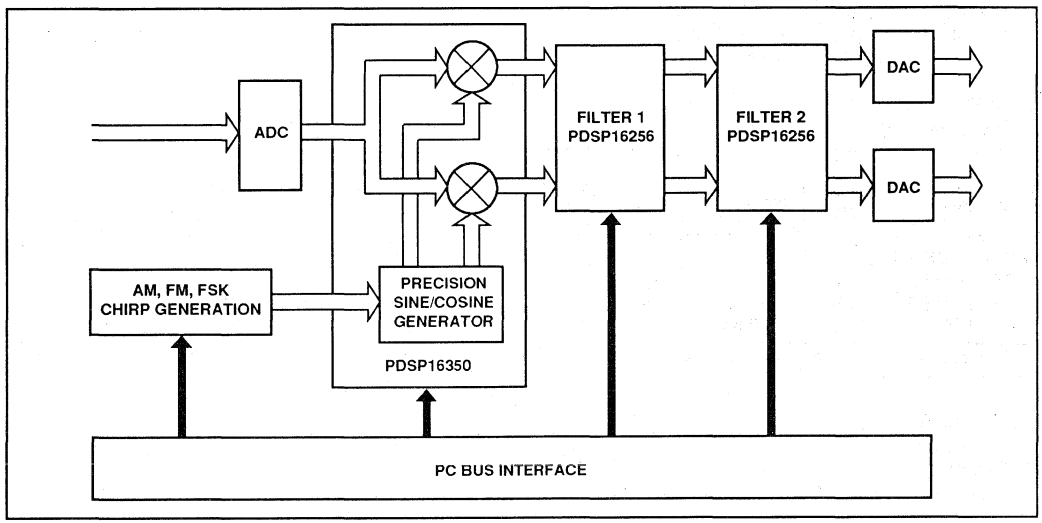
GEC PLESSEY
SEMICONDUCTORS

DS3854 - 2.0

PDSP16256/PDSP16350 EVALUATION SYSTEM

AN IBM PC COMPATIBLE DEVELOPMENT SYSTEM FOR HIGH PERFORMANCE DIGITAL FILTERING AND SIGNAL GENERATION USING THE PDSP16256 AND PDSP16350

(Supersedes version in June 1995 Digital Video & Digital Signal Processing IC Handbook, HB3923-2)



The evaulation system provides a complete environment for the development of high performance digital filtering and signal generation systems. The development system is based on the powerful GEC Plessey Semiconductors' PDSP16350 and PDSP16256 digital signal processing components and comprises the following elements:

- An IBM PC compatible board for high performance digital filtering and signal generation
- A powerful digital filter design software package optimised to the specific characteristics of the PDSP16256 programmable FIR filter
- A flexible digital filter development software package enabling the board to be configured and operated in a wide range of modes
- Comprehensive supporting documentation

These facilities constitute an easy-to-use development tool for digital filtering systems requiring sample rates of up to 20MHz and provide an ideal environment for rapidly evaluating the capabilities of these high performance GEC Plessey Semiconductors devices.

APPLICATIONS

The evaulation system is applicable to a wide range of areas, including:

- Radar
- Ultasonics
- Video processing
- Digital radio
- Sonar
- Data communications
- Instrumentation
- Satellite communications

DIGITAL FILTERING BOARD

Key features of the IBM PC compatible board are as follows:

General

- 8- or 12- bit ADC versions
- Dual 12-bit DACs
- 16-bit data
- Real or quadrature modes of operation
- Sample rates between 1kHz and 200MHz
- Digital output ports

Digital Filtering

- Configurable as separate I and Q channels or as a single real only channel
- Cascaded or single filter options
- Filtering lengths between 8 and 128 coefficents (dependent on sample rate and configuration)
- Decimate by 2 mode

Signal Generation

- High resolution sine/cosine generation
- Supports amplitude modulation (AM) and frequency modulation (FM)
- High precision quadrature chirp signal generation

PDSP16256/PDSP16350 EVALUATION SYSTEM

DEVELOPMENT SOFTWARE

- Filtering designs optimised to the characteristics of the PDSP16256
- Cascaded, dual or single filter modes
- Frequency selective and Hilbert transform filters
- Bit-accurate frequency responses
- EPROM file generation
- Flexible board configuration options
- Filter coefficient loading
- Control of precision waveform generation
- Easy-to-use menu driven operation

ORDERING INFORMATION

The following options are available:

Part number	ADC sample rate	ADC resolution	No. of PDSP16256 ICs
PDSP DFDS-1	20MHz	8 bits	1
PDSP DFDS-2	20MHz	8 bits	2
PDSP DFDS-3	1MHz	12 bits	1
PDSP DFDS-4	1MHz	12 bits	2

All options include the following IBM PC compatible hardware and software:

- Digital filtering board
- Digital filter design package
- Digital filter development package
- Support documentation

Note Owing to the pending obsolescence of certain devices the supply of this evaluation board may be discontinued during the life of this handbook. Please confirm availablity with your GPS Customer Service Centre.

Section 10
Application Notes

See next page for the index to this section.

GEC PLESSEY
SEMICONDUCTORS

A LOW COST 1.5 to 2.2GHz VOLTAGE CONTROLLED OSCILLATOR

The introduction of the GPS range of 2GHz synthesisers and prescalers for low cost applications such as consumer satellite TV reception has created the requirement for an economic VCO design covering a frequency range from around 1.5GHz to 2.2GHz. Although suitable hybrid oscillator designs are available from various manufacturers, these generally carry a price tag at least an order of magnitude higher than the synthesiser, thus making their use in consumer equipment hopelessly uneconomic.

The design shown in Fig.1 has been developed using low cost components which should be easily available, the varicap diodes being normal UHF TV tuning types and the transistor a standard catalog item.

A major problem when operating at these frequencies is that the series inductance of most capacitors becomes very significant compared with that required in the resonator circuit and also prevents good decoupling. These problems are overcome when designing fixed frequency oscillators by replacing the normal resonant circuits and decoupling capacitors with open or short circuited resonant transmission lines but a design requiring wide frequency variation must use more conventional techniques.

The transistor is biased to about 1.5mA using a 22kΩ resistor from collector to base. Any problems with decoupling at the emitter are avoided by connecting the emitter direct to ground. Stabilisation of the bias point relies on the 330Ω collector load resistor providing a degree of feedback A small inductor in series with the collector load resistor reduces any loading and improves the effectiveness of the +12V supply decoupling A series tuned circuit consisting of a small inductor and two varicap diodes is connected between collector and base with a 390pF capacitor providing DC isolation of the varicap diodes from the collector voltage. To avoid the introduction of any additional series inductance, the varicap diodes are connected direct to the transistor base without a coupling capacitor The oscillator frequency is varied by adjusting the varicap bias voltage from 0 to 30V via a 47kΩ isolating resistor Output amplitude from the basic oscillator is much higher than the input requirements of the synthesiser or prescaler and therefore about 10dB of attenuation is provided by a resistive attenuator.

As might be expected with an oscillator operating at this frequency, layout is fairly critical and the layout shown in Fig.2 should be followed accurately or extensive trials made before any variations are attempted. The prototype oscillators were made on standard 1/16 inch fibreglass board, but it was found impossible to mount the frequency determining components on the board without greatly affecting the frequency range available; these components are therefore mounted off board, relying on short lead lengths to provide sufficient rigidity.

OSCILLATOR SPECIFICATION

Operating Voltage: +9V to +14V
Frequency Range: 1.5GHz to 2.2GHz
Varicap Voltage Range: 0V to +30V
Output Level: (with 10dB attenuator) -10dBm (70mV)

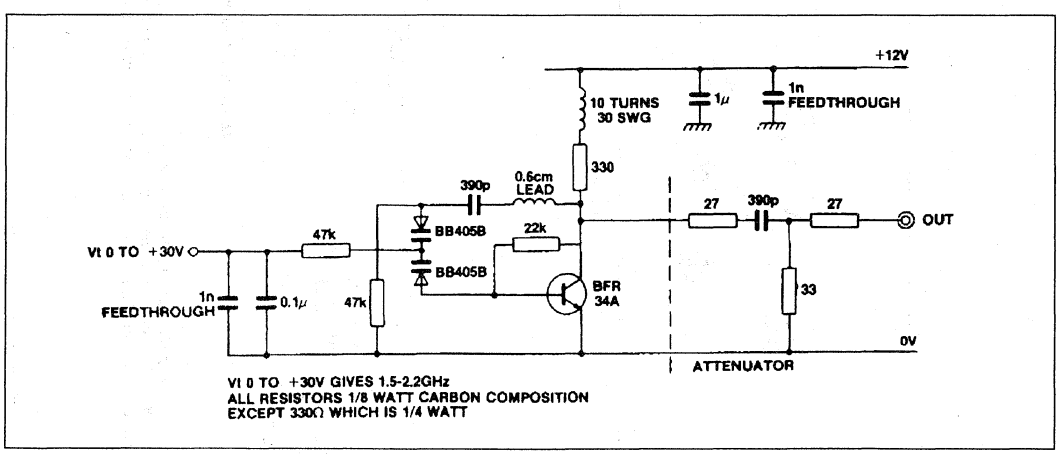


Figure 1: 2GHz VCO Circuit Diagram

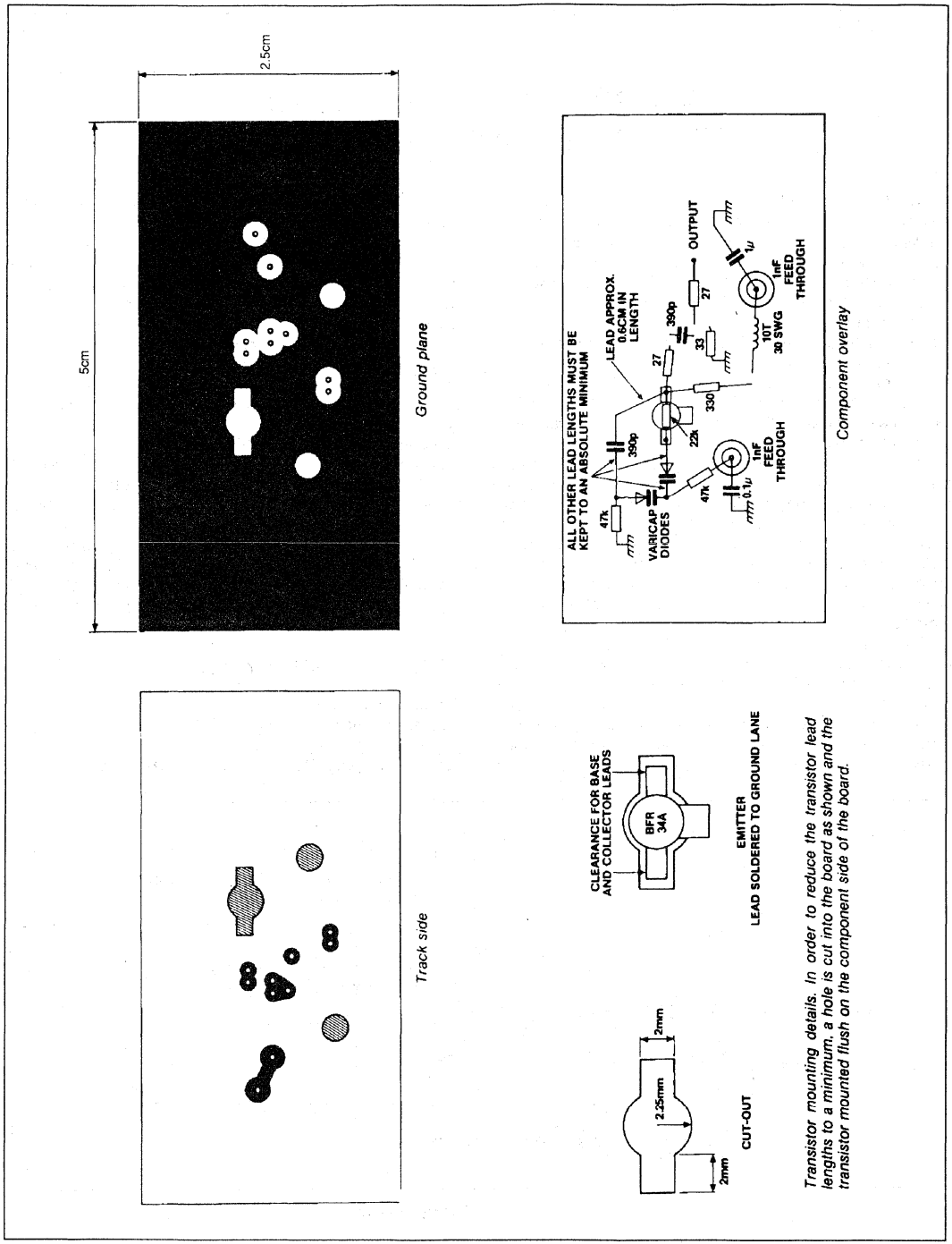


Figure 2: Oscillator printed board layout

AN168

TV/SATELLITE SYNTHESISERS - BASIC DESIGN GUIDELINES

EXTERNAL NOISE PROBLEMS

I²C BUS RADIATION PROBLEMS

The main problem when designing PCBs using any I²C device is that data and clock are always being transmitted and fed to the transceivers. This can lead to problems with radiation unless suitable precautions are taken.

Coupling from the SCL and SDA lines can often occur where these lines are long tracks leading to the synthesiser. The SCL and SDA lines pose particular problems as clock and data are always present on the I²C databus, regardless of whether the synthesiser is being addressed or not. These can couple into the synthesisier through any of the pins; it is therefore important to ensure that all pins are decoupled where possible. Unused ports should be taken to ground. Small decoupling capacitors may be placed directly on the pin to cut radiation into ports.

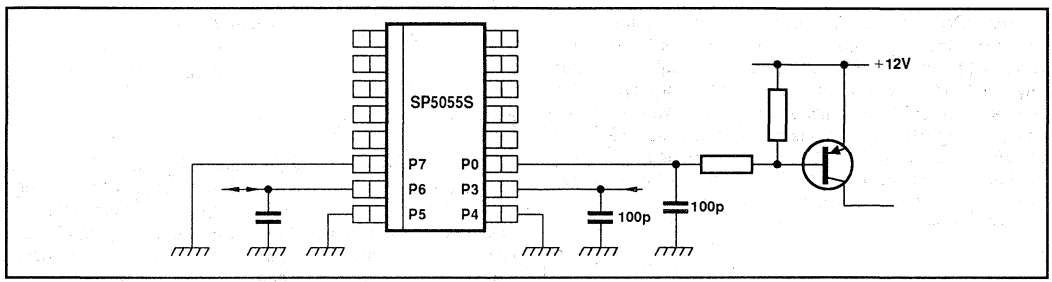


Fig.1 Decoupling/grounding of used and unused ports

I²C BUS LINE FILTERING

I²C bus specifications permit a maximum of 400pF on the SDA andSCL lines. This figure refers to the maximum total capacitance present on the bus so therefore includes other devices. Most applications use a combination of 100pF decoupling capacitors on each line together with a series resistor of up to 100kΩ, depending on the clock rate.

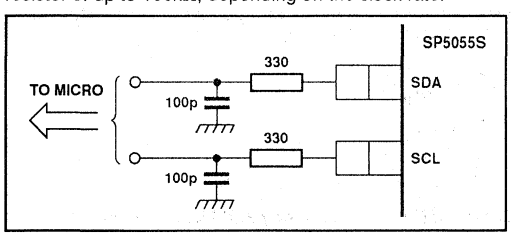


Fig.2 I²C bus line filtering

SYNTHESISER DECOUPLING

Supplies should be decoupled as close to the chip as possible. It is suggested that combination of 100pF and 100nF is used to give the best possible immunity against low and high frequency noise.

Layout

Care must be taken with layout to ensure that the supply rails are as short as possible and that no loops (either ground or supply) exist. If the layout permits, the V_{CC} line should not be routed near the loop filter.

Grounding

The synthesiser should be taken to a clean ground separate from the track used to ground any of the oscillators. If possible, shielding should be introduced between the oscillators and the synthesiser to ensure that no spurious coupling occurs.

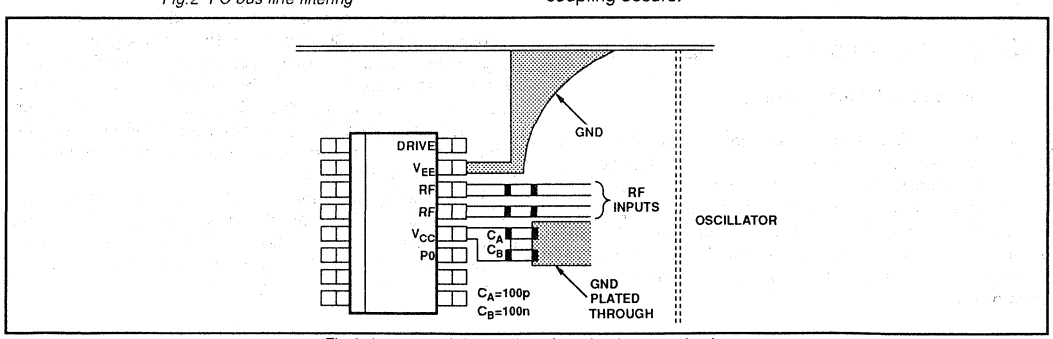


Fig.3 Layout and decoupling of synthesiser supply pins

VARACTOR LINE FILTERING

Special care should be taken with the varactor line. A low pass filter may be placed in the varactor line to prevent ripple being fed along the line and mistuning the oscillator. A typical application is shown in Fig.4.

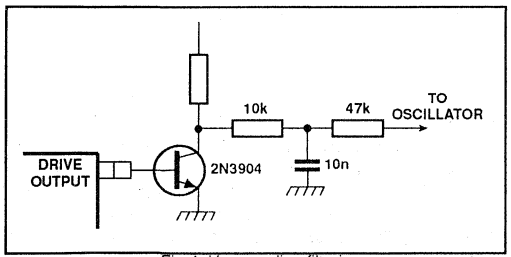


Fig.4 Varactor line filtering

The NPN transistor TR1, connected to the drive output, should be placed as close to the drive output pin as possible. The input to this transistor presents a very high impedance. Any length of track between the drive output of the synthesiser and the base of TR1 can act as an antenna which will feed unwanted signals into the transistor. To minimise this effect, a low value capacitor of, say 39pF may be connected between the base and collector of TR1 (as shown in Fig.5) without modifying the dominant loop characteristics.

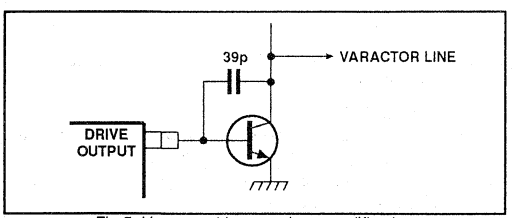


Fig.5 Varactor drive transistor modification

It is important that no other RF signals which may be present in the tuner, for example IF outputs, are routed anywhere near the synthesiser as they can also couple into the device.

All of the above suggestions are made in an attempt to achieve the best possible phase noise and sideband performance for the synthesised oscillator. Whilst a good synthesiser application does not guarantee good phase noise performance, a bad synthesiser application will almost certainly limit the overall performance of the tuner and degrade phase noise compared to that of a free-running oscillator.

CALCULATION OF LOOP COMPONENT VALUES

Applications Circuit (See Figure 6)

A typical synthesiser application circuit is shown in Figure 6. The optional additional filtering (referred to by Note 1 on this diagram) rolls off at a frequency well above the main loop filter. Its main purpose is to reduce any noise picked up on the varactor control line. Consequently its effect is ignored in this analysis. The following is a summary of the derivation of the basic design equations used to calculate the loop filter components.

Phase Detector Gain (See Figure 7)

The phase detector outputs pulses of current I_{cp} μA with a pulse frequency equal to the comparison frequency $\frac{\omega_{in}}{M}$ and width proportional to the phase error. These pulses are averaged by the loop filter so that the phase detector gain is given by:-

$$Kd = \frac{I_{cp}}{2\pi} \ \mu A/\text{radiation} \qquad ....(1)$$

Loop filter analysis (See Figure 8)

The loop filter converts the current pulses from the charge pump into a voltage proportional to the phase error. The filter recommended for normal applications is shown in fig 8(c). The transfer characteristic is :

$$F(S) = \frac{(1+s\tau_2)}{s\tau_1(1+s\tau_3)}$$

where $\tau_1 = C_1$

$\tau_2 = (C_1+C_2)\,R_2$

$\tau_3 = C_2, R_2$

Procedure for design of filter

Fig.8b shows an exact equivalent of the filter in figure 8(a). It is not possible to implement this configuration since the only points which are accessible are the input and output of the op-amp, but it serves as a useful design model. If C_2 and R_1 are incorporated as a current "pulse integrator" into the phase detector then the remaining components consisting of the op-amp, resistor $[1 + C_2/C_1]\,R_1$ and capacitor C_1 can be regarded as the loop filter.

This procedure allows us to treat the filter as a 2nd order loop rather than the more complex 3rd order loop of figure 8(a). This loop will have a natural frequency of ω_o and damping factor ζ which we can select based on the application. The cut off frequency of the "pulse integrator" would normally be set to $5\omega_o$ or more. By manipulation of the transfer function (see appendix) we can derive simple approximate design formulae for C_1, R_2 and C_2. These are:-

$$C_1 = \frac{KdKo}{PN\omega_o^2}$$

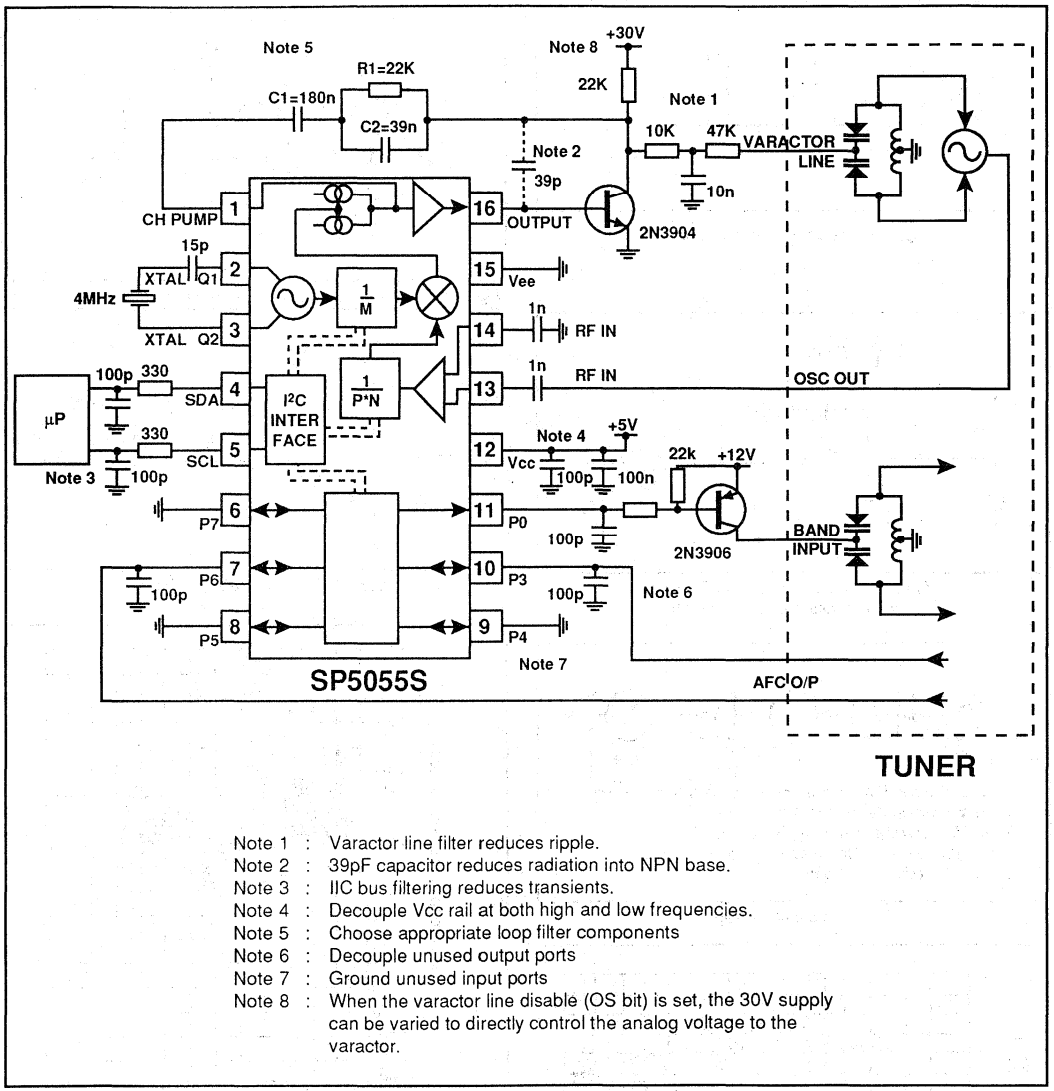
$$C_2 = C_1/5$$

$$R_2 = \frac{2\zeta}{\omega_o C_1}$$

Choice of Natural Frequency and Damping Factor

When the synthesiser is reprogrammed, the application will usually require the VCO to settle to the new frequency within a specified time to a specified accuracy. Appendix 3 (Time Domain Response) shows that the time domain response to a frequency step is an exponentially decaying sinusoid. From this the natural frequency ω_o can be calculated if we specify the settling time t_s and the accuracy $\omega_e/\Delta\omega$, provided we already know the damping factor ζ.

The damping factor must be chosen so that the system remains stable. For this the phase margin should be reasonably high say 0, > 45° or so. See Appendix 3 (Phase margin). The amount of 'overshoot' might also be used to estimate a value for ζ. See Figure 11.



Note 1 : Varactor line filter reduces ripple.
Note 2 : 39pF capacitor reduces radiation into NPN base.
Note 3 : IIC bus filtering reduces transients.
Note 4 : Decouple Vcc rail at both high and low frequencies.
Note 5 : Choose appropriate loop filter components
Note 6 : Decouple unused output ports
Note 7 : Ground unused input ports
Note 8 : When the varactor line disable (OS bit) is set, the 30V supply can be varied to directly control the analog voltage to the varactor.

Fig.6 Typical I²C Synthesiser application

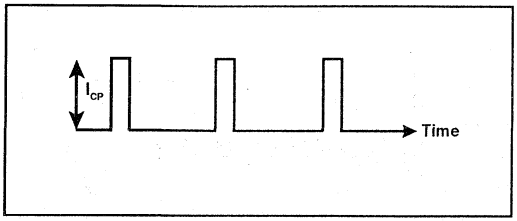


Fig.7 Phase detector current pulses

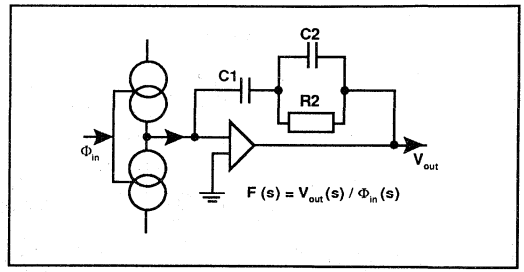


Fig.8 (a) Phase detector and charge pump - third order type 2 loop

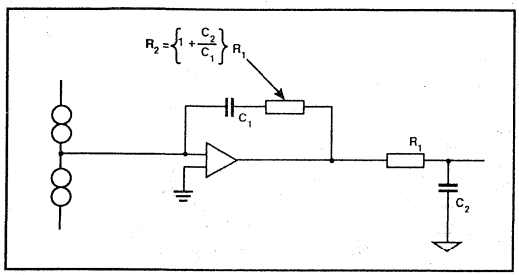


Fig.8 (c) Exact equivalent of Fig.8(a)
(Practical alternative to Fig.8(a))

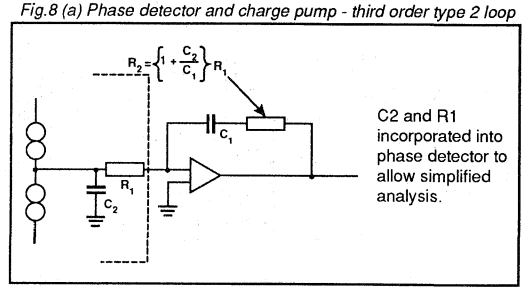


Fig.8 (b) Exact equivalent of Fig.8(a)

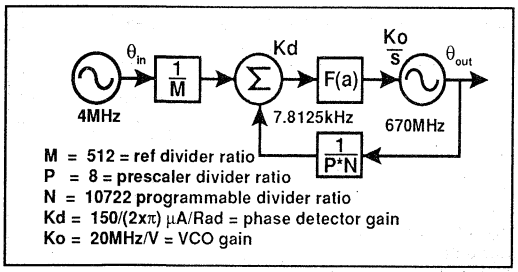


Fig.9 System block diagram

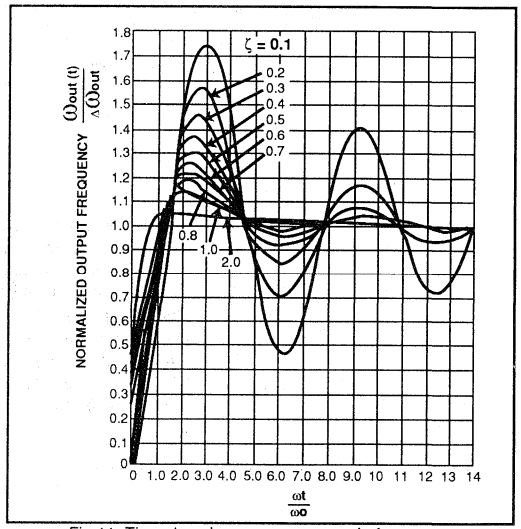


Fig.11 Time domain response to step in frequency

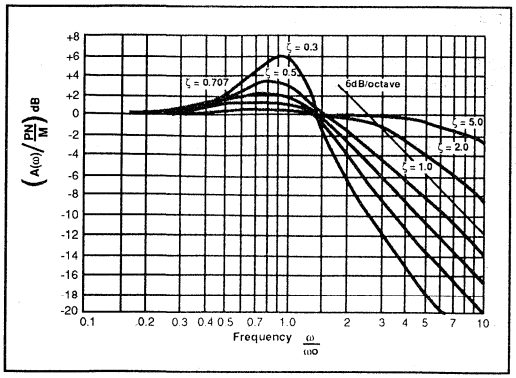


Fig.10 Frequency response of a high gain second order loop

Example (Selection of ω_o and ζ)

Assume the reprogramming causes a frequency step of 512 MHz and we wish the VCO to settle to an accuracy of 5.12 Hz within 100 mS. If the phase margin is 70° then the values for ζ and ω_o are:-

$$\zeta = \frac{\tan\emptyset}{2\sqrt{(1+\tan^2\emptyset)}} \quad \frac{= \tan 70°}{2\sqrt{(1+\tan^2 70°)}} = 0.8$$

$$\omega_n = \frac{-\text{Ln}\left[\frac{\omega_e}{\Delta\omega_{out}}\sqrt{1-\zeta^2}\right]}{\zeta ts} = \frac{-\text{Ln}\left[\frac{5.12}{512\times10^6}\sqrt{1-0.8^2}\right]}{0.8 \times 0.1}$$

$\therefore \omega_n$ = 237 rads/sec = 37Hz

Design Formulae

Using the known values of ω_o and ζ we have :-

$$C_1 = \frac{KdKo}{PN\omega_o^2}$$

$$R_2 = \frac{2\zeta}{\omega_o C_1}$$

$$C_2 = C_1/5$$

Example (Selections of C_1, C_2 and R_2)

Suppose Kd = 150μA/2π μA/rad y, K_o = 20 MHz/volt, P = 8, N = 10,722 whilst ω_o = 440 rads/sec and ζ = 0.87.

$$\therefore \quad C1 = \frac{150 \times 10^{-6} \times 20 \times 10^6 \times 2\pi}{8 \times 10722 \times 440^2 \times 2\pi} = 180.16\text{nF}$$

$$R2 = \frac{2 \times 0.87}{440 \times 180.6 \times 10^{-9}} = 21.9\text{K}\Omega$$

$$C2 = C_1/5 = 36.12\text{nF}$$

ω_o = 440 rads/sec = 70Hz.

PHASE NOISE CONSIDERATIONS

Noise Sources (See Figure 12)

The noise present at the VCO output originates from three main sources.

(a) Phase noise in the reference oscillator θ_r
(b) Phase noise in the detector θ_d
(c) Phase noise in the VCO θ_O.

A small sinusoidal frequency modulation of the reference oscillator for example, with peak phase deviation of θ_r radius and modulation frequency ω_m would produce an output voltage of :-

$$V_r(t) = V\cos(\omega_r t + \theta_r \sin \omega_m t)$$
$$= V\cos(\omega_r t) - \frac{V\theta_r}{2}\cos[(\omega_r+\omega_m)t] - \frac{V\theta_r}{2}\cos[(\omega_r-\omega_m)t]$$

See Figure 13. Many such sidebands will be contributed by random noise modulation mechanisms in the reference oscillator such as thermal and schott noise.

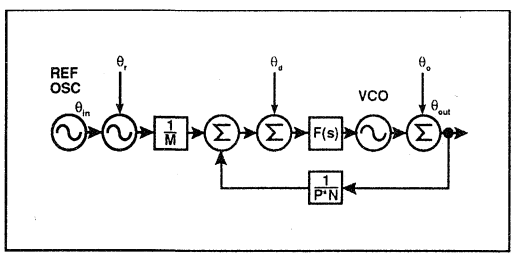


Fig.12 System diagram including phase noise

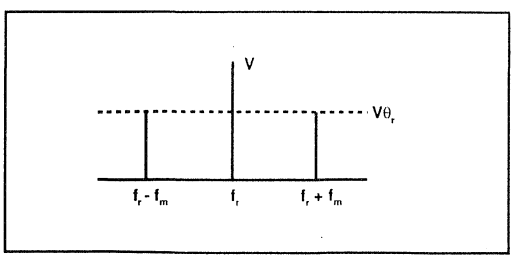


Fig.13 Noise sidebands

Noise at Synthesiser Output

The analysis of the System block diagram shows that the output noise spectrum is determined by :-

$$\theta_{out}(\omega) = A(\omega)\theta_r(\omega) + MA(\omega)\theta_d(\omega) + \left[\frac{1 - MA(\omega)}{PN}\right]\theta_O(\omega)$$

Where A(ω) is the system frequency response, described in Appendix 3 (system transfer charateristics) and shown in Figure 10.

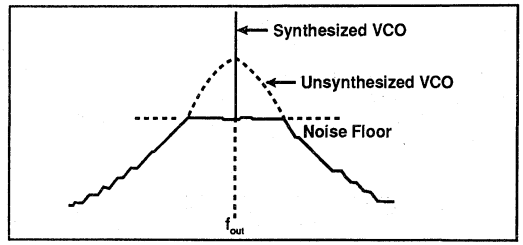


Fig.14 Output spectrum

Noise inside the Loop Bandwidth

The system frequency response inside the loop bandwidth is approximately given by :-

$$A(\omega) = \frac{PN}{M}$$

$\frac{PN}{M}$ This is just a statement that the system output frequency is times bigger than the reference frequency. As a result the noise at the output is :-

$$\theta_{out}(\omega) = \frac{PN}{M}\theta_r(\omega) + PN\,\theta_d(\omega)$$
INBAND

Notice that the phase noise due to the phase detector is M times bigger than the phase noise from the reference oscillator. Thus the phase detector noise dominates. This noise appears as a plateau on the spectrum analyser display as shown in Figure 14. The inband VCO noise meanwhile has been suppressed by the loop filter. Thus the inband output noise is determined by the prescaler and programmable divider ratios and by the noise floor of the detector.

$$\theta_{outINBAND} = PN\,\theta_d(\omega)$$

Noise outside the Loop Bandwidth

The output noise outside the loop bandwidth is approximately given by :-

$$\theta_{outOUTBAND} = \theta_O(\omega)$$

This shows that any noise components due to the VCO having frequencies outside the loop bandwidth are <u>not</u> suppressed. Thus the phase noise outside of the loop bandwidth is determined largely by the performance of the VCO itself and no improvement of this can be gained by the use of the synthesiser. See Figure 14.

Example (Low Comparison Frequency Synthesiser)

A synthesiser such as the SP5510 operates with a comparison frequency of 7.8125 KHz. If an LO of 512 MHz is to be synthesised then :-

$$PN = \frac{512 \times 10^6}{7.8125 \times 10^3} = 65536$$

In practice, since the phase detector noise floor predominates, the reference oscillator noise may be ignored. If the phase detector noise floor is -130 dBc then the noise floor at the output is given by :-

θ_{out} = -130dBc + 20 log 65536 = -130 + 96.3 = -33.7dBC

Example (High Comparison Frequency Synthesiser)

The SP5058 has been designed to operate, with a high comparison frequency, typically 250 KHz. If an LO of 2.048 GHz is to be synthesised then :-

$$PN = \frac{2.048 \times 10^9}{250 \times 10^3} = 8192$$

If the phase detector noise floor is -140 dBc then the noise floor of the output is :-

θ_{out} = -140dBc + 20 log 8192 = -140 + 78.3 = -61.7dBC

High comparison frequency synthesisers are used in applications where the phase noise within the loop bandwidth is an important consideration such as scrambled satellite or cable systems using the double conversion principle. See Figure 15 (shown below).

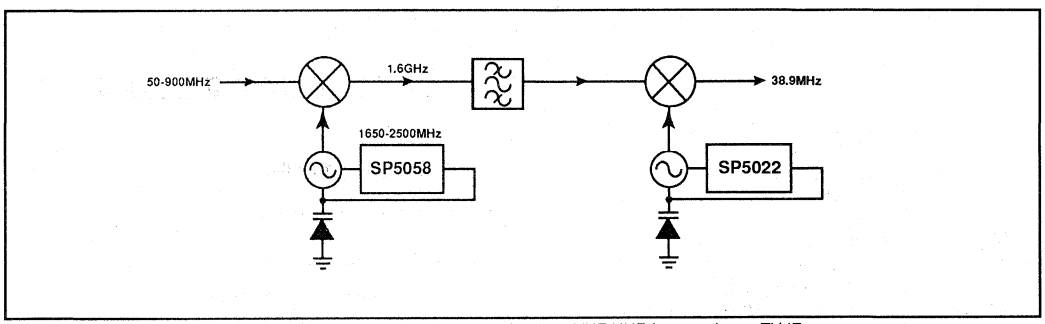


Fig.15 Example of double conversion from VHF/UHF frequencies to TV IF

USE OF VARACTOR LINE DISABLE (OS BIT) IN TUNER ALIGNMENT

In tuner manufacture, many of the wound components must be aligned to give the desired tilt factors, filter matching and correcting range for local oscillators and IF output.

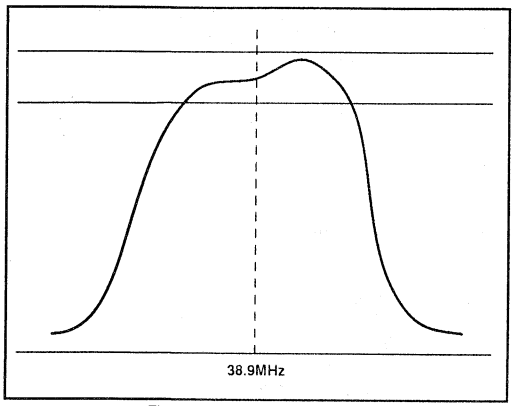


Fig.16 Alignment of IF output

This is a time-consuming process and is usually carried out by tuning the synthesiser to a number of different channels and aligning to these points (shown • on Fig.17).

Each time a new channel is selected, data must first be written to the synthesiser. In this example, 6 sets of data must be sent from the micro to the synthesiser.

However, if the varactor line disable bit OS is used, the varactor line voltage can be externally controlled. This allows the selected channels to be tuned without the use of a micro to address and program the device.

The varactor line disable facility is available on all GPS I²C bus synthesisers and also on I²C bus compatible 3-wire synthesisers such as the SP5024 and SP5054. With the latter devices, the varactor drive is disabled by applying a negative voltage to the ENABLE pin (pin 10) and sourcing greater than 350µA from the device. using this method of tuning can result in appreciable saving of test time.

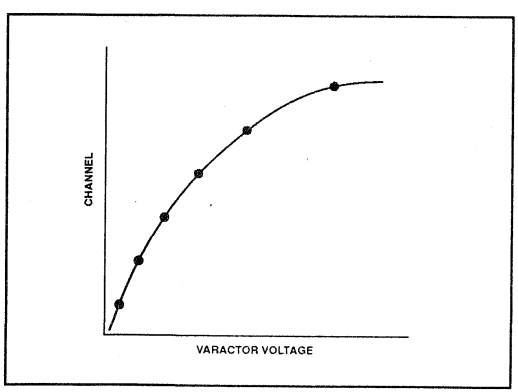


Fig.17 Varactor tuning curve

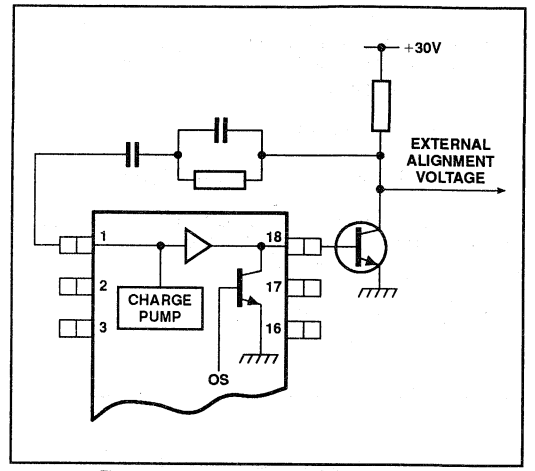


Fig.18 Application of external tuning voltage

APPENDIX 1 (NOTATION)

Description of symbols used.

$\theta_{out}(s)$ = VCO output phase

$\theta_{in}(s)$ = Reference oscillator phase

$\omega_{out}(s)$ = VCO output frequency

$\omega_{in}(s)$ = Reference oscillator frequency

K_O = VCO gain in rads/sec/volt

K_d = Phase detector gain = $\frac{Icp}{2\pi}$ Amps/rad

M = Reference divider ratio

P = Prescaler divider ratio

N = Programmable divider ratio

ω_O = Natural frequency of 2nd order system in rads/sec

ζ = Damping factor of 2nd order system

S = Laplace frequency variable

$\underline{S}$ = S/ω_O = Normalised laplace frequency variable

$\underline{\omega}$ = ω/ω_O = Normalised frequency

APPENDIX 2 (SYSTEM EQUATIONS)

System Transfer Characteristics (See Figure 9)

$$G(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{\omega_{out}(s)}{\omega_{in}(s)} = \frac{K_O K_d(s)/Ms}{1 + K_O K_d(s)/PNs}$$

Open Loop Gain

$$G_{OL}(s) = K_O K_d F(s)/PNs$$

APPENDIX 3 (2ND ORDER TYPE 2 SYSTEM)

System Transfer Characteristics

$$G(s) = \frac{PN}{M}\left[\frac{1 + 2\underline{s}}{\underline{s}^2 + 2\zeta\underline{s} + 1}\right]$$

Where:-
Normalised Laplace variable is

$$\underline{s} = s/\omega_o$$

Natural Frequency is

$$\omega_o = \sqrt{\frac{K_d K_o}{PN\mathcal{T}_1}}$$

Damping Factor is

$$\zeta = \omega_o\mathcal{T}_2/2$$

$$\mathcal{T}_1 = C_1$$

$$\mathcal{T}_2 = \left[1 + \frac{C_2}{C_1}\right] R_1C_1$$

System Frequency Response (See Figure 11)

Amplitude

$$A(\omega) = \frac{\sqrt{1+(2\zeta\underline{\omega})^2}}{\sqrt{(1-\underline{\omega}^2)+(\zeta\underline{\omega})^2}}$$

Phase

$$\varnothing(\omega) = \text{atan}(2\zeta\underline{\omega}) - \text{atan}\left(\frac{\zeta\underline{\omega}}{1-\underline{\omega}^2}\right)$$

Time Domain Response (See Figure 12)

$$\omega_{out}(t) = \Delta\omega_{out}\left[1 - \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}}\left(\cos\sqrt{1-\zeta^2}\,\omega_n - \frac{\zeta \sin\sqrt{1-\zeta^2}\,\omega_n}{\sqrt{1-\zeta^2}}\right)\right]$$

$\omega_{out}(t)$ = output frequency at time t.
$\Delta\omega_{out}$ = output frequency step caused by reprogramming the divider

Settling Time

$$ts = \frac{-\text{Ln}\left[\frac{\omega_e}{\Delta\omega_{out}}\sqrt{1-\zeta^2}\right]}{\omega n\zeta}$$

Where $\omega_e = \Delta\omega_{out} - \Delta\omega_{out}(ts)$ radians/sec
is the error in the output frequency at time ts following a step adjustment of the output frequency of $\Delta\omega$.

Open Loop Gain

$$G_{OL}(s) = \frac{1 + 2\zeta\underline{s}}{\underline{s}^2}$$

Open Loop Frequency Responses

amplitude

$$A_{OL}(\omega) = \frac{\sqrt{1 + 2\zeta\underline{\omega}^2}}{\underline{\omega}^2} \qquad \text{Where } \underline{\omega} = \frac{\omega}{\omega_0}$$

phase

$$\varnothing_{OL}(\omega) = -\pi + \text{atan}(2\zeta\omega)$$

Phase Margin

$\varnothing_1 = \text{atan}(2\zeta\underline{\omega})$
where unity gain frequency $\omega_1 = \sqrt{2\zeta^2 + \sqrt{4\zeta^4+1}}$

$$\therefore\zeta = \frac{\tan\varnothing_1}{2\sqrt{(1+\tan\varnothing_1)}}$$

AN OVERVIEW OF THE H.261 VIDEO COMPRESSION STANDARD AND ITS IMPLEMENTATION IN THE GPS CHIPSET

THE REQUIREMENT

H.261 is an ITU recommendation concerned with providing an international standard for video codecs which will allow inter regional compatibility for video telephony. The recommendation covers the bitstream contents and the accuracy of the decoder, but leaves room for differentiation in the encoder and pre/post processing. It also allows users with either PAL, NTSC, or SECAM local cameras and monitors to communicate freely without knowing the TV standards of the remote participant. It was also concerned in specifying a compression method which could economically be mechanized at real time camera rates. This implies that the processing requirements for coding and decoding should not be vastly different, as is the case with the MPEG standard.

The Integrated Services Digital Network (ISDN) provides the means of communication, and thus compressed video bandwidths are based on increments of 64 Kbits/second. The basic rate ISDN interface provides two 64 Kbits/second information (B) channels and the primary rate interface (PRI) in Europe provides scope for 30 B channels. H.261 thus describes video coding and decoding methods at rates of p x 64 Kbits/second, where p is in the range of 1 to 30. For this reason the specification is often known as the px64 compression method.

Once a call has been established the transmission must continue at a fixed bitrate regardless of the level of activity within the picture. Since movement within a picture generally results in more bits being generated for that picture, then quality usually has to suffer in some way in order to keep the bitrate constant. This is in spite of system level buffering to smooth out the peaks and troughs in the bitrate. The use of broadband ISDN technology (B-ISDN), with its use of asynchronous transfer mode (ATM), would remove this restriction. The basic compression standard would not be affected, but the variable bitrate available with ATM allows the picture quality to remain constant when movement occurs. There may still be an upper bound to the bitrate, but only above this limit will quality start to suffer.

H.261 only covers the video side of a video phone system. Audio can use any of the adopted standards but typically would be either G.722 wideband coding at 48/56/64 Kbits/second or G.728 narrowband coding at 16 Kbits/second. The combined video and audio bitrate must comply with the number of information (B) channels provided at a given time. Thus in a basic rate system providing 2 B channels, and which uses G.728 audio coding, only 112 Kbits/second would be available for the video path.

Several other standards exist to cover a complete narrowband video telephony system. The complete top level specification is covered by H 320; H.221 covers the framing structure for the multiplexing of H.261 video, audio, data and signalling; H.242 covers the communication procedure (call set up, capability exchange, etc.); and H.230 covers control and identification signals.

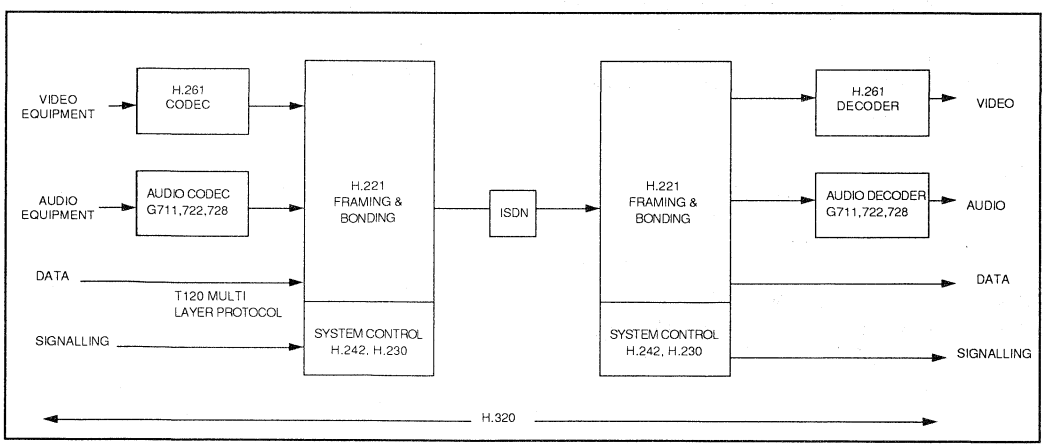


Fig.1 Video Phone Architecture Specified by H.320

THE PROBLEM

Studio quality PAL requires 720 luminance pixels per line and 576 active lines at 25 frames per second. Chrominance pixels can have half the horizontal resolution of luminance pixels without any perceived loss in quality; this results in 4:2:2 video with each of the 720 x 576 pixel positions requiring a 16 bit word to represent an 8 bit luminance component plus one of the 8 bit chrominance components. All this equates to the need for bitrates of around 166 M bits/second for studio quality video.

Videophones do not, of course, have to transmit studio quality video, and in fact a subjective quality of that achieved by domestic video recorders would be perfectly adequate. For this reason a Common Intermediate Format (CIF) was defined which in many ways was a political compromise between Europe and USA/Japan. It had the line rate of PAL/SECAM and the frame rate of NTSC, and is defined to have a luminance resolution of 352 x 288 lines with an update rate of 30 frames per second. Chrominance resolution is half that of the luminance in both the horizontal and vertical directions i.e. it has a resolution of 176 x 144 lines. These resolutions result in a bandwidth requirement of 31 Mbits/second to transmit uncompressed CIF frames at 30 Hz rates.

The problem then is to reduce this 31 Mb/s rate down to one within the range defined by H.261. Thus at the top end of the range a compression ratio of around 16:1 is needed, but for a 64 Kb/s line a compression ratio of 480:1 is required.

When the received picture is only to be displayed in a small window on a PC monitor, it is possible to get acceptable quality with lower spatial resolution. A quarter CIF (QCIF) standard was thus defined which is half the luminance and chrominance resolution in both the vertical and horizontal directions. This requires one quarter of the compression ratios given above, but is normally only used in low bitrate applications.

Since video phone systems still use conventional PAL or NTSC cameras, and off the shelf digital composite video decoders, it is necessary to use digital filters when decimating down to CIF or QCIF resolutions. Simply discarding alternate pixels produces unacceptable aliasing effects which soon annoy the user. There is a problem in producing a CIF frame from an NTSC source which is usually glossed over by people offering single chip or software solutions to H.261 compression. PAL is relatively easy since one of the fields out of an interlaced pair provides the correct number of luminance lines. Simple low pass filtering is then needed to reduce the bandwidth to match the required horizontal resolution. With NTSC, however, a single field only produces 240 active lines and polyphase interpolating vertical filters are needed to get acceptable quality. These require six sets of coefficients to produce six CIF luminance lines for every 5 NTSC lines.

THE COMPRESSION SOLUTION AND ITS EMBODIMENT IN THE GPS CHIPSET

One fairly obvious way of reducing the amount of data needed to transmit a sequence of related frames is to code only the differences between frames. This is known as inter frame coding as opposed to intra frame coding which codes each frame in isolation. It is particularly useful for a video phone comprising a head and shoulders view of a talking person. Only the lips move plus a slight movement of the head between frames. Even so these movements plus camera noise and lighting effects can still cause significant frame to frame differences.

The first step is thus to minimize the secondary effects (caused by camera noise etc.) and then to recognize that movement has occurred. It is then possible to code vectors defining the movement of blocks of pixels rather than re-coding the complete frame every time. Both these steps are considered enhancements to the H.261 specification, although the decoder must be capable of using the coded motion vectors when they are transmitted.

The secondary frame to frame differences can be minimized by a combination of spatial low pass filtering and temporal filtering. The latter produces an average of the present and previously captured camera frame which is dependent on the difference between individual pixels in each of those frames. Thus if the difference is small the previous pixel is used and if it is large the new pixel is used. In between large and small some fraction of the actual difference is added to the previous pixel to produce a new pixel which is closer to the previous pixel than it would have been. The fraction applied varies in a non linear way, and above some difference threshold the new pixel is always used i.e. the whole difference is added to the previous pixel.

In the present GPS chipset the spatial noise filtering is done with the VP520. Decimation down to CIF or QCIF is done at the same time. It uses 8 tap horizontal filters and 5 tap vertical filters for producing CIF, and 16 tap horizontal and 7 tap vertical filters for producing QCIF. It also provides the six phase filters previously identified as being needed to produce 288 CIF lines from a 240 line NTSC field. Temporal filtering is presently not implemented but will be featured in the next generation solution.

Movement can only be estimated by considering manageable blocks of pixels. The assumption then being that all pixels in that block move in the same direction. The pixels must thus be strongly correlated. For simplicity only luminance pixels are used, and the difference between pixels in the present and the previous block is calculated by summing the absolute differences between each pair of pixels. The block of pixels is then moved around in a search area the dimensions of which represent the maximum value of the motion vectors to be produced. The difference summation is done at each pixel position in the search window, and the position with the minimum sum of differences defines the best fit.

The size of the luminance block used to detect movement is defined to be 16 x 16 pixels in the H.261 specification. The maximum search displacement is ±15 from the centre position, giving a total search window size of 46 x 46 pixels. Even though the position of the best fit has been found there will still be errors between individual pixels in the 16 x 16 block. These errors are coded but, as will be shown later, still represent a bitrate saving over simply re-coding every new frame as it occurs. If the error in the best fit position is outside a threshold then motion compensation is aborted, and the new block is coded without reference to the previous frame.

The H.261 specification does not demand that the encoder uses motion compensation, only that the decoder can use any transmitted vectors plus the errors. An encoder without such facilities would, of course, produce worse quality video for a given bitrate. The VP2611 Encoder incorporates a motion estimator but displacement vectors are limited to ±7 pixels i.e. the search window is limited to 23 x 23 pixels. This

was considered adequate in its intended traditional video conferencing environment, where the camera is a long way from the speakers and little movement occurs at 30 Hz frame rates. In a PC based video phone, however, the camera is only a couple of feet from the user and lower frame rates are used. Much more movement is then possible between frames and the full ±15 search area would be advantageous in reducing bitrates. This is being addressed in the next generation design.

The calculations required to find the best fit, using an exhaustive search of all the positions that a 16 x 16 block can occupy over a ±15 range, amount to approximately 256 thousand 8 bit differences and 256 thousand 16 bit accumulations. In a CIF frame there are 396 such blocks, and at a 30 Hz frame rate the calculation must be done in about 75 microseconds. This is equivalent to a computation rate of approximately 6.5 giga operations per second (GOPS). Several algorithms have been put forward in an attempt to reduce the computation rate, but with all it is possible to never find the optimum fit. It should be noted that since the errors between previous and present blocks are always coded then not finding the best fit does not actually cause any corruption of the picture. It simply means that a higher bitrate is produced when coding that part of the picture, which does however mean that lower quality is obtained for a fixed average bitrate.

A two step algorithm has been developed for the new VP600 Encoder which has been shown to give good performance with a standard set of test sequences. In the first pass a fit is calculated at every third pixel position in both the horizontal and vertical directions. In the second pass a search is done using the twenty four positions round the first pass best fit. This reduces the computation rate to less than one GOP, and is implemented with 20 eight bit subtractors and 20 sixteen bit accumulators. With a 54 MHz clock rate these allow 30 Hz frame rates to be achieved.

TRANSFORM CODING AND QUANTIZATION

To achieve the high compression rates needed in a video phone system it is necessary to use transform coding plus lossy compression techniques i.e. the reconstructed image will contain errors when compared to the original image. This in turn requires that the encoder keeps a copy of the image which has been encoded and then decoded when inter frame coding is to be implemented. This re-constructed image is then used to calculate frame to frame differences.

Transform coding is a way of compressing the energy present in a two dimensional array of pixels such that most of the information contained in the original number of spatial pixels is reduced to a smaller number of transform coefficients. An array of closely correlated pixels is converted to one of de-correlated coefficients, and redundancy is removed. Once these coefficients have been calculated the bits used to represent each value can be reduced by a division process (quantization) and most of the smaller values should then go to zeros. At this point the compression method becomes lossy since it is impossible to re-construct the original image.

In the H.261 specification the Direct Cosine Transform (DCT) was chosen to do the energy compression. Although other transforms are more optimal the DCT was chosen since it is relatively easy to implement at video scan rates and does not use complex numbers. To the non mathematical user it has the advantage that the coefficients can be likened to frequency components, since the DCT can be compared to the real part of an FFT calculation. Thus conceptually the transform and quantization process is simply converting from the spatial to the frequency domain and then filtering out the higher frequencies. The eye is known to be less sensitive to the higher frequencies in a video frame, and thus they can be removed without the effect being too visible. A visualisation of the mathematical transform process is thus possible.

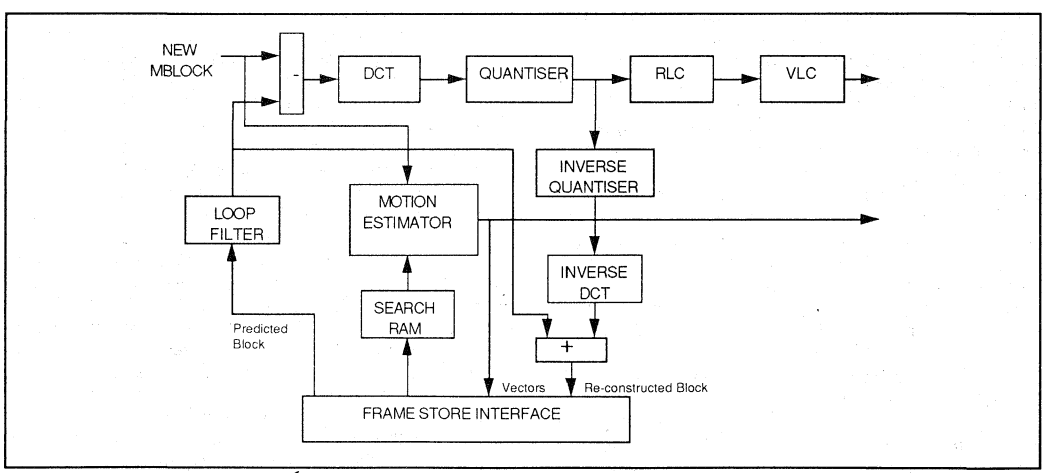


Fig.2 H.261 Coding Kernel

The pixel array size was chosen to be 8 x 8, and was a compromise between the computation power needed to calculate the DCT and selecting the largest possible group of correlated pixels. Earlier proprietary standards had chosen a 16 x 16 block as being optimal, but beyond this pixels are not as well correlated in a typical picture. The actual accuracy of the DCT calculation is not specified, but the error tolerance in the output of the Inverse DCT is well defined. The DCT is performed either on absolute pixels or signed pixel differences if inter frame coding is being performed. The latter are represented by 9 bit two's complement numbers in the VP2611 Encoder, and a sign bit is added to the 8 bit unsigned absolute pixel value. A 12 bit two's complement number is obtained form the DCT circuit and this is then quantized.

The quantization value is defined by the H.261 specification to be an even number in the range 2 to 62, it can thus be expressed as a 5 bit value in the coded bitstream. The 12 bit signed value is thus divided by a variable unsigned number, and then clipped to an 8 bit signed number. For quantization levels below 8 it is possible that clipping will occur with high coefficient values from the DCT.

The actual quantization value is determined by the system operating conditions. Since the number of bits generated for a frame depends on the amount of movement since the last frame, it is necessary to have a buffer at the output of the system. This attempts to smooth out the peaks and troughs and will be loaded at a variable rate but read at a fixed rate determined by the chosen constant line rate. When this buffer starts to fill the system reacts by increasing the quantization level in an attempt to produce more zero coefficients out of the quantizer. As the buffer gets even fuller the system is allowed to completely skip coded blocks and ultimately complete frames.

Since the clipped output from the quantizer is expected to contain a large amount of zero's, run length coding can be used to reduce the number of bits needed to represent the coefficients. This is made more effective if the coefficients are first re-arranged in ascending frequency order since we expect that the higher frequencies values will have disappeared. This is known as zig zag scan order.

For every original array of 8 x 8 pixels we have now obtained 64 quantized coefficients expressed as runs of zero's and actual values. We normally only expect three or four actual values to remain, and several combinations of runs and coefficients have a higher probability of occurring. There is thus something to be gained by using variable length coding, and the codes to be used are defined in the H.261 specification. Motion vectors are also variable length coded.

H.261 STRUCTURE

We have established that H.261 video coding is based on quantizing the output of a DCT which is done on an array of 8 x 8 pixels. Inter frame coding is supported in which the DCT is done on pixel differences, and the performance can be further improved by optionally applying motion compensation. The output is a series of run length coded coefficients which can be variable length coded in commonly occurring sequences. This data must then be combined with any motion vectors, and also with information amount the coded blocks such as quantization values and whether they were inter or intra coded. A serial bitstream must then be produced.

It is beyond the scope of this paper to fully define the H.261 bitstream but essentially the 8 x 8 basic DCT blocks (sub blocks) are firstly combined into macroblocks. These consist of four luminance sub blocks plus two chrominance sub blocks (one for each component). Remember that the definition of CIF called for chrominance to be half the resolution of luminance in both directions. A chrominance sub block thus corresponds to the same spatial screen area as four luminance sub blocks. These four luminance sub blocks are considered as one 16 x 16 entity when motion estimation is calculated.

Each macroblock is given a relative address since macroblocks can be skipped if they contain no coded inter mode data (fixed backgrounds) or they can be forcibly skipped to keep the generation of bits under control (the decoder then uses the same macroblock in the last received frame and hopes it is relevant). A macroblock header defines its quantization value if this has changed from the last macroblock, plus whether it was inter or intra coded and whether it was motion compensated etc.

Macroblocks are then combined into 11 x 3 groups (GOBS) and finally a picture header is added. For a CIF picture there are 12 GOBS and for a QCIF picture there are 3 GOBS. All headers are unique sequences of bits and cannot be produced by the data coding scheme.

The serial bitstream contains all this information plus the actual coded data. This is divided into frames of 512 bits which should not be confused with original video frames. The 512 bits consist of 492 bits of the above data; plus 18 parity bits for error correction; plus one bit of framing code which allows synchronization of the decoder; plus a fill bit which indicates whether the data is valid or whether the transmission buffer was empty and the system is just keeping the line busy. The parity bits allow one or two bit errors to be corrected within that particular frame, and the framing code is 8 bits long in total. The decoder initially searches for this framing code by examining 8 bits which are 512 apart in the received bitstream. Once the code has been detected it must be repeated three times to ensure that it was not found by chance in the data. Having obtained frame lock the receiver then knows the position of the fill bit and the error correction bits. It can then do any error correction and finally search for unique picture start codes. Once a picture start code has been found the decoder can progress through the various layers and finally decode the run length coded coefficients using the inverse DCT transform.

IMPLEMENTATION WITH THE GPS CHIPSET

The encode path, from CCIR601 video data out of a composite video decoder through to an error corrected H.261 bitstream, takes three devices in the present GPS one micron solution. The VP520 contains all the vertical and horizontal filters necessary to produce CIF or QCIF macroblock data from both PAL and NTSC line video.

The VP2611 contains the complete coding kernel comprising of the ±7 motion estimator; the loop filter defined in the specification; the inter/intra decision processor; the DCT and quantizer; and finally zig zag re-ordering and run length coding. It also contains a complete reverse path so that quantized coefficients can be inverse quantized and passed through an inverse DCT in the same manner as one at the far end. This re-constructed data is then written to an external DRAM frame store and used in inter frame coding.

The VP2612 takes the run length coded coefficients and motion vectors from the VP2611 and does variable length coding. These are then written to an external transmit buffer, and read out at the required line rate. The H.261 header information, framing structure, and error correction bits are then added to produce an H.261 compliant bitstream.

The quantization is not done by dedicated hardware, but all the information for an external software algorithm is provided on a host controller bus. This allows each user to add differentiation to their product, since experienced providers of video conferencing system have their own proprietary algorithms.

Three devices provide the reverse operations in the decoder. The VP2614 De-Multiplexer needs the support of an external 32K x 8 static RAM. It searches for H.261 frame lock and then does error correction. Picture start codes are then identified and variable length decoding takes place. A state machine interprets the H.261 coding structure and produces run length coded coefficients for the VP2615 Decoder. The VP2615 then completes the decoding operation and performs the inverse DCT operation. It fetches the previous block from an external DRAM if inter frame coding was specified. The output of the VP2615 consists of macroblocks of pixel data which are supplied as inputs to the VP520. This device has both encode and decode modes of operation; in the decode mode it interpolates the CIF or QCIF data up to normal CCIR601 resolutions. Two sets of vertical filter coefficients allow interlaced fields to be produced.

This chipset is now in production and the next generation system is now being designed. This comprises two devices; the VP600 contains all the present functionality of the VP520, VP2611, and VP2612 and only requires a single external DRAM rather than two DRAM's and an SRAM. Likewise the VP610 contains all the functionality of the VP2614, VP2615, and VP520 in decode mode. It also only requires a single external DRAM rather than three RAM's as at present.

The new devices are specifically aimed at single board PC videophone designs, rather than it raditional video conferencing systems. They thus contain system level enhancements aimed at meeting the needs of multimedia PC's and offer increased performance with a ±15 search window and temporal filtering.

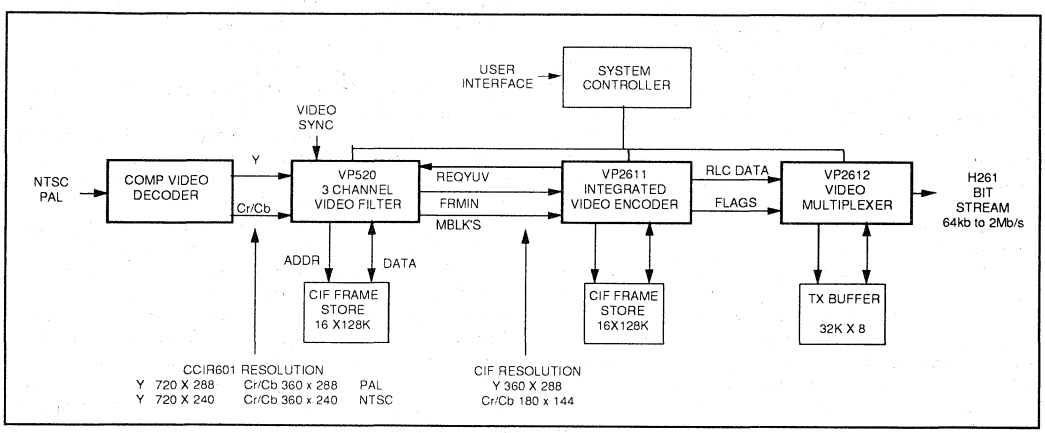


Fig.3 Complete H.261 Encoder Using the GPS Chipset

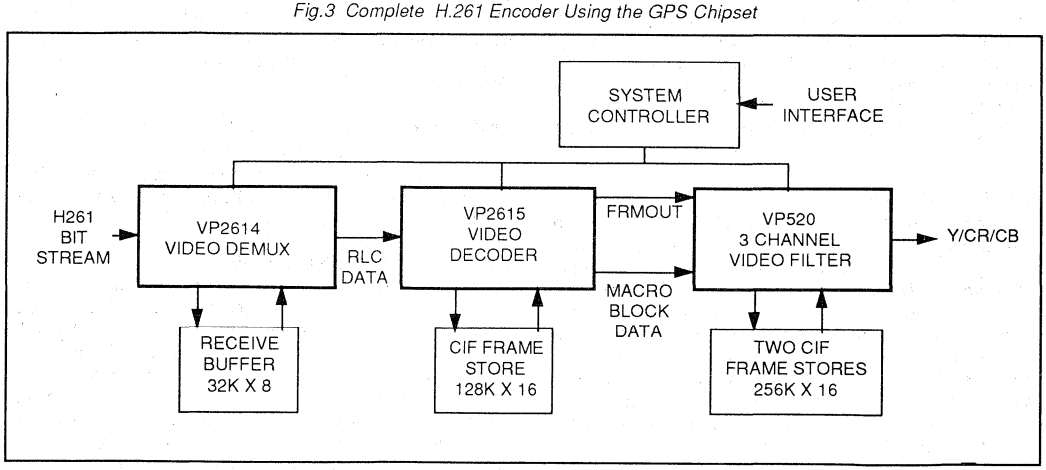


Fig.4 Complete H.261 Decoder Using the GPS Chipset

MV1817 APPLICATIONS

PACKET 31 RECOVERY

Introduction

MV1817 can be used for packet 31 data recovery simultaneously with normal page reception via the two page acquisition circuits, and in addition to packet 8/30 and packet 29 reception.

In MV1817, there are eight acquisition circuits dedicated to packet 31 reception, one for each of the eight magazines in which packet 31 data could be transmitted.

Because these packets might be transmitted at a very high rate (potentially) much faster than data could be read from the normal memory via the I^2C bus), the received data from each of the packets is written to a single memory location, so that simple external hardware can be used to assemble the memory data nibbles into bytes, and then write the bytes sequentially to a suitable buffer. The output data from this buffer can be read by a computer or other system with appropriate decoding software.

The relevant address for packet 31s from each magazine are shown in Table 1. they are all in store 00.

Magazine	EBU Channel	Hex Byte Address	RAS Address	CAS Address
0	8	10	002	000/1
1	9	11	002	002/3
2	A	12	002	004/5
3	B	13	002	006/7
4	C	14	002	008/9
5	D	15	002	00A/B
6	E	16	002	00C/D
7	F	17	002	00E/F

Table 1. Address for the eight acquisition channels

Description of the MV1817 DRAM signals

Fig. 1 shows the basic signals from MV1817 that are used to control the external hardware. Data bytes are written to the DRAM as two four bit nibbles using standard page mode signals. A normal memory cycle has a $\overline{RAS}$ pulse and two $\overline{CAS}$ pulses to read/write the eight data bits.

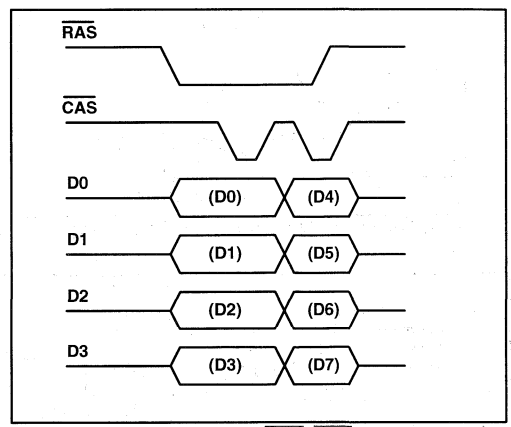


Fig. 1. DRAM signals $\overline{RAS}$, $\overline{CAS}$ and Data

Description of the Packet 31 recovery circuits

The logic proposed in this Application brief is intended as a preliminary guide to what would be needed in a real application. The circuits shown have not been tested and no guarantees are given as to their suitability for any particular application,

It is important that logic circuits to work with MV1817 are based on an advanced CMOS logic family, as some signals described in this brief can have separations of as little as 9ns. The D-types in particular therefore need set up times for the data input with respect to the clock, of better than about 6ns (dependent on logic delays)

The FIFO buffer shown is a generic 64 x 9 type. The speed rating for this device will probably be dependent on the output data rate required, since the input rate is relatively low, being at maximum the standard teletext byte data rate of 867 · 1875 kbytes/sec. Other FIFO devices such as 2048 x 9 should be equally suitable, and may make the system design easier.

With reference to Fig. 2 and 3, the leading edge of $\overline{RAS}$, and the four edges, A, B, C, and D on $\overline{CAS}$, are used to control the latching of data from D<0:3>, addresses from A<0:9> and the latching/clocking of data into/through a FIFO buffer.

A D-type is used to latch the state of the address lines at the leading (falling) edge of $\overline{RAS}$. If they are all low except A1, a logic 1 is held on the $\overline{Q}$ output. Edges B and D (Fig. 2) are used to clock the state of $\overline{RAS}$ through a second D-type to produce 'RC1', while a third D-type uses edges A and C to latch the state of 'RC1', generating 'RC2'.

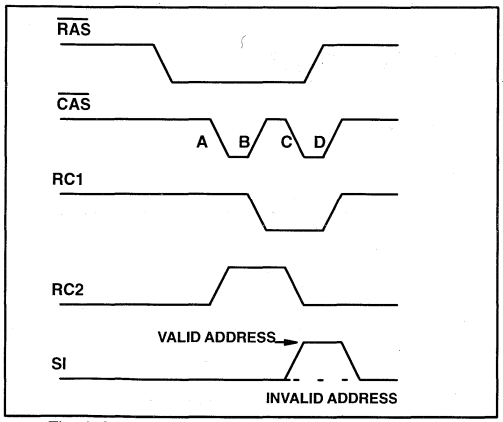


Fig. 2.Generation of SI pulse from DRAM signals.

If address lines A4 through A9 are also low during the CAS cycles, an active low signal VALID ADDRESS is produced. When NORed together with VALID ADDRESS, RC1 and RC2 produce the conditional 'SI' pulse which loads data into the FIFO on its leading (rising) edge, and clocks it through the FIFO on the trailing (falling) edge. A quad D-type (74AC175) is used to latch the first data nibble using edge 'B' of the CAS signal. This allows the whole data byte (D<0:7>) to be presented to the FIFO inputs at the rising edge of SI.

Address decoding

As detailed in Fig. 3, the address decoding from A<0:9> during RAS and CAS, will write packet 31s from any one of the eight addresses 10 - $17_{hex.}$ into the FIFO.

These addresses correspond to magazines 0 - 7 respectively. If data from only one magazine is required, address lines A3, A2 and A1 need to be appropriately decoded during CAS, and the decode ANDed with the other parts of the CAS address.

With the circuit as shown, the magazine number for any particular byte(s) of data can be latched during either CAS cycle from A<3, 2, 1> and presented to the microprocessor via separate logic.

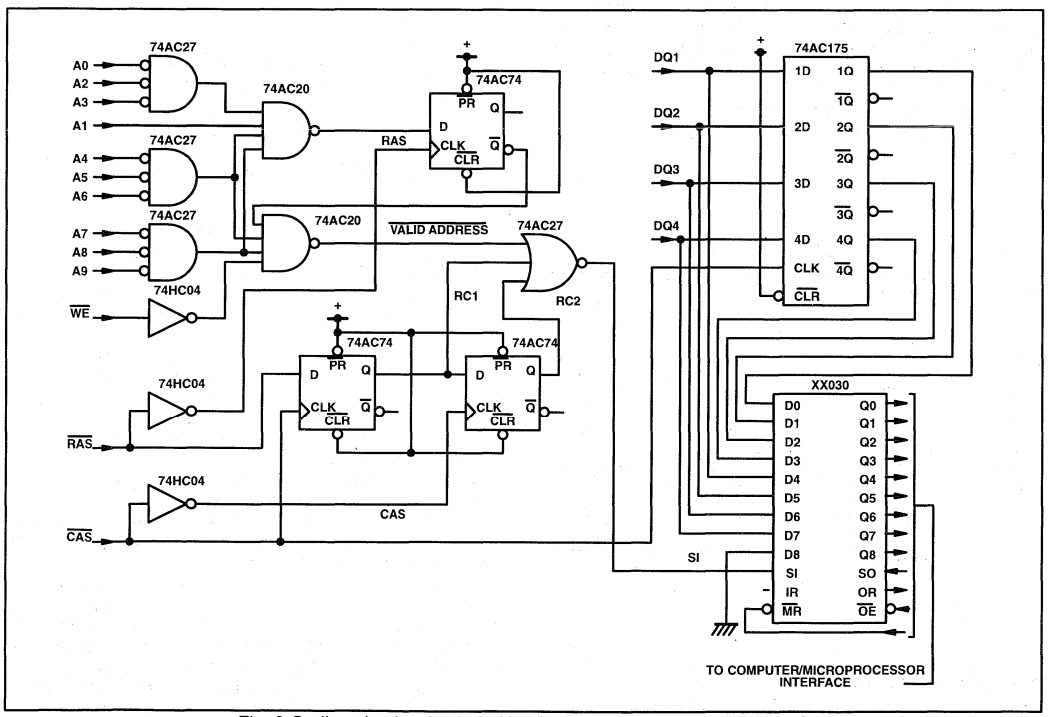


Fig. 3 Outline circuit to latch and load packet 31 Data Bytes into FIFO

Further information

Detailed timing information for the DRAM signals is available in the Datasheet. Reference should be made to these figures to ensure that adequate timing margins are allowed.

Note

This Application Brief also applies to MV1816/18/19.

THE VPS/PDC RECORDING FUNCTION

OUTLINE RECOMMENDATIONS FOR SOFTWARE IN VCRs USING THE MV1820 FAMILY

1. LABEL MATCHING

a. How Many Labels?

The PDC data in Format 2 packet 8-30s, is protected against errors by 8/4 Hamming encoding. This protection allows for the correction of a one bit error in any of the words in the message. Detection of uncorrectable errors caused by two errors in one word, will cause the whole packet to be rejected. This protection usually ensures that a message is either received correctly or is abandoned without generating an interrupt or writing data to the I^2C registers.

However, for maximum reliability, we recommend that at least two matching labels should be read from MV1820/21, before any action is taken. For VPS labels, where the level of error protection is not as good as PDC, five consecutive matching labels are recommended (ARD/ZDF Technical Guideline 8-R2, part IV -101 9.1/9.2)

b. Label Content

The last two (VPS five) consecutive labels in any particular LCI (channel) should be identical, i.e. the same as each other. This means that the labels must all be the same in every byte. If any byte is different (but see section 4), even a byte that is not relevant to the particular application such as the sound status bits, then all but the last label should be discarded, and the checking re-started.

c. Consecutive Labels

Consecutive – following continuously – means the last two actual labels received by MV1820/21 in a particular channel, whether they are received at 40 millisecond intervals, 200 millisecond intervals, 1 second intervals, or even longer intervals.

2. VPS/PDC LABEL TRANSMISSION/RECEPTION RATES

a. Overview

VPS programme labels are transmitted in line 16 of every frame, therefore there are (under normal conditions) 25 per second. There is a restriction to a maximum of five packet 8-30s per second of either format.

Normally, packet 8-30 format 1 (8-30-1) which carries the time and date, is transmitted once per second just prior to the change of each second (but can be transmitted at a faster rate). This leaves reception space for up to four other packet 8-30s of a different format. These five time slots could legitimately have any combination of format 1 and format 2 packet 8-30s. For instance, all five could be format 1, or all five could even be format 2s with the same channel (LCI).

Designers should note that very poor reception conditions, or even erroneous transmissions, might cause the loss of a significant proportion of the packets at the receiver, resulting in a reception rate of only one packet every few seconds.

b. Timer/PDC Mode Switching

PDC software should not rely on receiving packet 8-30s at any particular rate, but should evaluate the contents of a packet with respect to the previous packet. Inevitably though, there will be a reception rate at which the software must decide that there are insufficient packets to rely upon for accurate timing. This rate is probably about one packet per LCI per ten seconds, since that would still allow three packets to be received during any 30 second period, and should therefore guarantee that the start of a programme would not be missed.

Reception rates of less than one per ten seconds should therefore cause the system to switch into timer mode. To avoid frequent switching between modes if reception is intermittent, it would be sensible to provide some hysteresis in the switching. Therefore to switch back to PDC control from timer mode, should require a better reception rate, such as one label per LCI per two seconds.

c. VPS Reception

VPS packets are transmitted at 25 per second, which is anything from 5 to 25 times faster than packet 8-30-2s. Similar rules for mode switching need to be applied when receiving VPS, except that because the packets are transmitted much faster, the rules need to be suitably adapted.

For mode switching, a suitable gap might be one second without any VPS labels to enter timer mode, and one or two good labels to re-enter VPS mode.

3. THE 30 SECOND RULE

a. Recording Start (see also 4.a)

The 30 second rule states that the broadcaster should start the labels for any particular programme about 30 seconds before the programme itself starts. This is to allow time for VCRs that might be channel scanning, to find and check the labels and then enter RECORD mode without missing any of the programme.

If a VCR is not scanning other channels, then it should see the very first label that matches. It could start a 30 second timer so that it actually starts recording exactly on the start of the programme, but because of the difficulty of making the timer correct when the VCR is scanning other channels, we recommend that:

as soon as two consecutive and identical labels have been received, recording should be started immediately, if the labels match the user defined label.

This may record slightly early if the VCR is not scanning

other channels, but this may be easier for the software than trying to guess when to start if it has missed the label change point for any reason.

b. Recording Stop (see also 4.b)

The 30 second rule means that if the labels for one programme start early, the labels for the previous programme may also finish 30 seconds early, therefore VCRs must not stop recording immediately after a label change.

When the VCR is recording, it cannot be scanning other channels, therefore it should receive the first label of the next programme. Assuming that this label does not match any from the user programmed list, the software should start a 30 second timer as soon as a non-matching label is received.

After another identical label is received (in the relevant LCI), the current programme is confirmed as completed, and the label is deleted from memory. If another identical label is not received, the 30 second timer is repeatedly restarted until two identical labels (not matching the user label) are received. Recording is only stopped after the 30 second count-down has been completed.

LCI	LABEL	MATCH	ACTIONS
0	19/2 08:00	Yes	Continue recording
0	19/2 10:30	No	Note 1st new label — Continue Recording — Start 30s Count-down
0	19/2 10:30	No	Note 2nd new label — Continue Recording — Continue Count-down
			Delete 19/2 08:00 label from memory
X	X	X	Continue recording until count-down completed
1	19/2 08:00	Yes	Continue Recording
1	19/2 08:01	No	Note 1st new label — Continue Recording — Start 30s Count-down
1	19/2 08:00	Yes	Note another 1st label — Continue Recording — Abandon Count-down
1	19/2 08:00	Yes	Note 2nd label — Continue Recording Label matches that in memory. No change of action required.

Note that providing the system is still in PDC mode (≥ 1 packet per 10 secs.), the time between received packets is irrelevant and therefore not shown in this table.

Table 1. Examples of two reception sequences with recommended actions

4. PRF and MI

These bits are proposed for addition to the PDC specification this year (1993). At the time of writing they are not believed to be in use anywhere in Europe. Software following the rules suggested in this document should always fail safe if these new facilities are not implemented: recording start and stop may include extra material, typically 30 seconds at each end of the recording.

a. Prepare to Record Flag

The Prepare to Record Flag, PRF, is intended to denote at its change from one to zero, the immediate start of the television programme. Providing the rest of the packet data is unchanged (and is in the same LCI), the software should act immediately on the information given by this bit – it should not wait for two identical labels with the PRF bit changed to zero.

In the event of packet reception problems around the time of a programme start signalled by PRF, the maximum delay in starting the VCR should be 10 seconds, after which timer mode should be applied.

LCI	PRF	LABEL	MATCH	ACTIONS
3	X	19/2 08:00	No	
3	X	19/2 08:00	No	
3	1	19/2 10:30	Yes	Note 1st new label
3	1	19/2 10:30	Yes	Note 2nd new label. — Start Record–Pause
3	1	19/2 10:30	Yes	Hold Record–Pause
3	1	19/2 10:30	Yes	Hold Record–Pause
3	0	19/2 10:30	Yes	Start Recording
3	0	19/2 10:30	Yes	Continue Recording

Table 2. Example of recommended actions when PRF is in use

b. Mode Indicator

The mode indicator (MI) bit has a similar effect to PRF in that when set to one, it denotes that the end of a television programme takes immediate effect upon the change of label within a particular LCI. However, unlike PRF, the software should not stop recording immediately, but after the reception two consecutive and identical labels, in the same LCI, that are different to the matched label. Essentially this removes the need to start a 30 second count-down timer, but not the need to validate a new label.

LCI	MI	LABEL	MATCH	ACTIONS		
2	1	19/2 08:00	Yes		Continue Recording	
2	1	19/2 08:00	Yes		Continue Recording	
2	X	19/2 10:30	No	Note 1st new label	Continue Recording	Do not start 30 sec. count-down
2	X	19/2 10:30	No	Note 2nd new label	Stop Recording	Delete 19/2 08:00 label from memory

Notes: In all the tables, an 'X' indicates a 'don't care' condition. The values shown for LCI are not important except that they do not change.

Table 3. Example of recommended actions when MI is in use

INTERFACING THE PDSP FAMILY

INTRODUCTION

GEC Plessey Semiconductors' PDSP family of DSP functional blocks are fabricated on a high speed CMOS process, and incorporate several design features to ease interfacing and board layout. However there are a few precautions which should be taken which will ensure trouble-free board design and operation.

All parts in the PDSP family are designed with the generic structure of Fig.1.

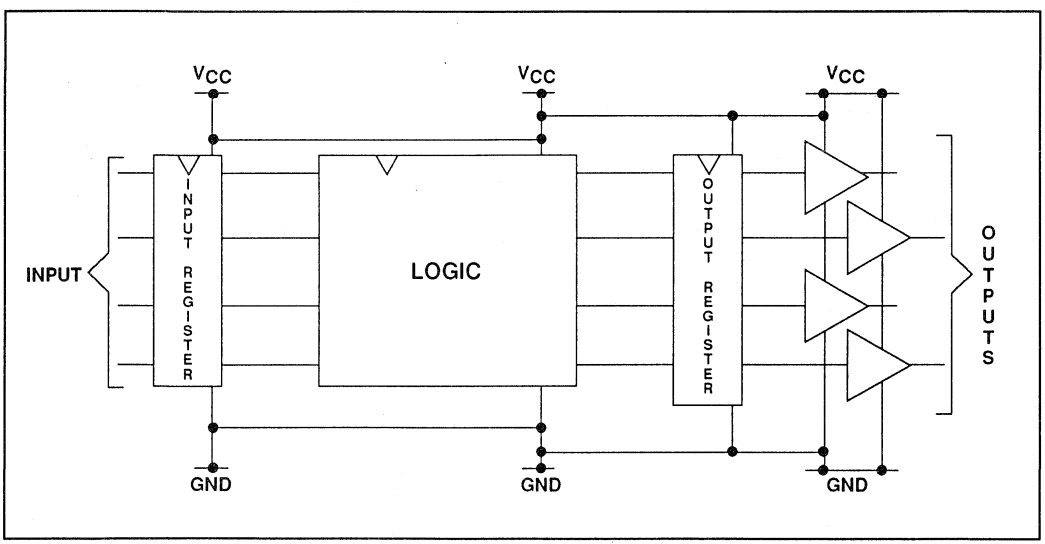


Fig.1 PDSP structure

The registered input is designed with a positive set-up time (ie data must be presented before the rising edge of the clock) and zero hold time (ie the data is allowed to change anytime after the rising edge of the clock). The input levels are designed for compatability with LSTTL outputs (V_{IH} = 2.2V, V_{IL} = 0.8 V), and the output, although conventional CMOS stages, are specified into a load of 2 standard LSTTL inputs + 20pF for track loading.

All PDSP devices have tri-state output buffers preceded by an output register, this ensures that the output data is valid for a whole clock cycle. To simplify timing requirements further, the clock to output valid delay is generally less than half a cycle at the maximum specified clock rate.

NOISE

The operating margins of all devices on a board of high-speed logic can best be maintained by providing a quiet environment free of noise spikes, undershoot, and ringing. The key elements in creating such an environment are good supply decoupling and termination of interconnections.

POWER DISTRIBUTION

To maintain wide operating margins across all devices on a board, the supply impedance at each device must be kept to a minimum. The internal design of PDSP devices is such that the input registers, main logic, and output buffers have separate supply pins. This arrangement is designed to ensure that current spikes generated in the output drivers do not modulate the supply to the input gates, hence altering the thresholds. Although these multiple supply pins are internally connected, the internal paths are not particularly low impedance, and therefore each individual Vcc pin should be separately decoupled.

The total supply impedance at a device is a function of the supply line impedance and the decoupling capacitors. In practice, the effect of local decoupling does not extend very far, because of the very fast edges of the current spikes generated by CMOS output stages and the inductive nature of the PCB tracks. In order to minimise the effects of these transients, the decoupling capacitors should be high quality, low inductance parts mounted as close as possible to the device pins, with as short a track length as is practical. Capacitor values should be in the 0.1 to 0.47μF region, too small and there will be insufficient decoupling, too large and the equivalent inductance will reduce decoupling efficiency. The quality of the ground connection is also important, this should be either a solid plane or a grid to minimise inductance and prevent loss of noise margin due to differential ground noise between devices.

Low frequency current transients can best be handled by tantalum capacitors mounted close to the edge connector where the panel tracks meet the backplane power distribution system. Such large capacitors provide bulk energy storage which prevents voltage drops due to the long inductive path between the logic board and the system power supply.

TRACK TERMINATION

On a large board PCB tracks look like shorted transmission lines to the signals they are carrying . This causes reflection of the signal resulting in undershoot, overshoot or ringing. Particular cases which can cause difficulty are large RAM arrays being addressed by the PDSP1601 - the long track lengths and heavy capacitative loading can store and reflect amounts of energy leading to severe ringing - and LSTTL to CMOS interface via long tracks which can suffer severe undershoot. In both cases track termination is best effected by a series resistor at the driving end (typically 10 or 18 ohms). Parallel termination is not recommended since it reduces the voltage swing at the input (making the noise margin even worse), consumes DC power (hardly desirable in a CMOS system) and doesn't work very well in any case.

VERIFICATION

When a board design is complete and the prototype built, it is good practice to check the power supplies to each device and the signals on the buses with a wideband 'scope to ensure that excessive noise, ringing or undershoot is not present. A board which works on the bench but which is marginal because of noise problems will almost certainly exhibit gremlins in the field.

A HIGH RESOLUTION FFT PROCESSOR USING THE PDSP16116/A

The PDSP16116A has been designed with an integral Block Floating Point system which can be used, in conjunction with other GEC Plessey Semiconductors' PDSP parts, to process FFTs with a combination of speed and accuracy previously unobtainable. All the functionality of this BFP system is contained within the PDSP parts, which are designed to interface easily to achieve a powerful FFT solution.

A butterfly processor based on the 20MHz PDSP16116A will allow the following FFT benchmarks:

1024 point complex radix-2 transform in 259us
512 point complex radix-2 transform in 118us
256 point complex radix-2 transform in 53us

This compares favourably with the current industry standard benchmark of around 2ms for a 1024 point complex FFT, but if speed is all important for a particular application, then the GEC Plessey Semiconductors PDSP16112/A 16x12 Complex Mulitplier can double the PDSP16116/A performance with up to 70dB of dynamic range.

The FFT Algorithm

The Fast Fourier Transform is essentially a computationally efficient algorithm for extracting spectral information from signal waveforms, which may be in real time or recorded form (i.e. a transformation from the time domain to the frequency domain). It is often used to dramatic effect in a growing range of applications including radar and sonar processing, speech recognition and image processing. It is no less accurate than the related Discrete Fourier Transform (DFT), but it enjoys a vastly improved performance due to the 'divide and conquer' approach of its algorithm.

There are several variations of the FFT algorithm, each with their own merits. For high throughput, hardware implemented solutions, a variant of the Radix-2 Decimation-in-Time algorithm is most suitable. The 'Constant Geometry' algorithm (Fig. 1) is easier to implement whereas the 'In-Place' algorithm (Fig. 2) halves the amount of memory required.

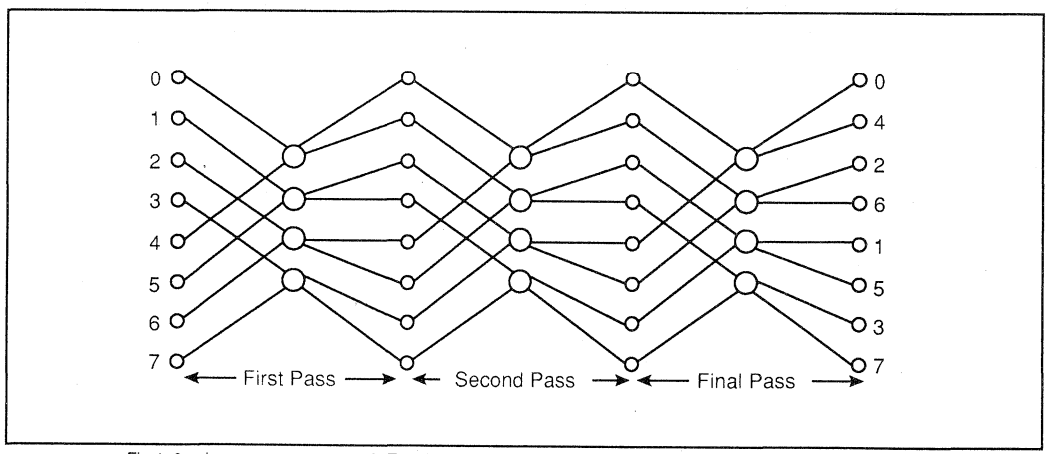


Fig.1 8 point constant geometry DIT radix 2 algorithm with normally ordered inputs and bit-reversed outputs

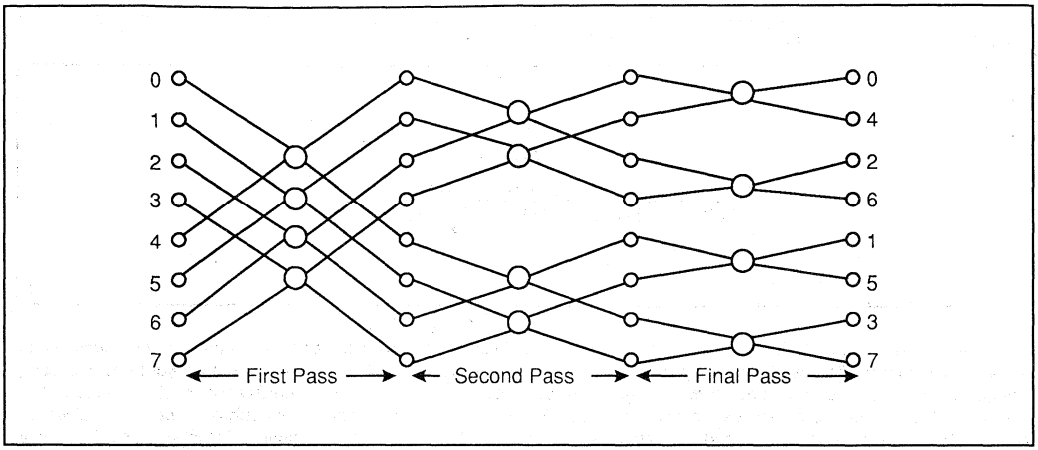
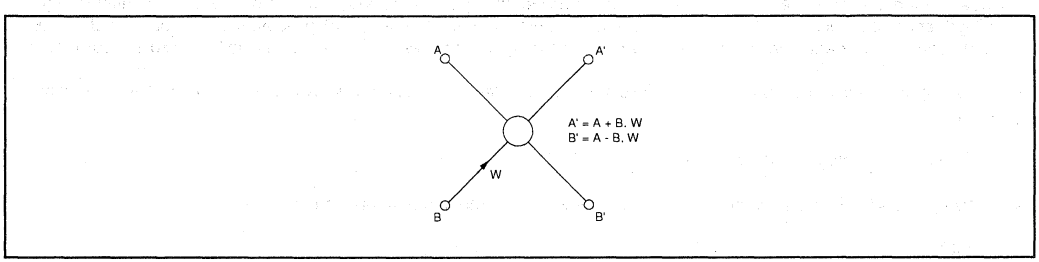


Fig.2 8 point in-place DIT radix 2 algorithm with normally ordered inputs and bit-reversed outputs

Both these variations are split vertically into a number of 'passes' ($\log_2 N$ passes for an N-point transform), each pass consisting of N/2 'butterfly' operations:



W is the complex coefficient and A and B are, for the first pass, the sampled data and then, in the second and subsequent passes, the values of A' and B' from the previous pass. The results of the FFT are the values of A' and B' from the butterflies of the final pass. In order to be compatible with previous FFT results, all points must be normalised to a universal format. These final complex number values (cartesian co-ordinates) may then be converted into magnitude and phase components (polar co-ordinates).

Defeating the Wordgrowth Problem

One of the most difficult problems to overcome when implementing an FFT algorithm in fixed point arithmetic is that of wordgrowth. The power of the PDSP16116s BFP system lies in its flexible and effective response to this problem. Before looking into the operation of this BFP system, the wordgrowth problem and some of the other solutions available are explained.

FFTs are implemented by means of successive multiplications and additions. Each time data is processed by an ALU (i.e. twice in each butterfly) there is the possibility of wordgrowth occurring: i.e. when two 16 bit words are added, they may produce a sum of 17 bits. The safe way to deal with this is to always pick the 16MSBs of the result. However, this will cause sign extension, i.e. repetition of the sign bit in the MSBs of the data. These two cases are illustrated in the examples below.

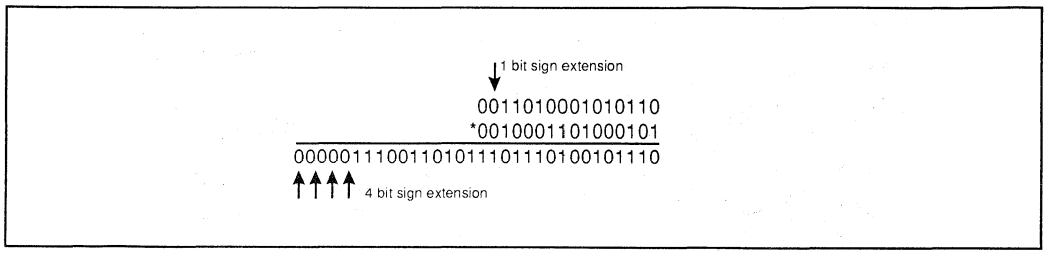
Wordgrowth occurs:

```
 0101110101110100
+0110100110101001
-----------------
01100011100011101
```

Wordgrowth does not occur:

```
 0101010111011010
+0010100010101110
-----------------
 0011111101000 1000
               ^
               |
          sign extension
```

Sign extension can cause severe problems when the next multiplication occurs, as it is likely to lead to a product with a further extended sign bit. For example:



After a few passes of the FFT, there is a danger that the data could become all sign bits and no information - not much use to anyone. The common alternative to this approach is to pick the 16 LSBs from the ALUs and hope that no wordgrowth occurs, as this will then lead to overflow. If overflow is flagged during the course of an FFT, then the calculation must be aborted. The input data is then scaled down and the calculation repeated. The hit and miss nature of this approach can be avoided by automatically scaling down the inputs and accepting the resulting penalty in accuracy. A 'conditional shift' system offers some degree of flexibility. Here, the 16 LSBs are selected from the second ALU in the butterfly hardware if no overflow occurs in any butterfly during that pass.

The PDSP16116 offers a superior solution to the problem by employing an intelligent control system which can monitor data magnitudes during the course of the FFT and adjust them as necessary so as to keep extended sign bits to a minimum, whilst eliminating the possibility of overflow. In fact, this system can not only deal with wordgrowth problems as they occur, but can also adjust underscaled input data in anticipation of these problems to ensure that a valid result is obtained at the end of the calculation.

A comparison of the data formats provided by each of the methods detailed above will clarify their differences. Given input data of the format:

X.XXX... (note the position of the binary point)

The UNCONDITIONAL SHIFT implementation will output all data at the end of a pass in the format:

XXX.X...

regardless of whether the data has increased in magnitude or not.

The CONDITIONAL SHIFT implementation will either output ALL data in the format:

XX.XX...

if the maximum wordgrowth was one bit in any butterfly; or, if two bits of wordgrowth occurred in any butterfly, then ALL data will be output in the format:

XXX.X...

The BFP implementation can output EACH butterfly result in ANY of the following formats, according to the data magnitude:

If data is underscaled	.XXXX...
If no wordgrowth occurs	X.XXX...
If wordgrowth occurs once	XX.XX...
If wordgrowth occurs twice	XXX.X...

The adaptability of the BFP system is clearly illustrated and it is this adaptability which allows the BFP system to defeat the wordgrowth problem.

How the BFP System Operates

A block floating point system is essentially an ordinary integer arithmetic system with some additional logic, the object of which is to lend the system some of the enormous dynamic range afforded by a true floating point system without suffering the corresponding loss in performance.

The initial data used by the FFT should all have the same binary weighting, i.e. the binary point should occupy the same position in every data word. This is normal in integer arithmetic. However, during the course of the FFT, a variety of weightings are used in the data words to increase the dynamic range available. This situation is similar to that within a true floating point system, though the range of numbers representable is more limited.

In the BFP system used in the PSDP16116, there are, within any one pass of the FFT, four possible positions of the binary point within the integer words. To record the position of its binary point, each word has a 2-bit word tag associated with it. By way of example, in a particular pass we may have the following four positions of binary point available, each denoted by a certain value of word tag:

XX.XXXXXXXXXXXXX	word tag = 00
XXX.XXXXXXXXXXXX	word tag = 01
XXXX.XXXXXXXXXXX	word tag = 10
XXXXX.XXXXXXXXXX	word tag = 11

At the end of each constituent pass of the FFT, the positions of the binary point supported may change to reflect the trend of data increases or decreases in magnitude. Hence, in the pass following that of the above example, the four positions of binary point supported may change to:

XXXX.XXXXXXXXXXX	word tag = 00
XXXXX.XXXXXXXXXX	word tag = 01
XXXXXX.XXXXXXXXX	word tag = 10
XXXXXXX.XXXXXXXX	word tag = 11

This variation in the range of binary points supported from pass to pass (i.e. the movement of the binary point relative to its position in the original data) is recorded in the Global Weighting Register (GWR). At the end of the final pass, the distance that the binary point has moved since the start of the FFT can be obtained by modifying the GWR according to the value of WTOUT of a particular word, as shown below:

WTOUT1:0	ADJUSTMENT TO GWR
00	SUBTRACT 1
01	NO ADJUSTMENT
10	ADD 1
11	ADD 2

For example, if the original data format was:

X.XXXXXXXXXXXXXX

then, if the GWR = 01001 and with WTOUT = 10 for a particular word, the binary point has moved 10 places to the right of its original position and will be situated as shown below:

XXXXXXXXXX.XXXXX

Using the GWR with Large FFTs

The Global Weighting Register represents the movement of the binary point in two's complement notation in a 5-bit field. An examination of FFT theory and the operation of the BFP system shows that, for an N-point transform, GWR will not exceed (2 = $\log_2 N$). This means that GWR can handle transforms as large as 8K by representing the movement of the binary point as a two's complement number. However, GWR can be used for much larger transforms by noting that GWR will never drop below -8, since with this degree of left shift, the rounding noise is amplified to fill the whole 16-bit data word. This fact allows GWR to be extended and represented as a six bit value simply by ANDing the two most significant bits to produce a new sign bit (Fig 3). This 6-bit field allows GWR to handle up to a 2097K transform.

Value of GWR	Decimal Equiv.	Meaning		
00000	0	Binary point as not moved		
00001	+1	Binary point has moved	1	place to the right
00010	+2		2	
00011	+3		3	
00100	+4		4	
00101	+5		5	
00110	+6		6	
00111	+7		7	
01000	+8		8	
01001	+9		9	
01010	+10		10	
01011	+11		11	
01100	+12		12	
01101	+13		13	
01110	+14		14	
01111	+15		15	
10000*	+16		16	
10001*	+17		17	
10010*	+18		18	
10011*	+19		19	
10100*	+20		20	
10101*	+21		21	
10110*	+22		22	
10111*	+23		23	
11000	-8	Binary point has moved	8	places to the left
11001	-7		7	
11010	-6		6	
11011	-5		5	
11100	-4		4	
11101	-3		3	
11110	-2		2	
11111	-1		1	

* not in two's complement format

Table.1 GWR values and meanings

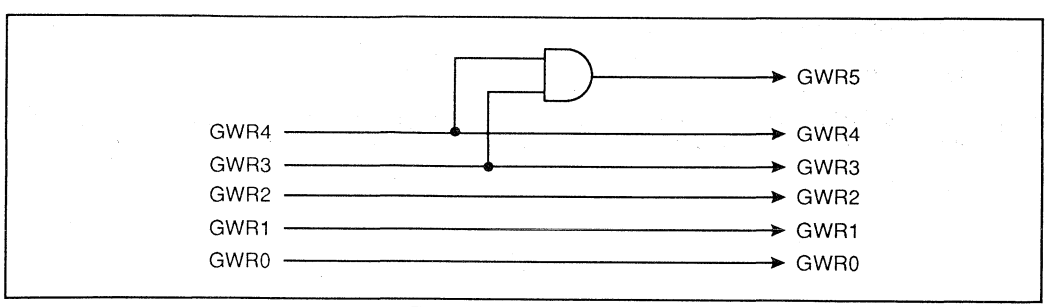


Fig.3 Extending GWR to 6 bits

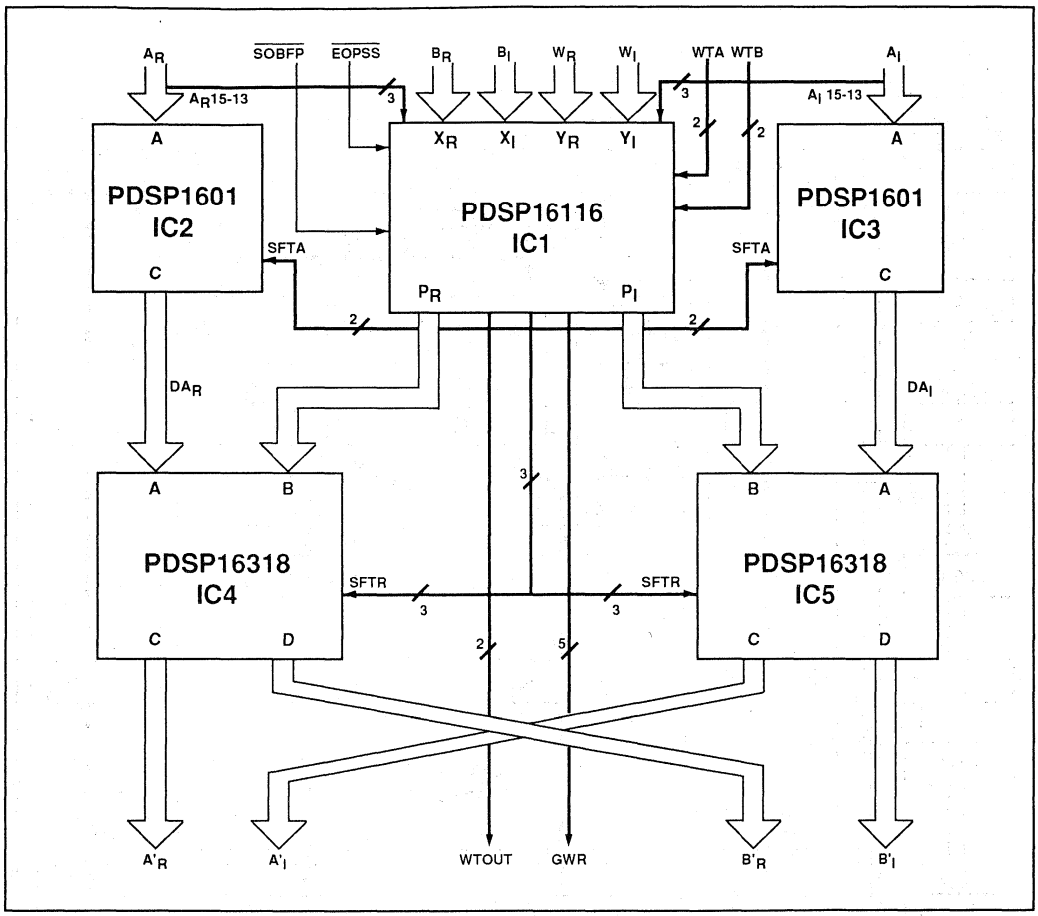


Fig.4 Block Floating Point FFT butterfly

Construction of an FFT Butterfly Processor

As described earlier, the calculations A' = A + BW and B' = A - BW, forming a 'butterfly operation' must be carried out repeatedly in the course of an FFT. Fig. 4 shows how a butterfly processor may be constructed using a single PDSP16116 in combination with two GEC Plessey Semiconductors' PDSP16318s and two GEC Plessey Semiconductors' PSDP1601s. The PDSP1601s are used to match the pipeline delay and shifting operations of the PDSP16116 to the datapath of the A word. The PDSP16318s are used to perform the complex addition and subtraction of the butterfly operation. Fig. 5 details the underlying architecture of the processor.

A detailed list of the various connections required to combine these five chips into a butterfly processor appears in the Appendix. I/O connections are not specified as there are a number of I/O options that allow the butterfly processor to be interfaced with the rest of an FFT system.

A point to note is the hard-wired 1-bit right shift in the A-word data paths between the PDSP16116 outputs and the PDSP16318 inputs. This is to keep the A-word data format the same as the PDSP16116 output data format so that the two words may be added within the PDSP16318. The PDSP1601 applies a shift of 0 to 3 places to the right whereas data is output from the PDSP16116 with the binary point shifted from 1 to 4 places to the right. Hence an extra right shift of one place needs to be inserted in the PDSP1601 data path to keep the data formats compatible at the inputs to the PDSP16318 (data words must have their binary points in the same places before being added).

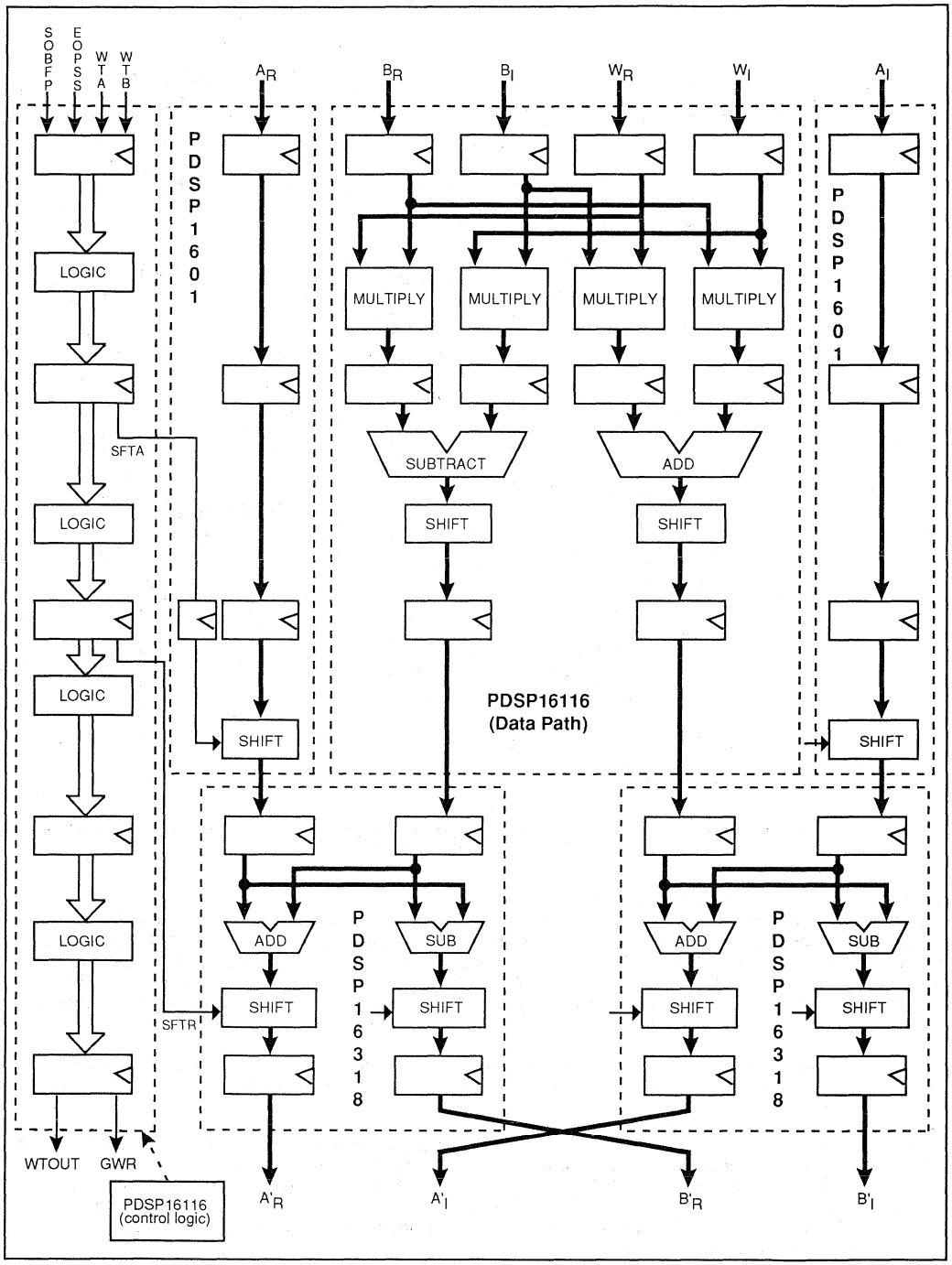


Fig.5 BFP Butterfly Detail

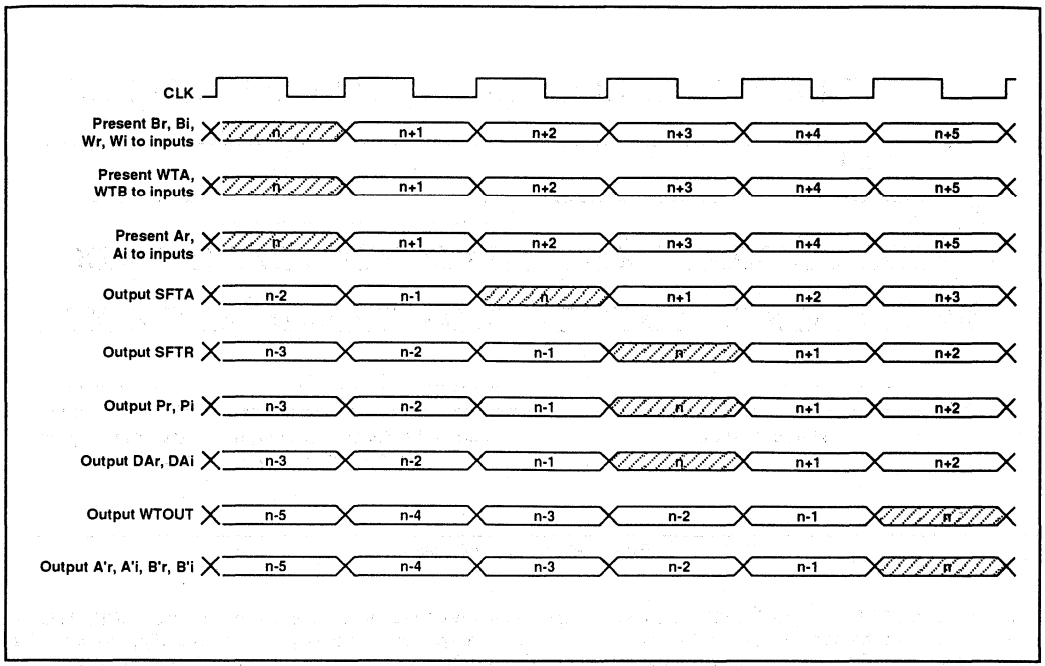


Fig.6 Data and Control Timing in the Butterfly

The Butterfly Operation

A new butterfly operation is commenced each cycle, requiring a new set of data for A, B, W, WTA and WTB. Five cycles later, the corresponding results A' and B' are produced along with their associated WTOUT. In between, the signals SFTA and SFTR are produced and acted upon by the shifters in the PDSP1601 and PDSP16318. The timing of the data and control signals is shown in Fig. 6.

The results (A' and B') of each butterfly calculation in a pass must be stored away to be used later as the input data (A and B) in the next pass. In every pass, each result must be stored together with its associated word tag, WTOUT. Although WTOUT is common to both A' and B', it must be stored separately with each word as the words are used on different cycles during the next pass. At the inputs, the word tag associated with the A word is known as WTA and the word tag associated with the B word is known as WTB. Hence the WTOUTs from one pass with become the WTAs and the WTBs for the following pass. It should be noted that the first pass is unique in that word tags need not be input into the butterfly as all data must initially have the same weighting. Therefore, during the first pass alone, the inputs WTA and WTB are ignored.

Control of the FFT

To enable the block floating point hardware to keep track of the data, the following signals are provided:

SOBFP - start of the FFT
EOPSS - end of current pass

These inform the PDSP16116 when an FFT is starting and when each pass is complete. Fig. 7 shows the timing of these signals and an explanation of their use follows.

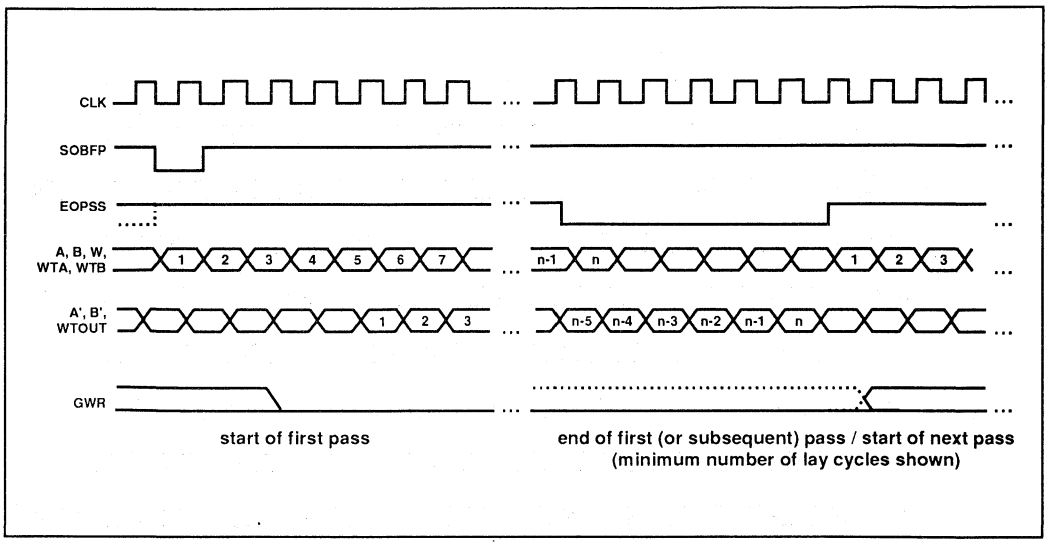


Fig.7 Use of BFP Control Signals

To commence the FFT, the signal EOPSS should be set high (where it will remain for the duration of the pass). SOBFP should be pulled low during the initial cycle, when the first data words A and B are presented to the inputs of the butterfly processor. The following cycle, SOBFP must be pulled high where it should remain for the duration of the FFT. New data is presented to the processor each successive cycle until the end of the first pass of the FFT. On the last cycle of the pass, the signal EOPSS should be pulled low and remain low for a minimum of five cycles, the time required to clear the pipeline of the butterfly processor so that all the results from one pass are obtained before commencing the following pass (should a longer pause be required between passes - to arrange the data for the next pass, for example - then EOPSS may be kept low for as long as necessary, the next pass cannot commence until it is brought high again). On the initial cycle of each new pass, the signal EOPSS should be pulled high and it should remain high until the final cycle of that pass, when it is pulled low again.

Building an FFT System

The Butterfly Processor is only one element of a complete FFT system. Also required are fast A/D converters at the front end of the system; a complex heterodyne filter to zoom-in on the frequencies of interest; fast memory and addressing circuits to store the data; additional fast memory and addressing circuits for the coefficients; an output normalisation circuit to make all data consistent; a Pythagoras Processor to extract magnitude and phase information from the results; finally, a D/A converter to allow the magnitude and phase information to be displayed on a video screen or oscilloscope. Fig. 8 shows how these blocks are connected. GEC Plessey Semiconductors makes a range of high performance DSP devices which solve the more difficult problems outlined above. The complex heterodyne filter may be constructed from a combination of either a PDSP16116 or PDSP16112 complex multiplier and either a PDSP16318 complex accumulator or two PDSP1601 augmented arithmetic logic units. Output normalisation is a simple matter with the PDSP1601's adaptable barrel shifter and the PDSP16330 Pythagoras processor to convert Cartesian to polar coordinates.

Memory Requirements

Memory requirements differ according to whether the 'In-Place' or 'Constant Geometry' algorithms are used. In either case, two reads from memory (A and B) and two writes to memory (A' and B') have to be made each 100ns cycle.

For the In-Place algorithm, the results (A', B') of a butterfly are written to the same locations from which the inputs (A & B) were read. Hence, the memory must have an access time of 25ns to cope with the two reads and two writes.

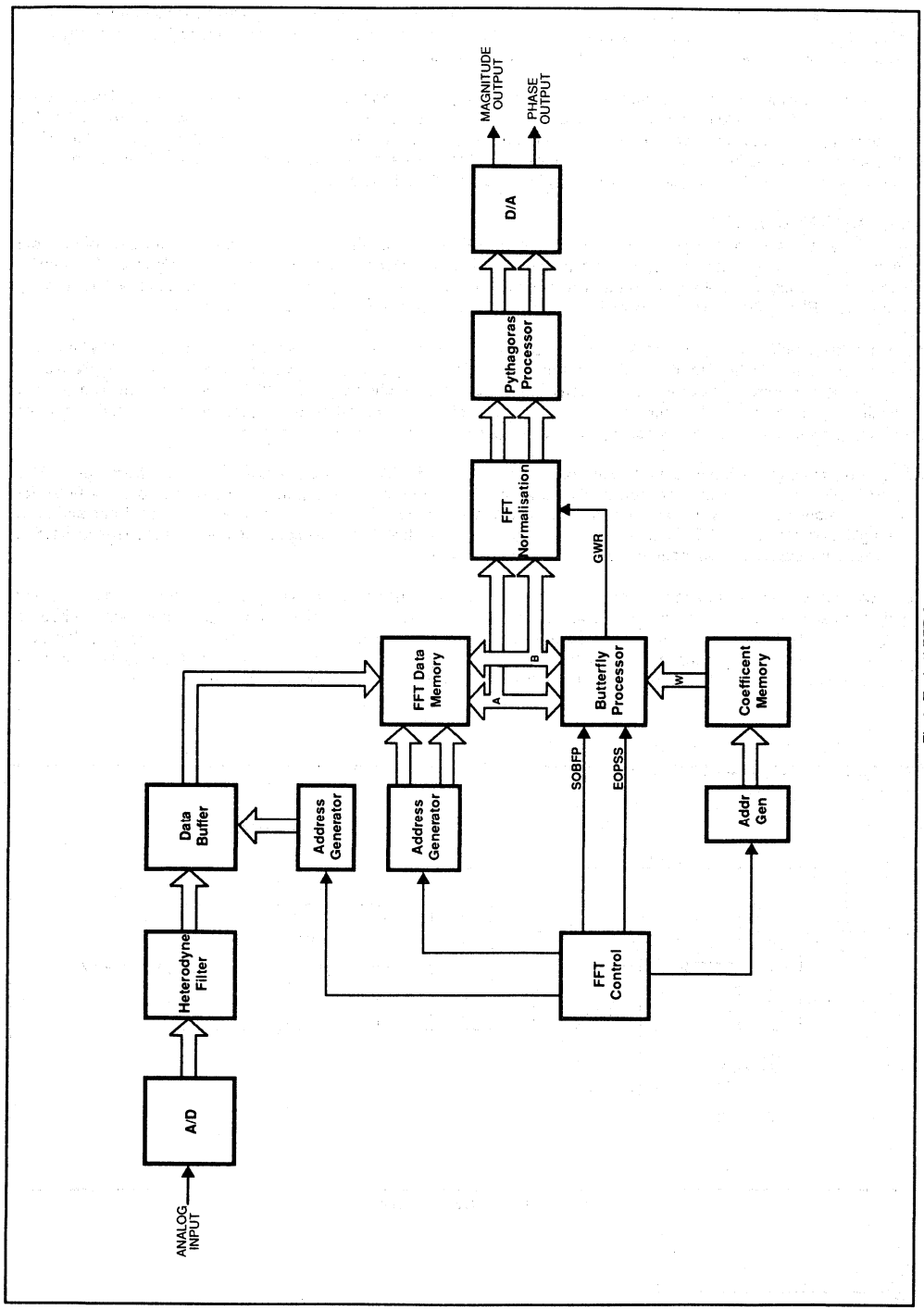


Fig.8 Typical FFT System

The Constant Geometry algorithm requires a memory access time of only 50ns, but the memory size must be double that of the In-Place algorithm. This is because the addresses written to after each butterfly are different from those from which the input data was read. This is possible due to the order in which data points are addressed.

The memory must be 32 bits wide to accommodate the real and imaginary parts of each word. Also, the 2 bit word tag must be stored with each word. This could be achieved by widening the memory to 34 bits or, alternatively, it could be stored in the LSB of the real and imaginary parts of the word, keeping the memory width at 32 bits. This would not affect the accuracy of the FFT, as the LSB is a rounded value in any case. There would be no problem in the initial pass when no word tags have been written to the memory as the PDSP16116 ignores the word tag inputs during the initial pass.

FFT Output Normalisation

In order to preserve the dynamic range of the data during the FFT calculation, the PDSP16116 employs a range of different weightings, however, at the end of the FFT, the data must be re-formatted to a pre-determined common weighting. This can be done by comparing the exponent of a given data word with the required universal exponent and then shifting the data word by the difference. The PDSP1601 ALU, with its multifunction 16-bit barrel shifter, is ideally suited to this task.

What value should the universal exponent take ? Theoretically, the largest possible data result from an FFT is 1.27N times the largest input data, where N is the size of the FFT. This means that the binary point can move a maximum of $(1 + \log_2 N)$ places to the right. Hence, if the universal exponent is chosen to be $(1 + \log_2 N)$, this should give a sufficient range to represent all data points faithfully. In practice, the FFT output data may never approach the theoretical maximum, therefore it may be worthwhile trying various universal exponents and choosing the one best suited to the particular application.

Data is output from the butterfly processor with a two part exponent: the 5-bit GWR applicable to all data words from a given FFT and a 2-bit WTOUT associated with each individual data word. To find the complete exponent for a given word, the GWR for that FFT must be modified by the WTOUT value, the result being the number of places that the binary point has been shifted to the right during the course of the FFT. This value must be subtracted from the universal exponent, the difference being the shift required for that data word, which is input to the SV port of the PDSP1601.

As FFT data consists of real and imaginary parts, either two PDSP1601s must be used or a single PDSP1601 handling real and imaginary data on alternate cycles, the same shift being applied to both parts. An example of an output normalisation circuit is shown in Fig. 9. Only 4-bit arithmetic is used in calculating the shift which means that very small (negative) values of GWR must be trapped and a forced 16-bit right shift applied. (NB. It is easier to simply add the word tag value to the GWR to determine the shift rather than modifying it exactly. To compensate for this, the universal exponent should be increased by one.)

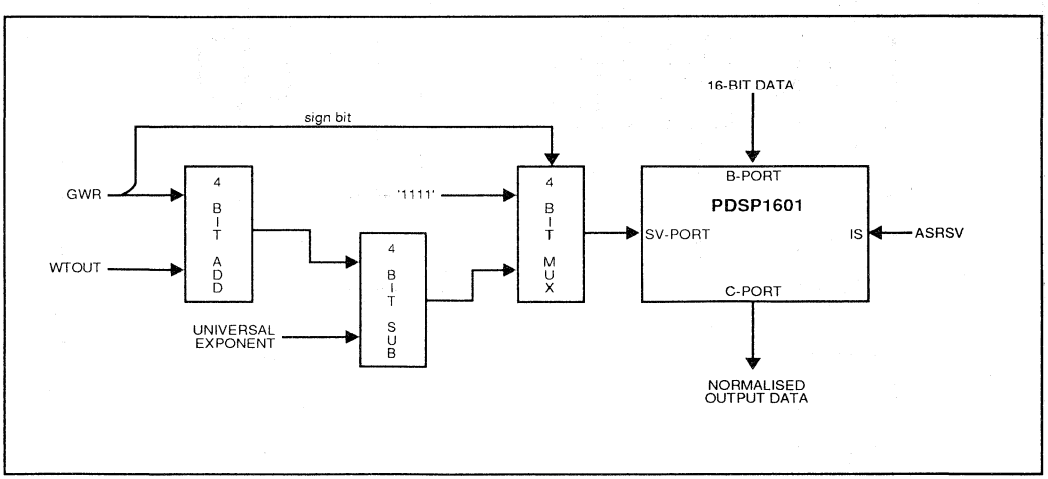


Fig.9 Output Normalisation Circuitry

Appendix A - Block Floating Point FFT Butterfly Net List

The following net lists give all the connections required for implementing the Block Floating Point FFT butterfly shown in Fig.4 :

IC1: PDSP16116 Complex Multiplier

Pin No.	Pin desc.	Net Name	Connections
D3	PI14	PI14	IC5-C11
C2	PI15	PI15	IC5-D10
B1	WTOUT1	WTOUT1	external o/p
D2	WTOUT0	WTOUT0	external o/p
E3	SFTR0	SFTR0	IC4-L7; IC5-L7
C1	SFTR1	SFTR1	IC4-J7; IC5-J7
E2	SFTR2	SFTR2	IC4-J6; IC5-J6
D1	OEI		tie low
F3	CONX		tie low
F2	CONY		tie low
E1	ROUND		tie high
G2	AI13	AI13	external i/p; IC3-H1
G3	AI14	AI14	external i/p; IC3-F1
F1	AI15	AI15	exteral i/p; IC3-G2
G1	AR13	AR13	external i/p; IC2-H1
H2	AR14	AR14	external i/p; IC2-F1
H1	AR15	AR15	external i/p; IC2-G2
H3	YI15	WI15	external i/p
J3	YI14	WI14	external i/p
J1	YI13	WI13	external i/p
K1	YI12	WI12	external i/p
J2	YI11	WI11	external i/p
K2	YI10	WI10	external i/p
K3	YI9	WI9	external i/p
L1	YI8	WI8	external i/p
L2	YI7	WI7	external i/p
M1	YI6	WI6	external i/p
N1	YI5	WI5	external i/p
M2	YI4	WI4	external i/p
L3	YI3	WI3	external i/p
N2	YI2	WI2	external i/p
P1	YI1	WI1	external i/p
M3	YI0	WI0	external i/p
N3	XI0	BI0	external i/p
P2	GND	GND	0V supply rail
R1	VDD	VDD	+5V supply rail
N4	XI1	BI1	external i/p
P3	XI2	BI2	external i/p
R2	XI3	BI3	external i/p
P4	XI4	BI4	external i/p
N5	XI5	BI5	external i/p
R3	XI6	BI6	external i/p
P5	XI7	BI7	external i/p
R4	XI8	BI8	external i/p
N6	XI9	BI9	external i/p
P6	XI10	BI10	external i/p
R5	XI11	BI11	external i/p
P7	XI12	BI12	external i/p
N7	XI13	BI13	external i/p
R6	XI14	BI14	external i/p
R7	XI15	BI15	external i/p

IC1: PDSP16116 Complex Multiplier (Continued)

Pin No.	Pin desc.	Net Name	Connections
P8	CEY		tie low
R8	CEX		tie low
N8	XR15	BR15	external i/p
N9	XR14	BR14	external i/p
R9	XR13	BR13	external i/p
R10	XR12	BR12	external i/p
P9	XR11	BR11	external i/p
P10	XR10	BR10	external i/p
N10	XR9	BR9	external i/p
R11	XR8	BR8	external i/p
P11	XR7	BR7	external i/p
R12	XR6	BR6	external i/p
R13	XR5	BR5	external i/p
P12	XR4	BR4	external i/p
N11	XR3	BR3	external i/p
P13	XR2	BR2	external i/p
R14	XR1	BR1	external i/p
N12	XR0	BR0	external i/p
N13	YR15	WR15	external i/p
P14	YR14	WR14	external i/p
R15	YR13	WR13	external i/p
M13	GND	GND	0V supply rail
N14	VDD	VDD	+5V supply rail
P15	YR12	WR12	external i/p
M14	YR11	WR11	external i/p
L13	YR10	WR10	external i/p
N15	YR9	WR9	external i/p
L14	YR8	WR8	external i/p
M15	YR7	WR7	external i/p
K13	YR6	WR6	external i/p
K14	YR5	WR5	external i/p
L15	YR4	WR4	external i/p
J14	YR3	WR3	external i/p
J13	YR2	WR2	external i/p
K15	YR1	WR1	external i/p
J15	YR0	WR0	external i/p
H14	EOPSS	EOPSS	external i/p
H15	VDD	VDD	+5V supply rail
H13	SOBFP	SOBFP	external i/p
G13	WTB1	WTB1	external i/p
G15	WTB0	WTB0	external i/p
F15	WTA1	WTA1	external i/p
G14	WTA0	WTA0	external i/p
F14	MBFP		tie high
F13	CLK	CLK	external i/p - common to all ICs
E15	OSEL1		tie low
E14	OSEL0		tie low
D15	OER		tie low
C15	SFTA0	SFTA0	IC2-L6; IC3-L6
D14	SFTA1	SFTA1	IC2-L8; IC3-L8
E13	GWR0	GWR0	external o/p
C14	GWR1	GWR1	external o/p
B15	GWR2	GWR2	external o/p
D13	GWR3	GWR3	external o/p
C13	GWR4	GWR4	external io/p
B14	PR15	PR15	IC4-D10
A15	PR14	PR14	IC4-C11

IC1: PDSP16116 Complex Multiplier (Continued)

Pin No.	Pin desc.	Net Name	Connections
C12	VDD	VDD	+5V supply rail
B13	GND	GND	0V supply rail
A14	PR13	PR13	IC4-B11
B12	PR12	PR12	IC4-C10
C11	PR11	PR11	IC4-A11
A13	PR10	PR10	IC4-B10
B11	PR9	PR9	IC4-B9
A12	PR8	PR8	IC4-A10
C10	PR7	PR7	IC4-A9
B10	PR6	PR6	IC4-B8
A11	PR5	PR5	IC4-A8
B9	GND	GND	0V supply rail
C9	VDD	VDD	+5V supply rail
A10	PR4	PR4	IC4-B6
A9	PR3	PR3	IC4-B7
B8	PR2	PR2	IC4-A7
A8	PR1	PR1	IC4-C7
C8	PR0	PR0	IC4-C6
C7	PI0	PI0	IC5-C6
A7	PI1	PI1	IC5-C7
A6	PI2	PI2	IC5-A7
B7	PI3	PI3	IC5-B7
B6	PI4	PI4	IC5-B6
C6	VDD	VDD	+5V supply rail
A5	PI5	PI5	IC5-A8
B5	GND	GND	0V supply rail
A4	PI6	PI6	IC5-B8
A3	PI7	PI7	IC5-A9
B4	PI8	PI8	IC5-A10
C5	PI9	PI9	IC5-B9
B3	PI10	PI10	IC5-B10
A2	PI11	PI11	IC5-A11
C4	PI12	PI12	IC5-C10
C3	PI13	PI13	IC5-B11
B2	GND	GND	0V supply rail
A1	VDD	VDD	+5V supply rail

IC2: PDSP1601 - Real Path

Pin No.	Pin desc.	Net Name	Connections
B10	VCC	VDD	+5V supply rail
A6	MSB		tie low
A5	MSS		tie high
B5	B15		tie low
C5	B14		tie low
A4	B13		tie low
B4	B12		tie low
A3	B11		tie low
A2	B10		tie low
B3	B9		tie low
A1	B8		tie low
B2	B7		tie low
C2	B6		tie low
B1	B5		tie low
C1	B4		tie low
D2	B3		tie low
D1	B2		tie low
E3	B1		tie low
E2	B0		tie low
E1	CEB		tie high
F2	CLK	CLK	external i/p - common to all ICs
F3	GND	GND	0V supply rail
G3	MSA0		tie high
G1	MSA1		tie low
G2	A15	AR15	external i/p ; IC1-H1
F1	A14	AR14	external i/p ; IC1 - H2
H1	A13	AR13	external i/p ; IC1-G1
H2	A12	AR12	external i/p
J1	A11	AR11	external i/p
K1	A10	AR10	external i/p
J2	A9	AR9	external i/p
L1	A8	AR8	external i/p
K2	A7	AR7	external i/p
K3	A6	AR6	external i/p
L2	A5	AR5	external i/p
L3	A4	AR4	external i/p
K4	A3	AR3	external i/p
L4	A2	AR2	external i/p
J5	A1	AR1	external i/p
K5	A0	AR0	external i/p
L5	CEA		tie low
K6	MSC		tie high
K10	VCC	VDD	+5V supply rail
J6	IS0		tie low
J7	IS1		tie high
L7	IS2		tie low
K7	IS3		tie high
L6	SV0	SFTA0	IC1-C15
L8	SV1	SFTA1	IC1-D14
K8	SV2		tie low
L9	SV3		tie low
L10	SVOE		tie high
K9	RS0		tie high
L11	RS1		tie high
J10	RS2		tie high

IC2: PDSP1601 - Real Path (continued)

Pin No.	Pin desc.	Net Name	Connections
K11	C0		N/C
J11	C1	DAR0	IC4-L11
H10	C2	DAR1	IC4-K10
H11	C3	DAR2	IC4-J10
F10	C4	DAR3	IC4-K11
G10	C5	DAR4	IC4-J11
G11	C6	DAR5	IC4-H10
G9	C7	DAR6	IC4-H11
F9	GND	GND	0V supply rail
F11	C8	DAR7	IC4-F10
E11	C9	DAR8	IC4-G10
E10	C10	DAR9	IC4-G11
E9	C11	DAR10	IC4-G9
D11	C12	DAR11	IC4-F9
D10	C13	DAR12	IC4-F11
C11	C14	DAR13	IC4-E11
B11	C15	DAR14:15	IC4-E9, E10
C10	OE		tie low
A11	BFP		N/C
B9	CO		N/C
A10	RA0		L on even cycles, H on odd cycles
A9	RA1		tie high
B8	RA2		tie low
A8	CI		tie low
B6	IA0		tie low
B7	IA1		tie high
A7	IA2		tie high
C7	IA3		tie low
C6	IA4		tie high

IC3: PDSP1601 - Imaginary Path

Pin No.	Pin desc.	Net Name	Connections
B10	VCC	VDD	+5V supply rail
A6	MSB		tie low
A5	MSS		tie high
B5	B15		tie low
C5	B14		tie low
A4	B13		tie low
B4	B12		tie low
A3	B11		tie low
A2	B10		tie low
B3	B9		tie low
A1	B8		tie low
B2	B7		tie low
C2	B6		tie low
B1	B5		tie low
C1	B4		tie low
D2	B3		tie low
D1	B2		tie low
E3	B1		tie low
E2	B0		tie low
E1	CEB		tie high
F2	CLK	CLK	external i/p - common to all ICs
F3	GND	GND	0V supply rail
G3	MSA0		tie high
G1	MSA1		tie low
G2	A15	AI15	external i/p ; IC1-F1
F1	A14	AI14	external i/p ; IC1 - G3
H1	A13	AI13	external i/p ; IC1-G2
H2	A12	AI12	external i/p
J1	A11	AI11	external i/p
K1	A10	AI10	external i/p
J2	A9	AI9	external i/p
L1	A8	AI8	external i/p
K2	A7	AI7	external i/p
K3	A6	AI6	external i/p
L2	A5	AI5	external i/p
L3	A4	AI4	external i/p
K4	A3	AI3	external i/p
L4	A2	AI2	external i/p
J5	A1	AI1	external i/p
K5	A0	AI0	external i/p
L5	CEA		tie low
K6	MSC		tie high
K10	VCC	VDD	+5V supply rail
J6	IS0		tie low
J7	IS1		tie high
L7	IS2		tie low
K7	IS3		tie high
L6	SV0	SFTA0	IC1-C15
L8	SV1	SFTA1	IC1-D14
K8	SV2		tie low
L9	SV3		tie low
L10	SVOE		tie high
K9	RS0		tie high
L11	RS1		tie high
J10	RS2		tie high

IC3: PDSP1601 - Imaginary Path (continued)

Pin No.	Pin desc.	Net Name	Connections
K11	C0		N/C
J11	C1	DAI0	IC5-L11
H10	C2	DAI1	IC5-K10
H11	C3	DAI2	IC5-J10
F10	C4	DAI3	IC5-K11
G10	C5	DAI4	IC5-J11
G11	C6	DAI5	IC5-H10
G9	C7	DAI6	IC5-H11
F9	GND	GND	0V supply rail
F11	C8	DAI7	IC5-F10
E11	C9	DAI8	IC5-G10
E10	C10	DAI9	IC5-G11
E9	C11	DAI10	IC5-G9
D11	C12	DAI11	IC5-F9
D10	C13	DAI12	IC5-F11
C11	C14	DAI13	IC5-E11
B11	C15	DAI14:15	IC5-E9, E10
C10	OE		tie low
A11	BFP		N/C
B9	CO		N/C
A10	RA0		L on even cycles, H on odd cycles
A9	RA1		tie high
B8	RA2		tie low
A8	CI		tie low
B6	IA0		tie low
B7	IA1		tie high
A7	IA2		tie high
C7	IA3		tie low
C6	IA4		tie high

IC4: PDSP16318 - Real Path

Pin No.	Pin desc.	Net Name	Connections
B2	D7	B'R7	external o/p
C2	D8	B'R8	external o/p
B1	D9	B'R9	external o/p
C1	D10	B'R10	external o/p
D2	GND	GND	0V supply rail
D1	VDD	VDD	+5V supply rail
E3	D11	B'R11	external o/p
E2	D12	B'R12	external o/p
E1	D13	B'R13	external o/p
F2	D14	B'R14	external o/p
F3	D15	B'R15	external o/p
G3	C15	A'R15	external o/p
G1	C14	A'R14	external o/p
G2	C13	A'R13	external o/p
F1	C12	A'R12	external o/p
H1	VDD	VDD	+5V supply rail
H2	GND	GND	0V supply rail
J1	C11	A'R11	external o/p
K1	C10	A'R10	external o/p
J2	C9	A'R9	external o/p
L1	C8	A'R8	external o/p
K2	C7	A'R7	external o/p
K3	C6	A'R6	external o/p
L2	C5	A'R5	external o/p
L3	C4	A'R4	external o/p
K4	C3	A'R3	external o/p
L4	C2	A'R2	external o/p
J5	C1	A'R1	external o/p
K5	C0	A'R0	external o/p
L5	OED		tie low
K6	OEC		tie low
J6	SD2	SFTR2	IC1-E2 ; IC5-J6
J7	SD1	SFTR1	IC1-C1 ; IC5-J7
L7	SD0	SFTR0	IC1-E3 ; IC5-L7
K7	MS		tie low
L6	ASI1		tie high
L8	ASI0		tie low
K8	DEL		tie low
L9	CLR		tie low
L10	ASR1		tie low
K9	ASR0		tie low
L11	A0	DAR0	IC2-J11
K10	A1	DAR1	IC2-H10
J10	A2	DAR2	IC2-H11
K11	A3	DAR3	IC2-F10
J11	A4	DAR4	IC2-G10
H10	A5	DAR5	IC2-G11
H11	A6	DAR6	IC2-G9
F10	A7	DAR7	IC2-F11
G10	A8	DAR8	IC2-E11
G11	A9	DAR9	IC2-E10
G9	A10	DAR10	IC2-E9
F9	A11	DAR11	IC2-D11
F11	A12	DAR12	IC2-D10
E11	A13	DAR13	IC2-C11
E10	A14	DAR14	IC2-B11
E9	A15	DAR15	IC2-B11

IC4: PDSP16318 - Real Path (continued)

Pin No.	Pin desc.	Net Name	Connections
D11	CEA		tie low
D10	B15	PR15	IC1-B14
C11	B14	PR14	IC1-A15
B11	B13	PR13	IC1-A14
C10	B12	PR12	IC1-B12
A11	B11	PR11	IC1-C11
B10	B10	PR10	IC1-A13
B9	B9	PR9	IC1-B11
A10	B8	PR8	IC1-A12
A9	B7	PR7	IC1-C10
B8	B6	PR6	IC1-B10
A8	B5	PR5	IC1-A11
B6	B4	RP4	IC1-A10
B7	B3	PR3	IC1-A9
A7	B2	PR2	IC1-B8
C7	B1	PR1	IC1-A8
C6	B0	PR0	IC1-C8
A6	CLK	CLK	external i/p - common to all ICs
A5	CEB		tie low
B5	OVR		N/C
C5	D0	B'R0	external o/p
A4	D1	B'R1	external o/p
B4	D2	B'R2	external o/p
A3	D3	B'R3	external o/p
A2	D4	B'R4	external o/p
B3	D5	B'R5	external o/p
A1	D6	B'R6	external o/p

IC5: PDSP16318 - Imaginary Path

Pin No.	Pin desc.	Net Name	Connections
B2	D7	B'I7	external o/p
C2	D8	B'I8	external o/p
B1	D9	B'I9	external o/p
C1	D10	B'I10	external o/p
D2	GND	GND	0V supply rail
D1	VDD	VDD	+5V supply rail
E3	D11	B'I11	external o/p
E2	D12	B'I12	external o/p
E1	D13	B'I13	external o/p
F2	D14	B'I14	external o/p
F3	D15	B'I15	external o/p
G3	C15	A'I15	external o/p
G1	C14	A'I14	external o/p
G2	C13	A'I13	external o/p
F1	C12	A'I12	external o/p
H1	VDD	VDD	+5V supply rail
H2	GND	GND	0V supply rail
J1	C11	A'I11	external o/p
K1	C10	A'I10	external o/p
J2	C9	A'I9	external o/p
L1	C8	A'I8	external o/p
K2	C7	A'I7	external o/p
K3	C6	A'I6	external o/p
L2	C5	A'I5	external o/p
L3	C4	A'I4	external o/p
K4	C3	A'I3	external o/p
L4	C2	A'I2	external o/p
J5	C1	A'I1	external o/p
K5	C0	A'I0	external o/p
L5	OED		tie low
K6	OEC		tie low
J6	SD2	SFTR2	IC1-E2 ; IC4-J6
J7	SD1	SFTR1	IC1-C1 ; IC4-J7
L7	SD0	SFTR0	IC1-E3 ; IC4-L7
K7	MS		tie low
L6	ASI1		tie high
L8	ASI0		tie low
K8	DEL		tie low
L9	CLR		tie low
L10	ASR1		tie low
K9	ASR0		tie low
L11	A0	DAI0	IC3-J11
K10	A1	DAI1	IC3-H10
J10	A2	DAI2	IC3-H11
K11	A3	DAI3	IC3-F10
J11	A4	DAI4	IC3-G10
H10	A5	DAI5	IC3-G11
H11	A6	DAI6	IC3-G9
F10	A7	DAI7	IC3-F11
G10	A8	DAI8	IC3-E11
G11	A9	DAI9	IC3-E10
G9	A10	DAI10	IC3-E9
F9	A11	DAI11	IC3-D11
F11	A12	DAI12	IC3-D10
E11	A13	DAI13	IC3-C11
E10	A14	DAI14	IC3-B11
E9	A15	DAI15	IC3-B11

IC5: PDSP16318 - Imaginary Path (continued)

Pin No.	Pin desc.	Net Name	Connections
D11	CEA		tie low
D10	B15	PI15	IC1-C2
C11	B14	PI14	IC1-D3
B11	B13	PI13	IC1-C3
C10	B12	PI12	IC1-C4
A11	B11	PI11	IC1-A2
B10	B10	PI10	IC1-B3
B9	B9	PI9	IC1-C5
A10	B8	PI8	IC1-B4
A9	B7	PI7	IC1-A3
B8	B6	PI6	IC1-A4
A8	B5	PI5	IC1-A5
B6	B4	PI4	IC1-B6
B7	B3	PI3	IC1-B7
A7	B2	PI2	IC1-A6
C7	B1	PI1	IC1-A7
C6	B0	PI0	IC1-C7
A6	CLK	CLK	external i/p - common to all ICs
A5	CEB		tie low
B5	OVR		N/C
C5	D0	B'I0	external o/p
A4	D1	B'I1	external o/p
B4	D2	B'I2	external o/p
A3	D3	B'I3	external o/p
A2	D4	B'I4	external o/p
B3	D5	B'I5	external o/p
A1	D6	B'I6	external o/p

References

For a general introduction to FFTs the following texts are recommended:

1. Rabiner and Gold, 'Theory and Application of Digital Signal Processing', Prentice - Hall 1975

2. Oppenhiem and Shafer, 'Digital Signal Processing' , Prentice - Hall 1975

Other GEC Plessey Semiconductors applications notes and briefs of interest include:

AN47 'A Radix 2 Butterfly Processor'

AN49 'Complex Signal Processing with the PSDP16000 Family'

AN50 'A Fast FFT Processor using the PDSP16000 Family'

AB01 'A 50ns Butterfly Processor'

AB10 'FIR Filtering with the PDSP16112 and PDSP16318'

In addition, many PDSP devices and applications are modelled on the 'PDSP Demonstrator' software, intended to be run on IBM-PC or compatibles.

CONFIGURING THE PDSP16256

1. INTRODUCTION

The PDSP16256 is a digital finite impulse response (FIR) filter capable of providing between 16 and 128 digital filtering stages at sampling rates from 3.125MHz for a 128 stage filter up to 25MHz for 16 stages. The device contains 16 multiplier-accumulator circuits which are multi-cycled to produce filters of greater than 16 stages. Input data and coefficents are both represented by 16 bit two's complement numbers with coefficients converted internally to 12 bits.

The PDSP16256 is designed such that devices may be easily cascaded. This allows filter lengths to be increased above the nominal 128 stages offered by a single device. Cascading may also be used to raise the filter sampling rate in those cases where a single device is unable to offer the required performance. For example, a single PDSP16256, when configured as a 64 stage filter, offers a maximum sampling rate of 6.25MHz. Using two devices in cascade, each configured as a 32 stage filter, offers a sampling rate of 12.5MHz. Expansion buses ensure that no loss of accuracy occurs when devices are connected in this configuration. If a system contains a number of PDSP16256 devices which each comprise separate unrelated filters, the inherent cascading features of the device may still be used in order to allow all of the devices to be configured from a single EPROM, thereby simplifying the system design.

The PDSP16256 contains a single 16 bit control register which determines the mode and speed of operation, along with other control functions. The filter coefficients are 12 bits wide, with one coefficient being required for each stage of the filter.

The data presented to the 16 bit coefficient input bus is automatically rounded to yield a 12 bit coefficient during device configuration. The rounding scheme employed is described in detail in the PDSP16256 data sheet.

For filters with 64 (single filter mode only), 32 and 16 stages the PDSP16256 offers the coefficient bank swap feature. If enabled, bank swapping allows one set of coefficients to be replaced by an alternative set without the need to load these from an external source.

Before filtering operations may commence, it is necessary to load the device with both the filter coefficients and the control register word. This may be accomplished in one of two ways;

- by loading the data from a local memory device (e.g. EPROM)
- via a system data bus under the control of an intelligent master device (e.g. a microprocessor)

The former has the advantage of providing a stand-alone system which is able to load the required data on system boot-up whilst using the minimum number of external components. The latter allows much greater flexibility in the types of filtering systems which may be implemented. Remote master mode could be used, for example, to implement an adaptive filtering system in which the filter coefficients are changed, depending on prevailing conditions, thus maximizing the performance of the filter at all times.

This application brief gives detailed information which will allow users to determine how to interface to the PDSP16256 in order to load coefficient and control information. This brief covers the use of the device in both automatic EPROM load and remote master modes. Information on cascading devices in both modes is also included.

2. TIMING

The PDSP16256 uses registers on all inputs and outputs to ensure that signals are synchronous with the system clock. This scheme ensures that all setup and hold times for incoming signals are the same. Similarly, all clock to data valid delays for output signals are also identical.

The PDSP16256 datasheet in this handbook lists these delays for the PDSP16256 as :

Parameter	Min	Max
Input signal setup	8	-
Input signal hold	4	-
SCLK to output valid	5	26

(All times in nanoseconds)

There is an exception to this rule; the output circuitry. Here, the delay from activating the output enable to the data being available on the pins is not the same as the value given above for other output signals. Similarly, the delays in changing from a high- to a low-impedance output state, and vice-versa, are also different. The values of these delays may be found by referring to the DSP IC Handbook.

3. AUTOMATIC EPROM LOAD MODE

The PDSP16256 generates all the required signals to interface directly to an EPROM and load the required data automatically without the need for external glue logic in this mode. Tying the EPROM input to ground selects this mode of operation. It is assumed that all data loaded consists of 8 bit bytes. The data load sequence is initiated by the RESET input to the PDSP16256. RESET, which is active low, should be held low for 16 cycles of the system clock, SCLK. After the sixth SCLK cycle, the BUSY signal will go high, signalling to other devices in the system that the PDSP16256 is performing a data load function. All output data is invalid while the BUSY signal is active. BUSY returns to its inactive state once all the required coefficient and control register data has been loaded.

The address bus used to access the EPROM is 8 bits wide. This allows a maximum of 256 data bytes to be read. For a digital filter containing the maximum 128 stages, 256 bytes will be required to store the coefficients as each one requires two bytes of storage. The byte held in the lower address of each byte-pair should be the least significant byte. If a smaller filter is to be implemented, 32 taps for example, then some of the address lines are redundant and will remain low at all times. These redundant address lines should not be connected to the EPROM when a number of PDSP16256 devices are to be cascaded. A further two bytes are required to store the 16 bit control register word. The control word always resides above the filter coefficients in the EPROM memory map.

The coefficient control pin, CCS, is used to determine whether the control register or filter coefficients are to be loaded. When CCS is high, the control register is loaded and when low, the filter coefficients are loaded. CCS is effectively used as the most significant address line in addition to the address bus A7:0. Hence, when CCS is high, the EPROM address that will be referenced is 256+A7:0, assuming that all eight address lines are in use. In order to load the control register, A7:0 takes the values 0 and 1 whilst CCS is held high, thereby accessing addresses 256 and 257 in 128 stage filter systems.

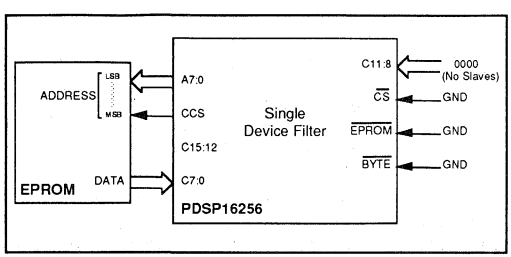


Fig.1 Diagram of standalone EPROM system

Once the control register has been loaded, A7:0 starts counting upwards from address 0. As CCS has now returned low, the EPROM addresses will be in the range 0 to 255. Bits 12, 13 and 14 of the control register define the number of digital stages in the filter and whether the decimate option is enabled. This defines the number of coefficients required and is used to regulate the number of bytes loaded from the EPROM. Every 4 SCLK cycles a new address is generated and a new byte loaded using the 8 least significant bits of the coefficient input bus, C15:0. If only one PDSP16256 device is contained in a filtering system (i.e. devices are not being cascading), then bits C11:8 should all be tied to ground and C15:12 should be left unconnected. The reasons for this will become apparent after reading section 3.2.

3.1 Timing Information

Each address is held on the A7:0 outputs for four SCLK cycles. On the fourth cycle, the data presented to the lower 8 bits of the C15:0 input bus is loaded into the device. Using this information the type of EPROM required to correctly interface to a PDSP16256 may be specified.

The EPROM access time is calculated by subtracting the output delay between SCLK and A7:0 and the setup time required to correctly load data into the PDSP16256 from four SCLK periods. Hence,

EPROM Access Time = 4.T - Output Delay - Setup Time

(where T is the SCLK period)

We know that the output delay has a maximum value of 26ns and that the setup time is 8ns. Therefore,

EPROM Access Time = 4.T - 26 - 8 = 4T - 34

For a typical application where SCLK is running at 25MHz (T=40ns), it can be seen that the EPROM access time will be 126ns. This means that to correctly load data with SCLK running at 25MHz, an EPROM with an access time of 126ns, or less, is required.

3.2 Cascading devices in EPROM mode

An arbitrary number of PDSP16256 devices may be cascaded to form a given filtering system. However, only a maximum of 16 devices may access the same EPROM to load configuration data. Hence, if more than 16 devices are to be cascaded, these should be subdivided into blocks of 16 for configuration purposes, with each 16 device block having access to a separate EPROM.

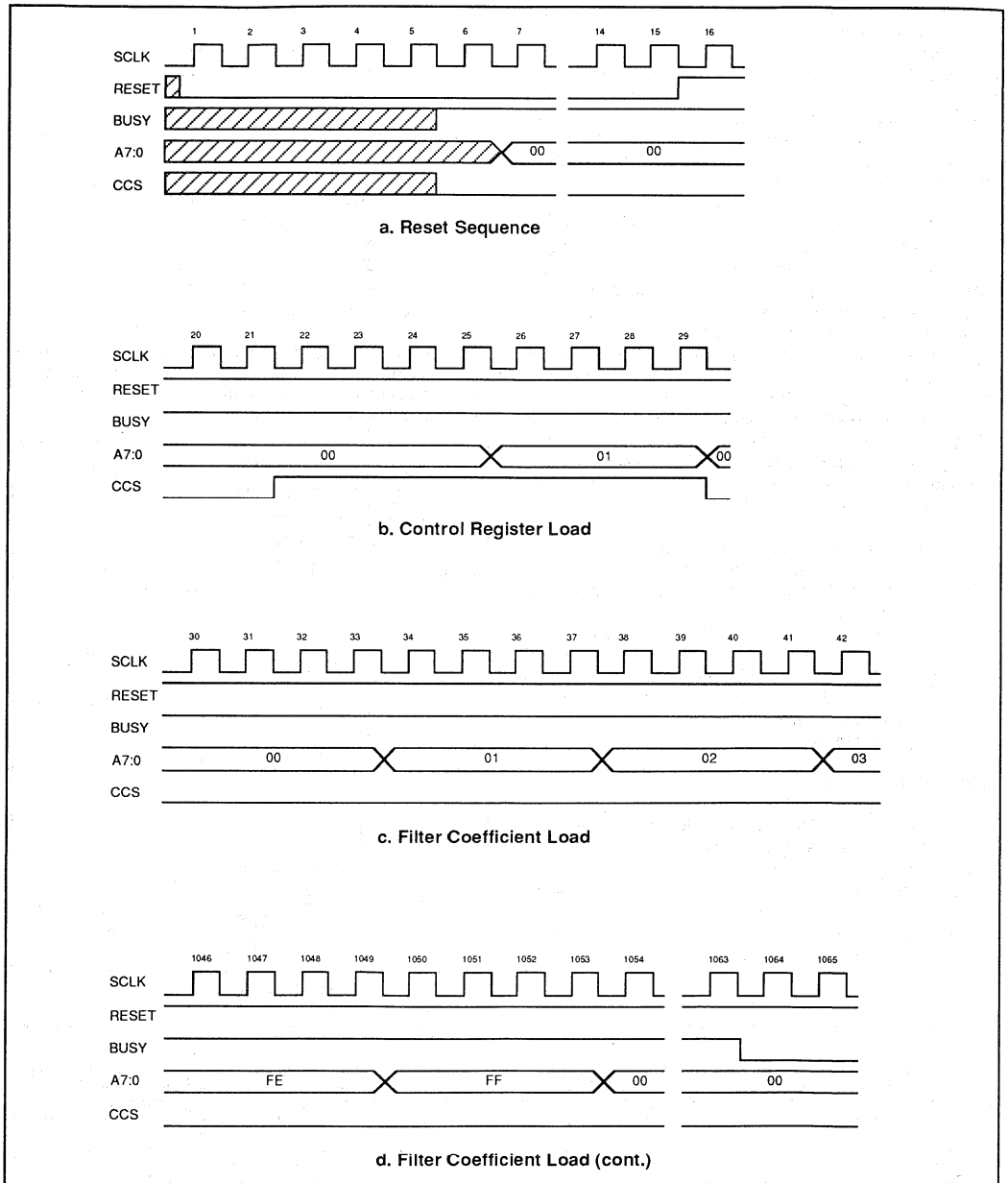


Fig.2 Reset & coefficient load sequences.

When several devices are connected in cascade, one of these devices is nominated the master (this should not be confused with a remote master discussed elsewhere in this application brief). The master device is responsible for controlling the loading of data for all devices to which it is connected. The master is identified by the fact that its EPROM input is grounded; all other cascaded devices, termed slaves, have their EPROM inputs connected to +5V. The master provides address, Write Enable, CCS and device decoding signals for all slave devices as well as for itself.

Only 8 of the 16 bits of the coefficient input bus, C15:0, are used in automatic EPROM load mode. The remaining eight lines are used to provide device decoding information. These signals help pass the required coefficient and control data to the correct device under the control of the master. The four bits C11:8, which are programmed as inputs on both slave and master devices, are used to assign a unique code to each slave. The first slave should have C11:8=0001, the second, C11:8=0010 and so on. The master device is therefore implicitly labelled 0000. The master uses C11:8 inputs to identify the total number of slaves contained in the cascaded system. If four devices are to be cascaded, for example, these will comprise one master and three slaves. Therefore, the C11:8 inputs on the master would be set to 0011.

The four bits C15:12 are programmed as outputs on the master and inputs on all slaves. Only when the value indicated on C15:12 is equal to the slave device code defined by C11:8 will the slave in question load the data passed to it via the coefficient input bus. This arrangement effectively provides a unique decode signal for each slave device in turn. The Chip Select signal, CS, should be tied to ground on all devices; slaves and master. C15:12 are used in conjunction wth A7:0 and CCS to access different pages of the EPROM, as shown by the timing diagram, fig. 4.

3.3 EPROM Memory Requirement

When the PDSP16256 loads coefficient data, if the filter length is such that bank swapping is possible, the device will always attempt to load a second bank of coefficients, irrespective of whether the bank swapping option has been enabled in the control word or not. Hence, in single filter mode, the amount of EPROM space required for each of the filter lengths, in bytes, is:

Filter Length	EPROM Space
128	512
64	512
32	256
16	128

In dual filter mode, the EPROM memory requirements are as follows:

Filter Length	EPROM Space
64	512
32	512
16	256
8	128

If n devices are connected in cascade, with each device implementing the same size of filter, then the EPROM space required is simply the product of the space required by a single device and the number of devices.

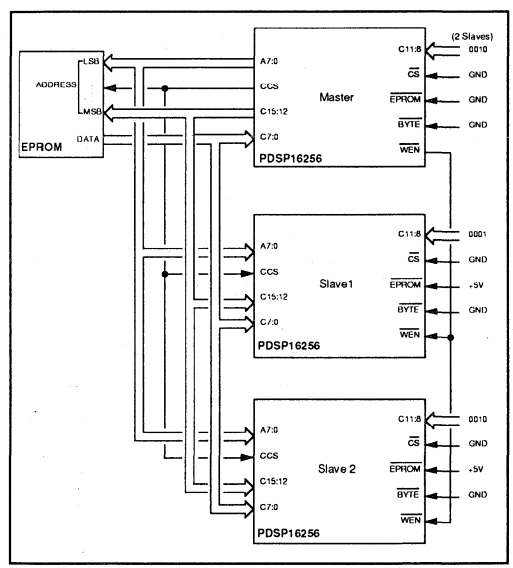


Fig.3 Cascaded system

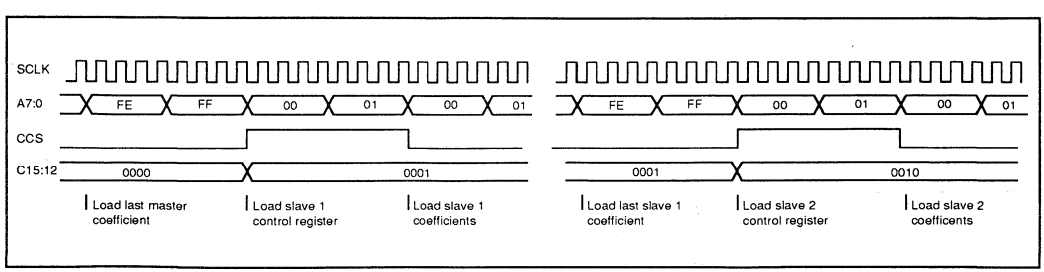


Fig.4 Load sequence for a cascaded system

Consider a system which contains four devices each of which contains a single 128 stage filter. In order to configure all four devices, an EPROM containing a total of

$$4 \times 512 = 2048 \text{ bytes}$$

will be required. The memory map for this EPROM is shown in Fig.5. The diagram shows the values of C15:12, CCS and A7:0 required to access each different area of the EPROM.

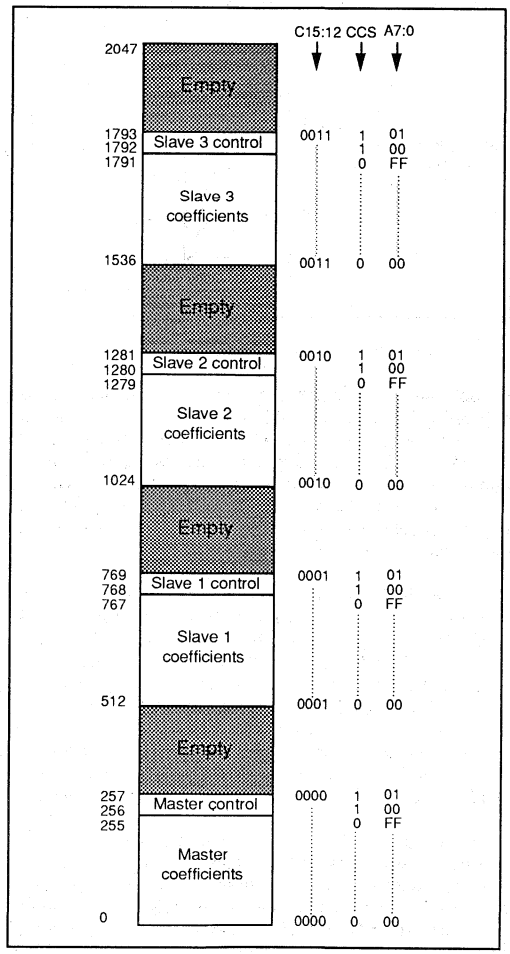


Fig.5 EPROM memory map for a four device system

4. REMOTE MASTER MODE

In this mode, the remote master, is charged with supplying the address and data buses to the PDSP16256 via a synchronous peripheral interface. This mode allows all or selected coefficients to be updated under the control of the remote master whenever conditions dictate. Remote master mode is selected by tying the EPROM input pin of the PDSP16256 to +5V.

A filter initialisation sequence, where both the control register and filter coefficients are loaded, is initiated by a RESET sequence. RESET should be held low for 16 cycles of SCLK. After the sixth SCLK cycle the BUSY signal goes high, indicating that the device is performing internal initialisation operations. BUSY will remain active for 31 SCLK cycles. Only when it goes low can data be written to the device. A RESET sequence, as described above, is not needed when filter coefficients alone are to be updated.

When valid data appears on the address and data bus, this data is written to the PDSP16256 by the application of synchronous Chip Select (CS) and Write Enable (WEN) signals. Data may be written to the PDSP16256 either in 8 bit bytes or 16 bit words, the data width being selected by the BYTE input pin.

If BYTE is tied low, data is loaded as 8 bit bytes, and if high, as 16 bit words. The comparison that is made in automatic EPROM load mode between C15:12 and C11:8 is also made in byte mode, irrespective of the fact that remote master mode is selected. Hence, to satisfy this comparison, pins C15:8 should all be tied to ground when using 8 bit data transfers. In byte mode, the least significant byte (which is accessed when A0=0) should be written first, followed by the most significant (accessed when A0=1). If the device is operating in byte mode, it is necessary to hold CS low for an extra two SCLK cycles once all the coefficients have been loaded. This can be clearly seen in fig. 8c.

When 16 bit words are used, a maximum of 128 transfers are required to load all the required filter coefficients. Hence, only 7 address lines are needed and A7 is therefore redundant in word mode. Unlike automatic EPROM load mode, new data may be written to the device on every SCLK cycle, if required, as long as the timing constraints are honoured.

As with automatic EPROM load mode, the control register should be loaded first, followed by the filter coefficients. A delay of at least two clock cycles needs to be inserted after the control register has been loaded and before any filter coefficents are written to the device. CS needs to be held low for a total of three clock cycles when loading the control register, as shown in fig. 8a. CCS becomes an input to the PDSP16256 in this mode and, when high, indicates that a load to the control register is to take place. Hence, as with automatic EPROM load mode, CCS is used as the most significant address line in conjunction with A7:0. The filter coefficients may be addressed at random, i.e. they need not be loaded in address order, and an arbitrary number may be modified under the control of the remote master at any time. It must be borne in mind that one of the effects of loading new coefficients will be that mathematically correct results will not

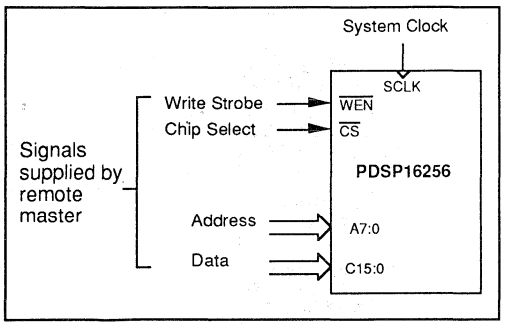


Fig.6 Remote Master standalone system

be obtained for a number of cycles, the exact number depending upon which coefficients were modified and the length of the filter. This is due to the effect of partial results, calculated using the old coefficients, being propagated through the device. It is not recommended that the control register be modified whilst the device is operating. The control register should only be loaded after a reset sequence, as described above.

The PDSP16256 is a synchronous device. This means that all external signals are assumed to be synchronous to the system clock. In general, the remote master's Write Enable and Chip Select signals will be asynchronous to the PDSP16256 system clock. Hence, the signals supplied to the PDSP16256 should be synchronised to SCLK and care taken to ensure that all setup and hold times are honoured. Double buffering the signals generated by the remote master, as shown in fig. 7a, will ensure that these constraints are met, whilst at the same time minimizing metastability problems.

The diagram below shows one possible implementation of a system that will ensure that all timing constraints are met when operating in remote master mode. The coefficient load state machine is used to generate the WEN and CS signals. As can be seen in fig. 7b, WEN is low only for the required one clock edge period. In more complicated systems this state machine could be used to perform other functions such as device decodes etc.

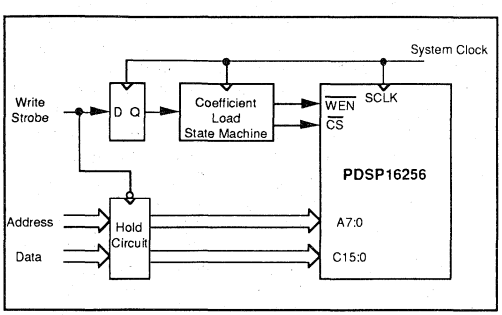


Fig.7a Remote master interface

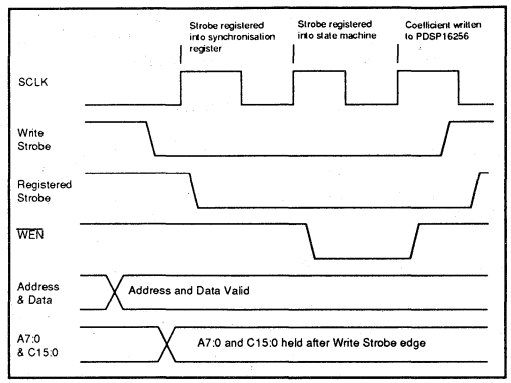


Fig.7b Remote master signal synchronisation

4.1 Timing

Figs. 8a and 8b show the setup and hold constraints which must be met if data is to be loaded correctly. The setup and hold time values are as listed in section 2 above. Fig. 9 shows examples of reset and load sequences for both byte and word modes.

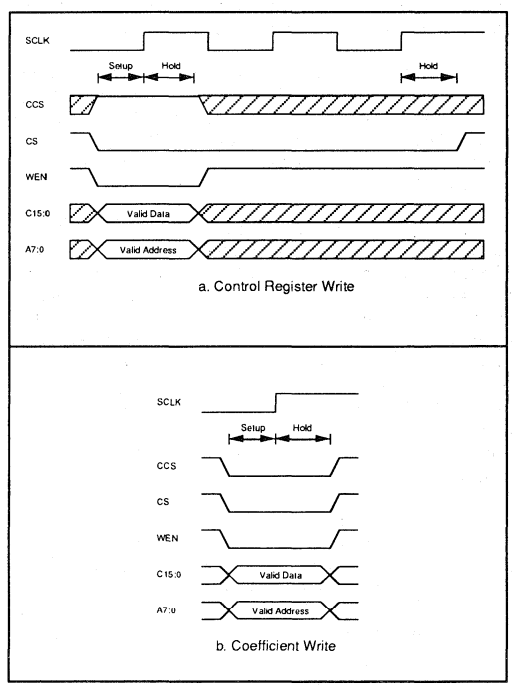


Fig.8a,b Remote master timing constraints

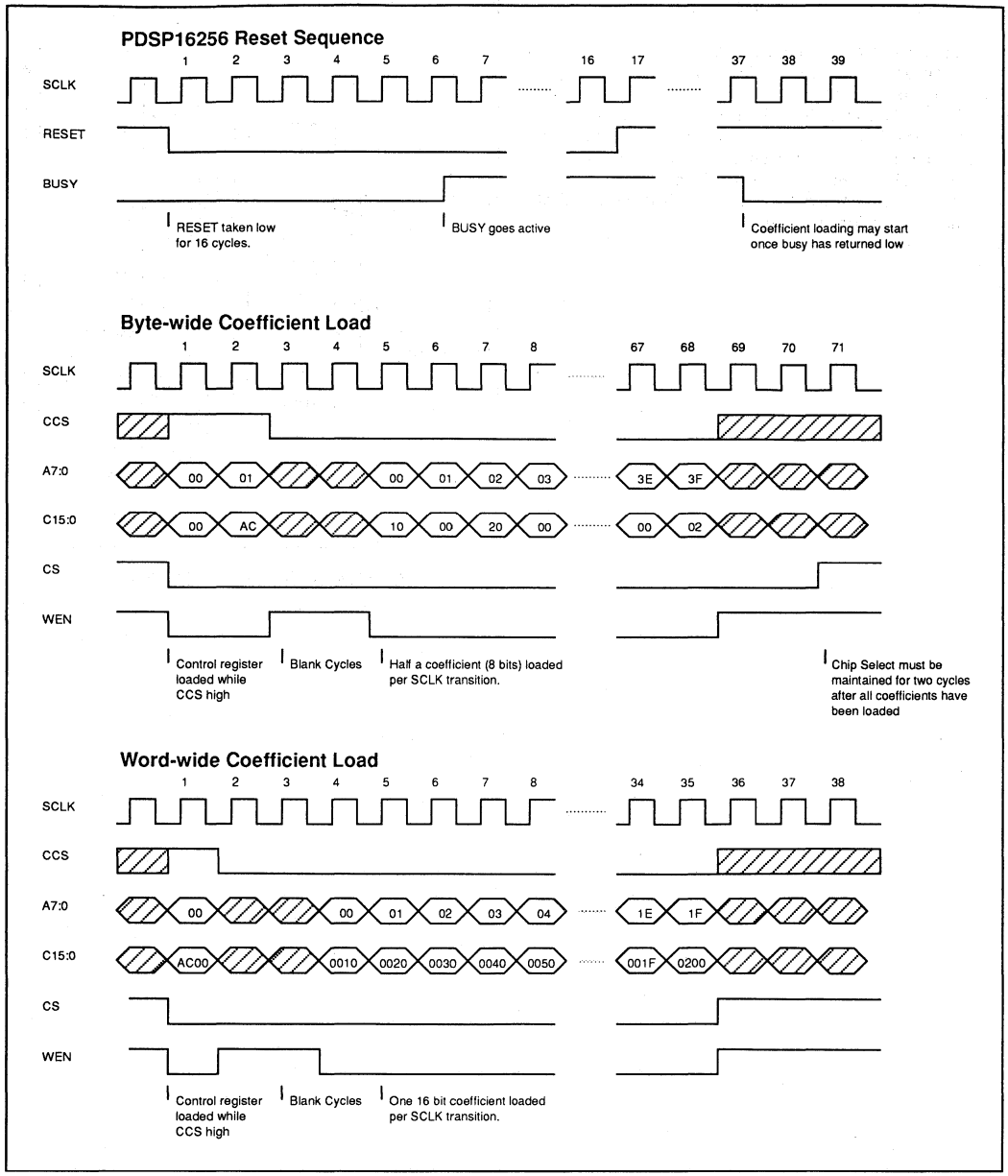


Fig.9 Reset & coefficient load sequences

4.2 Cascading in Remote Master mode

When devices are cascaded in this mode, the master-slave distinction that is evident in automatic EPROM load mode is not necessary as all devices are treated in the same way. Chip Select and Write Enable signals are used to selectively enable the required device and to write to it the relevant data. In many ways, the method used to write data to a series of PDSP16256 devices is analogous to the process of writing to a bank of RAM devices. Fig. 10 shows a typical cascade configuration for this mode.

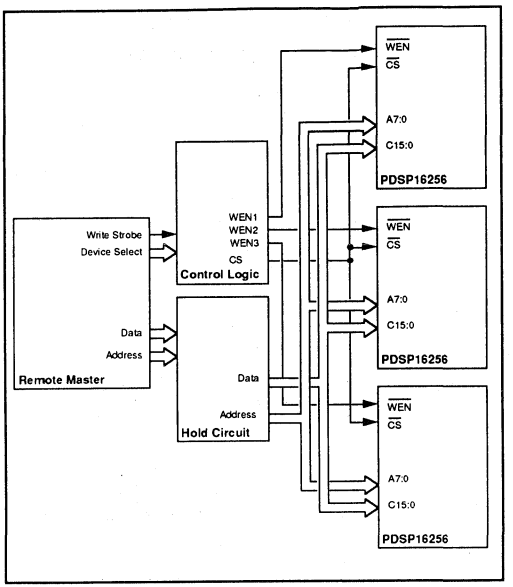


Fig.10 Cascaded remote master system

DIGITAL FILTERING USING THE PDSP16256

INTRODUCTION

In the field of high performance filtering, engineering solutions are making increasing use of digital techniques. Digital filters are known to typically offer improved accuracy, complete predictability, flexibility and performance improvements. They are also highly suitable for integration with modern CAD tools and techniques, thus reducing development times and simplifying the design process.

General purpose DSP processors can implement digital filters with sampling rates upto approximately 250kHz, but until recently sampling rates beyond this threshold required complex custom design. However the latest CMOS design techniques now enable dedicated standard parts of the necessary speed and complexity to be fabricated, rendering custom designs obsolete.

WHAT ARE DIGITAL FILTERS?

'When a signal that is sampled in time and quantized in amplitude is processed such that the spectral characteristics of the signal are altered in a controlled manner then the resulting operation is termed digital filtering'.

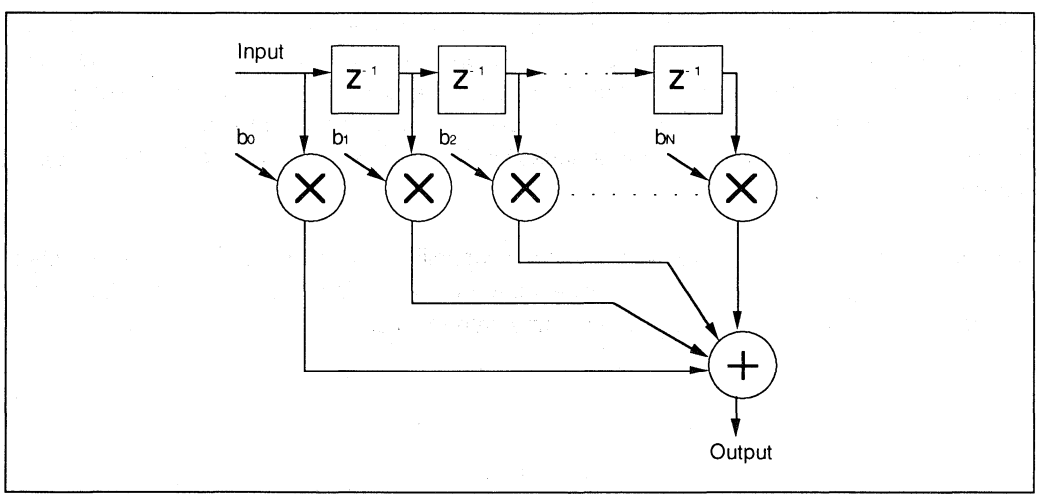


Fig 1 FIR Filter Structure.

Digital filters fall into two groups, those with infinite impulse response (IIR) and those with finite impulse response (FIR). The main difference between these two types is that the output from an FIR filter may be calculated from only current and previous inputs, whereas the output of an IIR filter depends on previous output states as well. Although IIR filters may be designed to be more efficient than an FIR for a given filter order, consideration must always be given to the stability of any design. FIR filters on the other hand, are inherently stable, are generally easier to design and implement in hardware and have the additional advantage that they may be designed such that they are free of phase distortion (i.e. constant group delay).

The output, y_n of an FIR may be calculated as the convolution of the input samples with the filter impulse response and can be represented by a difference equation such as:

$$y_n = b_0x_n+b_1x_{n-1}+.....+b_{N-1}x_{n-N+1}$$

or more generally:

$$y(n) = \sum_{k=0}^{N-1} h(k).x(n-k)$$

where coefficients b_k represent the N samples of the impulse response, h(k), of the desired filter.

WHAT IS THE PDSP16256?.

The PDSP16256 is a single chip FIR filter solution that is capable of operation at sample rates upto 25MHz. Internally it is arranged as two banks of eight multiplier/accumulators that are configurable in a number of ways. Each bank can be configured as a filter of 8, 16, 32, or 64 taps each doubling in length resulting in a halving of the maximum sample rate. The banks can be internally arranged as one single long filter, 2 independent filters, or 2 filters in connected in series. In addition a decimate option allows the output sample rate to be half the input sample rate, thus doubling the filter length. This mode ideal for low pass filter implementations since the high frequencys present in the input can be removed so the output still satisfies Nyquist's sampling criterion.

If the realization of the desired filter is beyond the capabilities of a single device then a number of devices in single filter mode can be cascaded to produce a filter with more taps, due to the provision at external pins of the full 32bit intermediate results.

DEVELOPMENT SYSTEM

A complete development system for the PDSP16256 is available from ERA Technology Ltd, consisting of a software package for filter design specifically tailored to the operating modes of the device and an IBM PC compatible board and control software.

The design package uses special procedures to quantize the filter coefficients in such a manner as to ensure an optimal filter response, given the internal bit accuracies. Low pass, high pass, Hilbert, delay, bandpass or bandstop filters are all supported. The user is given the option to leave any one of the filter design parameters free, and the software then determines this free parameter using the remaining specified parameters. Thus, for example, when designing a low pass filter the user can fix the number of taps to suit the maximum provided by the PDSP16256 at the required sampling rate. Either the transition band, pass band ripple, or stopband attenuation can then be left free, and the software will determine the best that can be achieved for that parameter, given the parameters which are fixed.

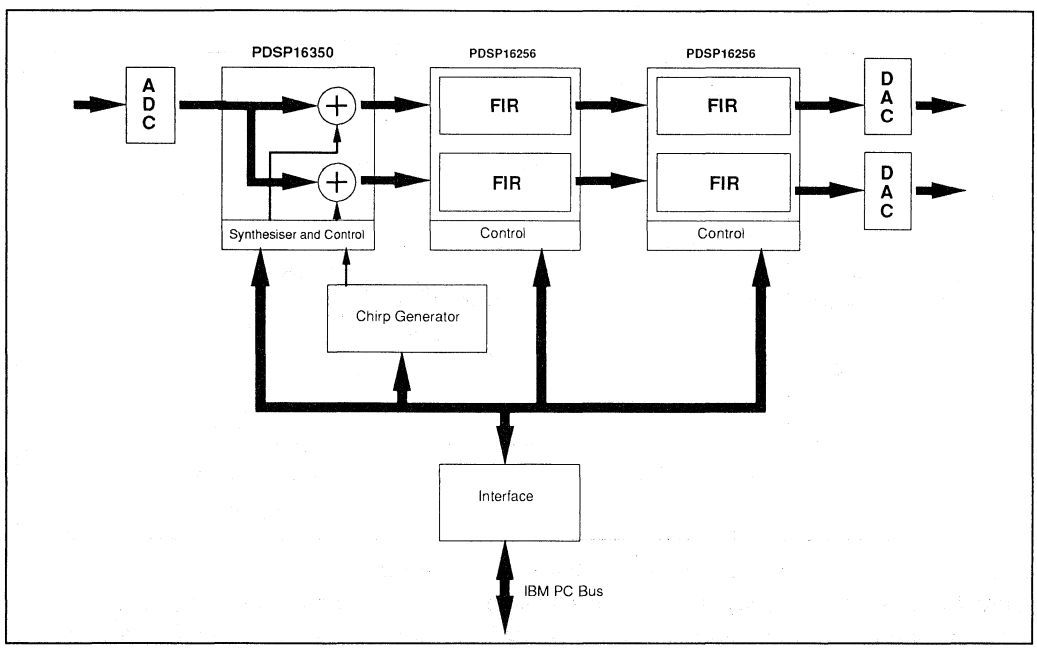


Fig 2 Schematic of Development Board.

The development board is arranged as shown in diagram 2. Digitization is undertaken using either a 20MHz eight bit ADC or a 1MHz twelve bit ADC. A quadrature mixing operation may be applied prior to filtering by means of a PDSP16350 I/Q splitter and numerically controlled oscillator. The

digital filtering itself is undertaken using either one or two PDSP16256's. This configuration enables filters of upto 256 coefficients to be implemented using 16-bit data. It also provides the capability for cascaded filtering stages, or for two completely separate filters. The latter would be needed if the complex mixing option is in use. The output signal is available in digital form and in analogue form via dual 12-bit DAC's. The software supplied for the board controls configuration, enables loading of coefficients and can synthesize various waveforms.

EXAMPLES OF FILTERS IMPLEMENTED ON THE PDSP16256

The following filters are designed on the IBM PC design software and show in detail some of the performance characteristics achievable with the PDSP16256.

Figure 3 shows the frequency response of a 128 tap low pass filter designed for a cutoff frequency of 0.1 of the sampling frequency. As implemented on a single PDSP16256, configured in single filter, decimating mode, it exhibits a stop band rejection characteristic approaching -50dB.

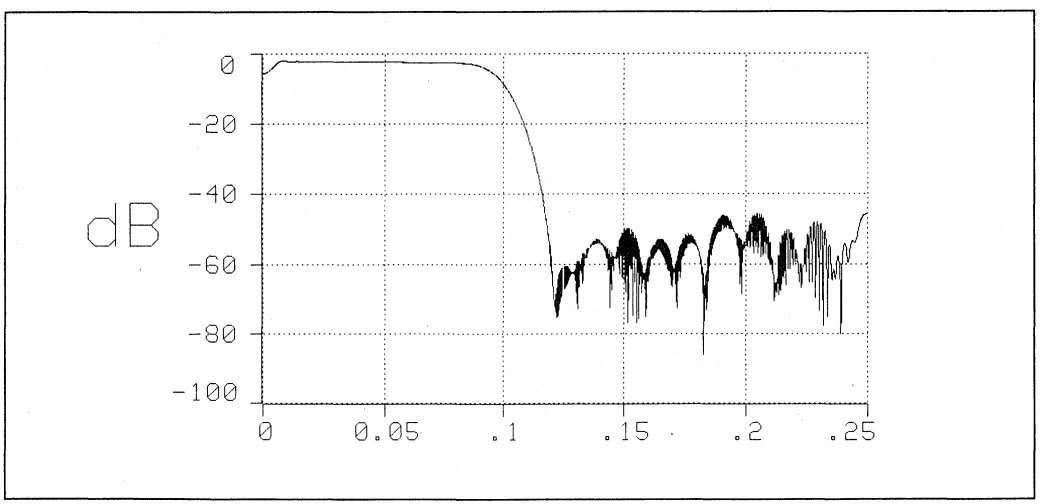


Fig 3 128 Tap Lowpass Filter on Single PDSP16256.

Figure 4 shows the frequency response of a filter designed to the same specification as the one shown in figure 3, but implemented as two 64 tap filters in series, again using a single PDSP16256.

It is clear that the series solution offers a much greater stop band rejection in practical applications but only as a trade off against the width of the transition band and at the expense of greater passband ripple.

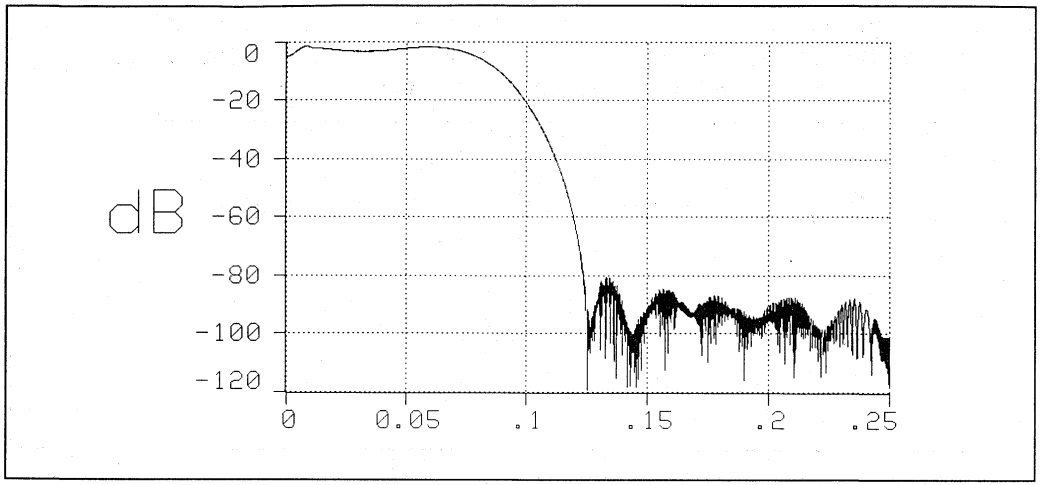


Fig 4 128 Tap Lowpass Filter Composed of two 64 Tap Filters in Series.

Figure 5 Illustrates the implementation of a narrow notch filter on a PDSP16256.

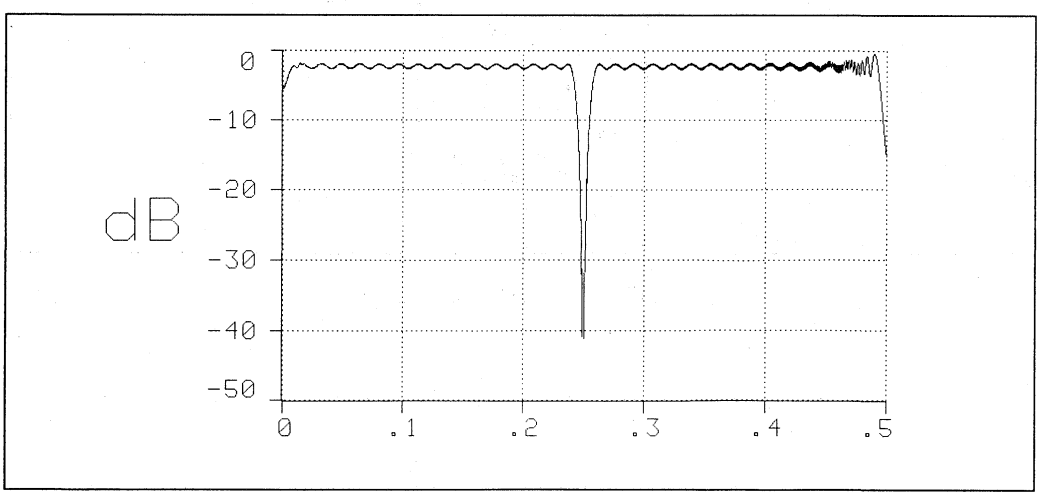


Fig 5 128 tap Bandstop Filter on a PDSP16256.

PRACTICAL SYSTEM CONFIGURATIONS

The PDSP16256 is designed with flexible interfacing characteristics to enable its use in a wide variety of system configurations. At it's simplest it can be configured to auto load the filter

coefficients directly from EPROM on power up and be directly connected to ADC's and DAC's (figure 6). Alternatively it could be configured as a dedicated co-processor for a general purpose programmable DSP processor with the DSP device controlling the PDSP16256 configuration, an architecture ideal for adaptive filtering applications for instance (figure 7).

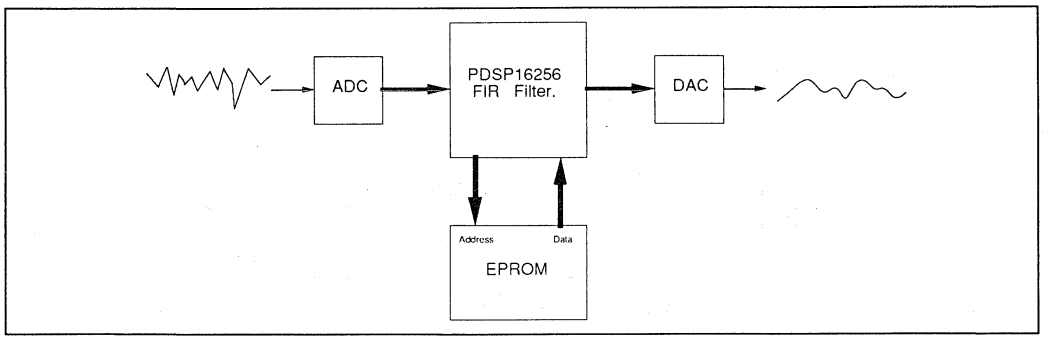


Figure 6 Simple Auto Load Configuration.

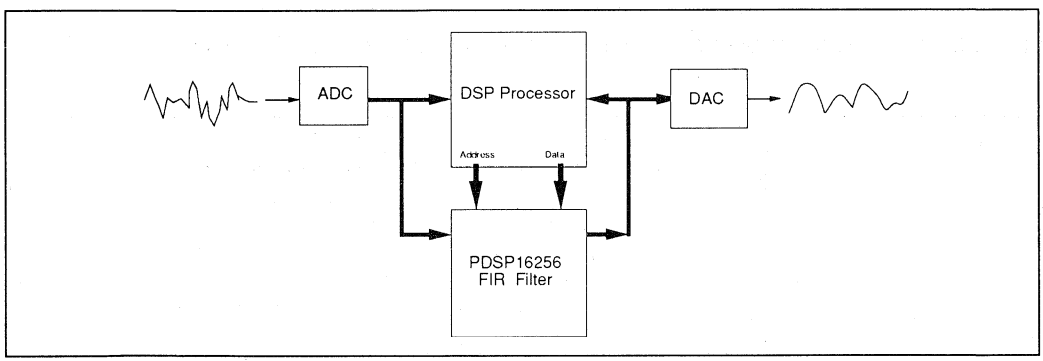


Figure 7 Slave Processor Configuration.

UTILISING THE "PDSP16256 FILTER DESIGN PROGRAM" FOR EXTERNALLY CASCADED FILTER CONFIGURATIONS

1.0 BACKGROUND

To help digital filter designers a program has been developed which generates the filter coefficients and allows software modeling of the filter response. This program (called the "PDSP16256 Filter Design Program") prompts designers for the system characteristics and filter design criteria, and computes the best coefficients to implement the desired filter characteristics. Unfortunately this software only works for single '256 designs and does not (directly) support multiple '256 designs using external cascading. For designers wanting a digital filter with tap length longer than that which is supported by a single device, there is no easy way to generate coefficients. This application note describes a way to use the filter design program for externally cascaded filters up to 128 taps long.

A single PDSP16256 (or PDSP16256A) FIR filter device (hereafter collectively called the '256) can be configured as a single filter, dual independent filters, or dual independent filters which are internally cascaded. For each of the configurations the maximum filter length (i.e. "taps") is determined by the ratio of the input and output sample rates to the system clock rate. The limitation is due to the fixed number of multiply/accumulate subsections in the device, and the need to multicycle them as the filter length is increased. The data sheet has tables identifying the maximum number of taps for sample rates in single filter mode (ref. Table 3, P. 126) and in dual filter mode (ref. Table 4, P. 128).

When additional tap length is required for a given input sample rate, multiple '256's may be externally cascaded together. There is no limit to the number of '256 devices which may be cascaded, although maintaining the overall numeric precision and avoiding arithmetic overflow needs to be carefully considered when cascading. To implement an external cascade of '256 devices, each device is programmed as a "single" filter (the "dual" and "cascaded" modes of operation are not supported when externally cascading).

2.0 THEORY

When executing the design program, two DOS files are generated to keep the filter characteristics, coefficients, and '256 configuration information. By editing one of the two files, it is possible to force the coefficient generating subroutines and filter output plotting routines to run with longer tap length filters than normally can be used in a single device. This technique will work up to the software limit of the compiled program, which is 128 taps.

To use the filter design program, start by typing "DESIGN" in the directory where the program was installed. As the software loads into memory, it will prompt you for a design file name (hereafter referred to as "<filename>") allowing the filter characteristics to be saved. The file name displayed is "FILTERxx" (where xx can be numbers or letters, but by default are nulls). Most designers enter their own eight (8) character DOS file name to provide some indication of what the filter characteristic is. Entering unique filenames allows previous filter simulations to be recalled, or evaluations of filter characteristic tradeoffs to be completed and compared to each other. Resulting calculations from the filter design program are stored in two external files using the specified file name, with .DSP and .COE extensions.

The <filename>.DSP file is an ASCII text file containing six data items. The first five items are the filter hardware characteristics. These are entered by the filter designer, and the values are stored on the first five lines (in the order shown below). The sixth line contains the calculated maximum number of filter taps, which is inserted by the program. The file is shown below, with available choices and the defaults:

LINE	DESCRIPTION	CHOICES	DEFAULT
Line #1	Device Type	PDSP16256 or PDSP16256A	PDSP16256
Line #2	Clock Rate (in Mhz)	Up to 20 for the PDSP16256, or up to 25 for the PDSP16256A	20 (PDSP16256) or 25 (PDSP16256A)
Line #3	Input Sample Rate	Clock rate $\prod$ (1,2,4,8)	Clock rate $\prod$ 1
Line #4	Filter mode	Single, Dual, Cascade	Single
Line #5	Decimation by 2	Off (0) or On (-1)	Off (0)
Line #6	Maximum # of taps	Calculated by program	Max. possible

Table 1.

This file limits the number of taps in the "Edit Design Parameters" section of the filter design program. Filter designers may enter any number of taps up to and including the maximum number specified in the .DSP file, but not more. If a number in excess of the maximum allowable is entered, the software merely returns the previously displayed value. By editing the sixth line of the <filename>.DSP file to be equal to the desired number of total taps, the program can be tricked into calculating coefficients for externally cascaded configurations up to 128 taps (regardless of input sample rate and system clock rates). Coefficient information (which is stored in the <filename>.COE file) may then be extracted so the proper coefficients will be placed into the appropriate cascaded digital filter device.

3.0 IMPLEMENTATION

To design a filter using externally cascaded devices with up to 128 taps, the following steps should be taken:

1. Run the filter design program by typing "design" in the installed directory.
2. Enter a carriage return, then a filter design file name up to eight characters long.
3. Enter information about the clock rate, and input sample rate. Specify the filter mode to be "single". Select whether decimation is desired or not.
4. Select "Main Menu" then "Quit" to exit the program.
5. Use an editor to edit the resulting <filename>.DSP file (which the program generated). Change the last line of the file to be the number of taps you would like to have, up to and including 128.
6. Restart the filter design program by typing "design" again.
7. Enter a carriage return, then enter the file name of the file you just edited.
8. Select the "Filter Design" option, then the "Design Filter" option.
9. Enter the filter type (lowpass, highpass, bandpass, bandstop, hilbert transform, or delay).
10. Edit the "frequency template" information. Remember that the cutoffs are expressed as a percentage of F_S.
11. Select "Edit Design Parameters", and select which of the design parameters the software should calculate. This is called the "free parameter".
12. Specify the remaining filter design parameters.
13. Select "Calculate Coefficients" to generate the coefficients.
14. It may require several iterations of steps 10 - 13 to generate coefficients. If the software indicates it's "Unable to generate coefficients" the specifications desired are too severe for the specified number of filter taps. Either simplify the filter parameters, or increase the number of taps (using the technique presented here) up to a maximum of 128, and try again.
15. After coefficients have been generated, spectral response can be viewed by selecting the "Plot Response" button on the screen. Frequency domain, impulse response, and step response graphs are the options.

When the filter characteristics desired have been achieved, exit the program and edit the <filename>.COE file. In this file, the design parameters and coefficients are stored. The format for this file is as follows:

- Line #1 - Filter type, represented by number as indicated below:
  0. Delay
  1. Lowpass
  2. Highpass
  3. Bandpass
  4. Bandstop
  5. Hilbert Transform
- Line #2 - Cutoff frequencies 1 & 2, expressed as a percentage of F_S.
- Line #3 - Four values separated by spaces (20h), indicating the following (in order below):
  1. # of filter taps used in solution (up to 128 max.)
  2. Transition width.
  3. Pass band ripple.
  4. Stopband attenuation.
- Line #4 - Coefficients, starting with the first, separated by spaces (20h).
- Lines #5 to #8 - Place holders for similar information when doing dual filter designs. Do not alter the information (mostly zeros) in these lines when doing an externally cascaded filter design.

The coefficients to be used will be found on the fourth line, separated by spaces (20h). These coefficients may then be manually partitioned into the '256 devices in your design to achieve the overall filter characteristic at the desired input sample rates.

4.0 EXAMPLE

We want to digitally process the information which is modulated onto the color subcarrier frequency used in NTSC televisions. Our application requires processing of the luminance information. We are not particularly concerned about processing the chroma signal, for it is being handled by a separate chroma circuit. To do the luma processing we need to extract 400 Khz of the color subcarrier, centered at 3.58 Mhz. The input has been sampled previously at 14.3 Mhz, and the 14.3 Mhz clock is available. The filter design criteria are as follows:

- System clock rate of 14.3 Mhz
- Input sample rate of 14.3 Msamples / second.
- A bandpass filter is to be developed, with the following design criteria:
  1. Pass band center frequency of 3.58 Mhz (color subcarrier frequency).
  2. Bandpass width of 400 Khz (desired bandwidth of modulated data).
  3. Stopband attenuation of -50 dB or better.

4. 100 milli dB of pass band ripple.
5. 1.3 Mhz transition width (maximum)

With the 400 Khz bandwidth desired, the values for cutoff frequency #1 and cutoff frequency #2 can be determined to be 3.58 Mhz ± 200 Khz. This gives us 3.38 Mhz for cutoff #1, and 3.78 Mhz for cutoff #2. To avoid aliasing the input sampling rate should exceed the highest frequency signal present by a factor of 2. With cutoff #2 at 3.78 Mhz, that means the Nyquist sampling rate must be greater than 7.56 Mhz. Options for setting up the '256 device include specifying the input sample rate equal to the system clock rate, or divided by 2, 4 or 8. The only option to avoid aliasing will be to design the system to use the '256 in a non-decimating, input sample equal to the system clock configuration.

To get the stopband attenuation, pass band ripple and 400 Khz pass band width will require more than 16 taps, which is the limit using a single '256 device. To determine the total tap length required of our digital filter we can experiment with the filter design program. We begin by executing steps 1-10 in the listing above (for step #5 pick 128, for step #9 choose "Bandpass", for step #10 put the 2nd cutoff frequency at .264 and the 1st cutoff frequency at .236). You'll notice (after pressing <esc>) that the picture of the filter frequency response at the top left of the screen changes to a narrow bandpass. At step #11, allow the "Transition Width" to be the free parameter. Specify 128 for the # of taps, 100 for the pass band ripple, and -50 for the stopband attenuation. Selecting "Generate coefficients" will now produce a set of coefficients for a 128 tap filter. To determine how many taps are actually required to implement this function, return to the "Design Filter" section, and begin reducing the number of taps. When the tap length is reduced below the amount required, the software will be unable to generate the coefficients. Multiple passes through the program will prove 78 taps are required.

In single filter mode with sample clock equal to system clock and no decimation the maximum number of taps achievable in a single device is 16. For a 78 tap filter, 5 cascaded devices would be required (i.e. int((78⌈16)+1)). To associate the generated coefficients with the appropriate '256 device, edit the <filename>.coe file, and extract coefficients from the fourth line, modulo 16. The first '256 device would receive the first 16 coefficients (C00 - C15), the second would receive the next 16 coefficients (C16-C31), and so forth until the fifth device, which receives the last 16 coefficients (C64 - C79). The last two coefficients (C78, C79) will be zeros.

Assuming the program constraints are such that the purchase of five '256's to implement the filter function is not plausible, consider some things which might be done to simplify the hardware:

- Relaxation of the filter design specifications. The 400 Khz pass band width is narrow, and coupled with the pass band ripple specification of 100 milli-dB make this a difficult filter to implement.

- Raising the input sample rate and system clock rate so the upper frequency transition is not so close to the Nyquist limit would help.

- The pass band of the filter is much lower in frequency than the input sample rate, it would be nice to be able to decimate the filter output, allowing us to double the tap length internally.

By redesigning the clock generation circuitry to use an oscillator at 20 Mhz, with a divide by 2 to generate a 10 Mhz clock, we can provide a 20 Mhz clock to the '256, and a 10 Mhz input sampling rate. This will also move the upper transition frequency away from the Nyquist sampling limit. Selecting the input sample rate to be 10 Mhz instead of 20 Mhz will allow us to double the number of taps available (per device).

Rerunning the filter design program and selecting 20 Mhz clock rate and "clk/2" as the input sample rate will provide us with 32 taps per device. Edit the <filename>.DSP file to show 128, and enter the following filter design criteria:

- Bandpass filter
- Frequency #2 = 0.378 * f_S
- Frequency #1 = 0.338 * f_S
- Free Parameter = transition width
- Filter order = 128
- Pass band ripple = 100 milli dB
- Stopband attenuation = -50 dB

Compiling this filter and re-iterating steps 10-13 listed initially will prove that 54 taps are required to implement this filter at the higher clock rates. Since the input sample rate is now 50% of the system clock rate, each device is capable of providing 32 taps. Only two '256 devices are now required to implement this function. Experimenting with the filter design program will show that a system clock equal to or greater than 16.5 Mhz will allow this function to be implemented (to full design specifications) using only 2 devices.

THE PYTHAGORAS PROCESSOR

In a signal processing system it is frequently necessary to calculate the modulus and argument of Complex numbers. This operation is particularly common after Fast Fourier Transforms or in coherent receiver systems. The evaulation of $\sqrt{(x^2 + y^2)}$ and arctan (y/x) are far from easy, so approximations are often used. A common technique for estimating the magnitude of x + jy is to take the larger value of x or y and add to it half the smaller value. The PDSP16330 Pythagoras Processor is a dedicated DSP engine capable of accurate calculation of both magnitude (modulus) and phase (argument) of Complex data at a rate of 100ns per sample.

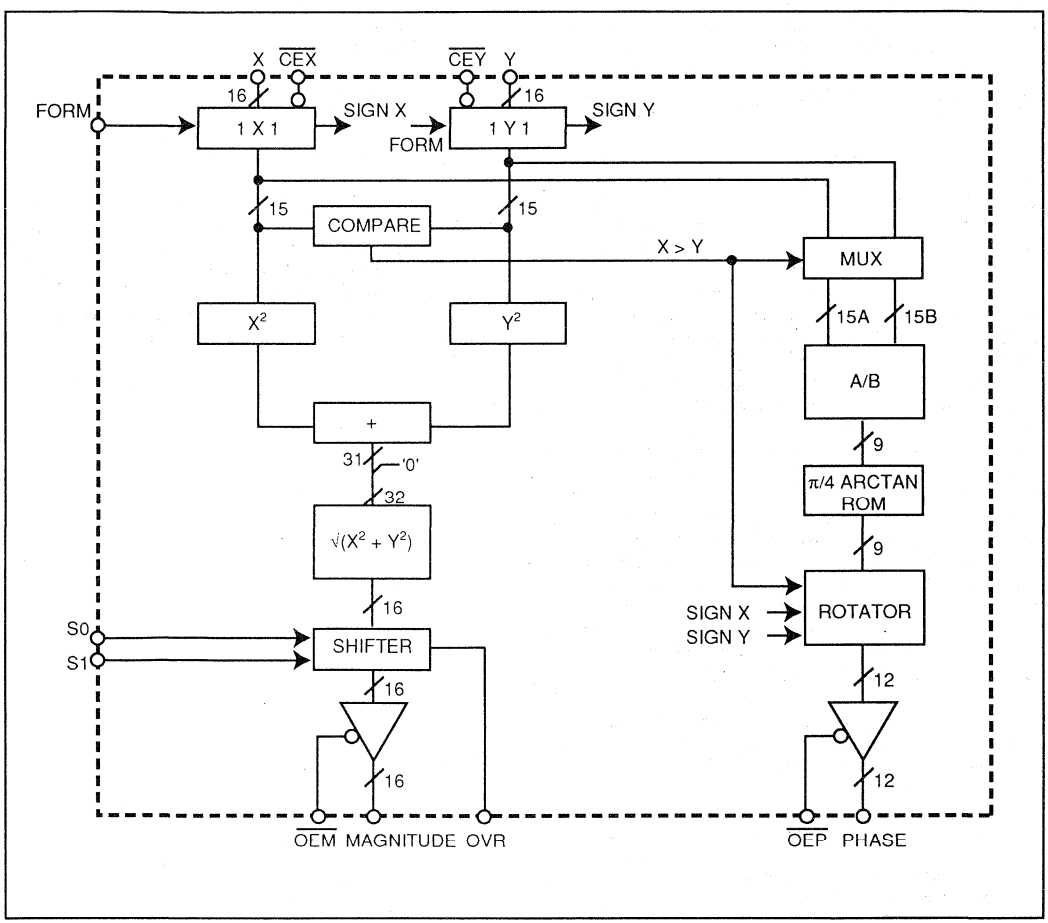


Fig.1 PDSP16330 Block diagram

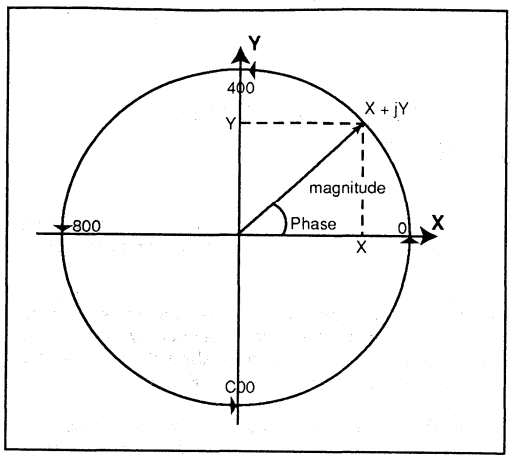


Fig.2

Fig.1 is the block diagram of the device, showing the separate paths for the root sum of squares and arctan (y/x). Fig.2 shows the relationship between the complex input x + jy and the magnitude and phase outputs. Input data can be either 2's complement or sign/magnitude format, depending on the state of the FORM control line.

The magnitude output has a range from 0 to FFFF, four degrees of magnitude output scaling are available via the shift control lines S0 and S1. If the MSB is shifted out of the 0 to FFFF range the OVR flag becomes active, indicating an invalid output. The range of the phase ouput is 0 to FFF representing a full 2π radians.

APPLICATIONS

FFT

After an FFT has been carried out the resulting data is complex. This complex data contains information on the magnitude and phase of individual spectral components, but a Cartesian to Polar co-ordinate transformation is required to extract the desired information.

DEMODULATION

In coherent receiver systems the output from the IF stage will have two orthogonal components, I and Q. The carrier may be amplitude or phase modulated, or both. The Pythagoras Processor is used to extract the modulations from the I/Q data.

ROBOTICS

There are many requirements in robotics, position control and position monitoring where conversion from Cartesian space (X, Y, co-ordinates) to polar space (range and angular position) is needed. The Pythagoras Processor is capable of these transformations at very high speeds making it suitable for use even in fast moving machines.

THREE DIMENSIONAL COORDINATE TRANSFORMS WITH THE PDSP16330

The PDSP16330 is designed to carry out the coordinate transform x,y,→r,θ. Many applications in robotics and target positioning require three dimensional transformations of the form x,y,z→r,θ,ø. This application brief shows how the Pythagoras Processor PDSP16330 can be used for three dimensional transforms.

Fig.1 shows a point x,y,z in a three dimensional space. If we move down the z-axis to the point x,y,0, we are at a point whose distance from the origin is $h = \sqrt{(x^2 + y^2)}$ whose bearing is arctan (y/x). The distance from the origin to the point x,y,z is therefore given by $r = \sqrt{(h^2 + z^2)}$ and the elevation of that point given by arctan (z/h). In this way the three dimensional transform x,y,z→r,θ,ø has been decomposed into two 2- dimensional transforms which can be carried out by the Pythagoras Processor.

Fig.2 shows the most obvious implementation of a 3-D transform, using two Pythagoras Processors. The first processor is given x,y as its input, providing the bearing and the distance to the point x,y,0. The second processor has z (suitably delayed to match the pipeline delay through the first processor) and h as its inputs giving r and ø as its outputs. Output θ from the first processor is delayed so that all three outputs suffer the same pipeline delay.

Fig.3 shows an alternative realisation employing a single Pythagoras Processor. In this case x and y data are input on every other cycle, the alternate cycle inputs being z and h. The z input has a pipeline delay to compensate for the delay on h relative to x and y. The configuration will achieve a throughput of 5MHz, half of the previous circuit.

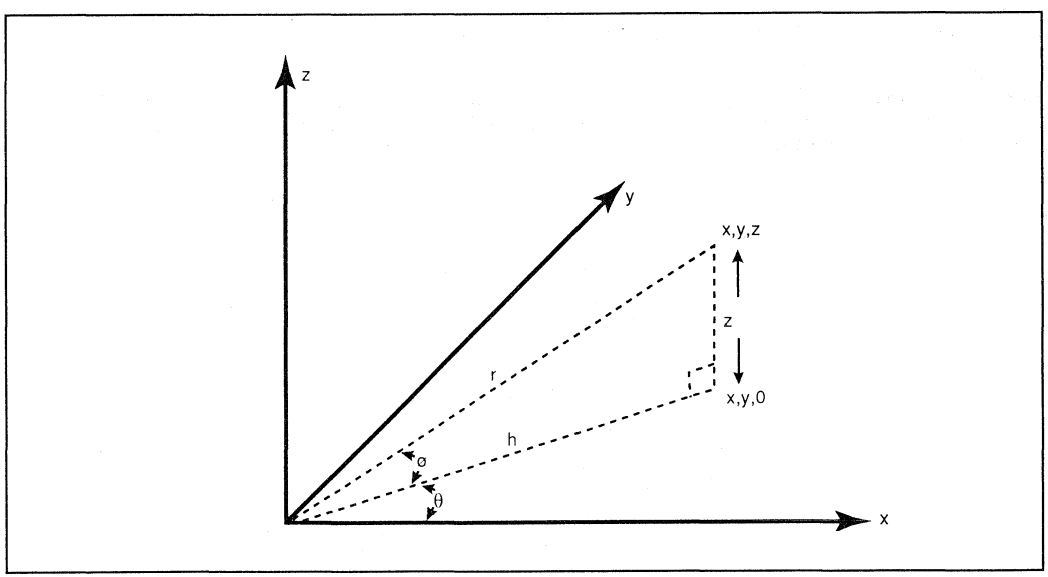


Fig.1

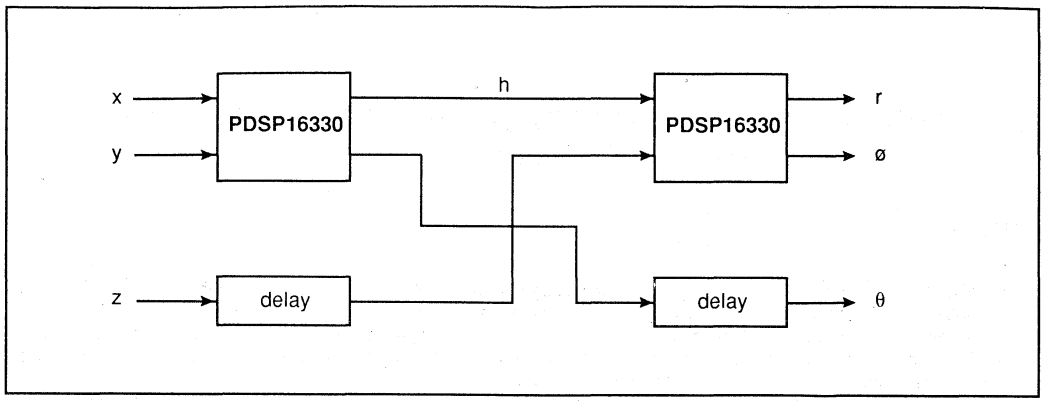

x
y
PDSP16330
h
PDSP16330
r
ø
z
delay
delay
θ

Fig.2

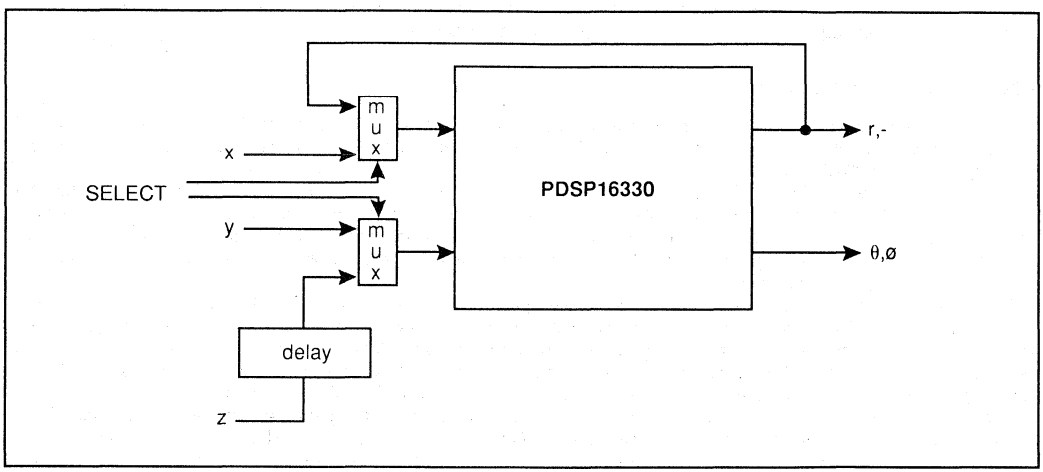

m
u
x
x
SELECT
y
m
u
x
PDSP16330
r,-
θ,ø
delay
z

Fig.3

IMPLEMENTING LARGE AND NON STANDARD TRANSFORMS WITH THE PDSP16510 FFT PROCESSOR

BACKGROUND

The PDSP16510 is a stand-alone FFT Processor which performs 16, 64, 256, or 1024 point FFT's with input sampling rates of up to 40MHz - typically an order of magnitude faster than programmable DSP parts. A single device can window and transform up to 1024 complex points without the need to access external memory during the computation. The device internally uses 16 bit block floating point arithmetic, which provides sufficient precision to allow transform sizes of 4096 points, or even 16384 points in some circumstances, to be implemented with adequate dynamic range.

The purpose of this application note is to describe how the PDSP16510 can be used in systems requiring transform sizes of up to 16384 complex points. In such applications it is necessary to support the PDSP16510 with other arithmetic devices from the PDSP family. Several alternatives are presented but the optimum architecture has a regular structure, is easy to control, and can be repeated as required to accommodate high input sampling rates.

DOING 512 POINT TRANSFORMS

Before going on to consider transform sizes of greater than 1024 points, the special case of the 512 point transform will first be considered. The radix 4 algorithm used by the PDSP16510 requires that the transform length be a power of four, so how can this be modified to handle 512 points?

The simplest way is to zero pad the input data, perform a transform of twice the required length and then discard half the spectral results. There are, however, two possible ways of inserting the zero's; either an equal number of zeros as data points can be appended to the end of the data block or a zero can be inserted between each data point. Appendices A and B present the mathematics of both these techniques, but in order to exploit the window and overlap facilities of the PDSP16510, it is essential to use the interleaving zero approach.

Rember that the PDSP16510 will apply its internal window operator to the complete 1024 point block, and not just to the 512 samples of actual data. Thus, if all the zero's are appended at the end, the data will be incorrectly modified since the actual data will only use half the window operator. In fact if block overlapping is used there will be a phase shift in the results, even for the case of a rectangular window. By interleaving with zero's, the actual data will be modified by every other value in a window containing 1024 operators. This is the correct value for 512 samples using a window with 512 operators.

In the case of interleaving zero's Appendix B proves that the spectrum is repeated in the second half of the outputs. Thus, even though a 1024 point transform is calculated, only the first 512 results need be outputed. The PDSP16510 provides an option to only output half the results, and hence improve the efficiency of the calculation. When zero's are appended at the end, the required spectrum is contained in the even results. The PDSP16510 does not provide an option to output only even results.

A suitable hardware configuration for performing 512 point transforms is shown in Figure 1. The PDSP16540 Bucket Buffer is needed to support continuous transforms, and also to implement block overlapping. Data is written to the buffer at twice the

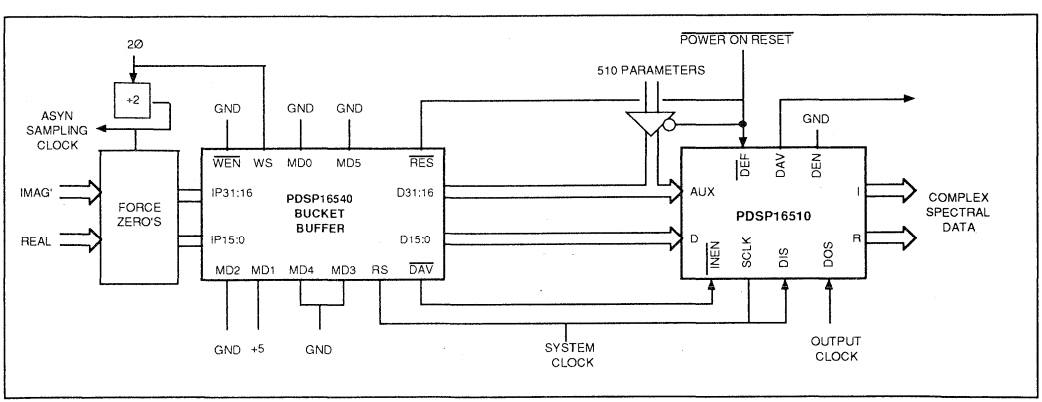


Figure 1. System for Performing 512 Point Complex Transforms

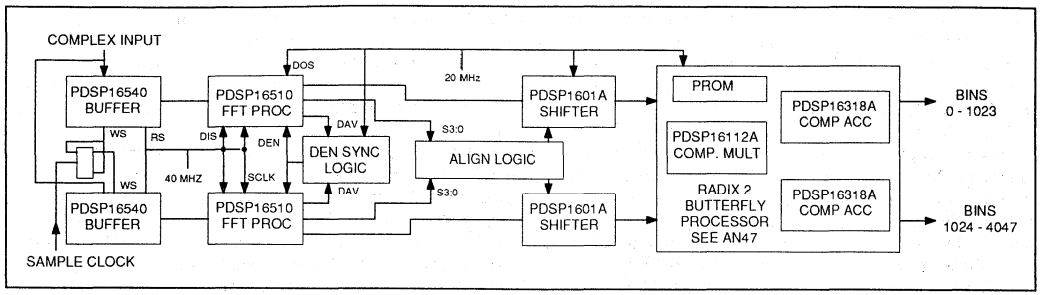


Figure 2. The Direct way to Implement 2048 Point Complex Transforms

original sampling rate, with external logic inserting zero's during the odd clock periods. Such a configuration will support a maximum data sampling rate of 3.4 MHz, but this can be increased to 20 MHz by connecting six devices in parallel. This multiple device arrangement is described in the PDSP16510 data sheet, and it should be noted that the Bucket Buffer is then not needed. The sampling rates achievable with a given number of devices will always be half those obtainable when doing true 1024 point transforms.

This highlights the disadvantages of the zero's insertion technique; the continuous sampling rates achievable are only half those obtainable when doing straightforward transforms of the same length. This stems from the fact that in the time taken to complete the whole transform operation, only half as many actual samples must have been written into the input buffer. Other system constraints must thus have dictated the need to only do 512 point transforms, rather than the transform time itself.

The techniques described in the following sections indicate how large transforms can be implemented, and are also applicable to 512 point transforms. In essence they trade the simple parallel approach to increasing the sample rate with additional multipliers, PROMS, and accumulators.

THE DIRECT WAY TO IMPLEMENT LARGE TRANSFORMS

Equation 1 in Appendix A indicates that an N point DFT can be expressed as the summation of the even and odd, N/2 point, DFT's; in fact a summation of the even points and the odd points twiddled by the otherwise missing sine and cosine values. Appendix A goes on to show that Equation 1 only represents the first half of the N point DFT. The second half is shown to be obtained by a twiddle and difference operation.

The direct way to implement a 2048 point transform would thus be to use two PDSP16510's; one performing a 1024 point transform on the odd inputs, and the other performing a 1024 point transform on the even inputs. As shown in Figure 2, the addition of a PDSP16112 complex multiplier and two PDSP16318 complex accumulators will combine the results to simultaneously produce both halves of the 2048 point transform. The use of the PDSP16540 Bucket Buffer allows the incoming data to be continuous, and any amount of block overlapping can be selected.

In this system both PDSP16510's must produce their results simultaneously. This can only be gauranteed if the outputs are controlled by the DEN input. When both DAV outputs have gone valid, a DEN signal should be produced which is synchronized to the DOS strobe. The even sequence will then be exactly concurrent with the odd sequence, once the output circuit has been primed (see the DSP Handbook page 134). If the derived DEN signal is delayed by 14 DOS strobes (4 PDSP16510 priming delays plus 8 PDSP16112 delays plus 2 PDSP16318 delays) it can be used to provide a Data Valid signal to the rest of the system.

One of the complex accumulators can be avoided if the results produced by the PDSP16510's are read twice, firstly to produce bins 1-1023 with an add operation, and then bins 1024 - 2047 with a subtract operation.

This configuration has two shortcomings; the internal window operator cannot be used and shifters are required to align the

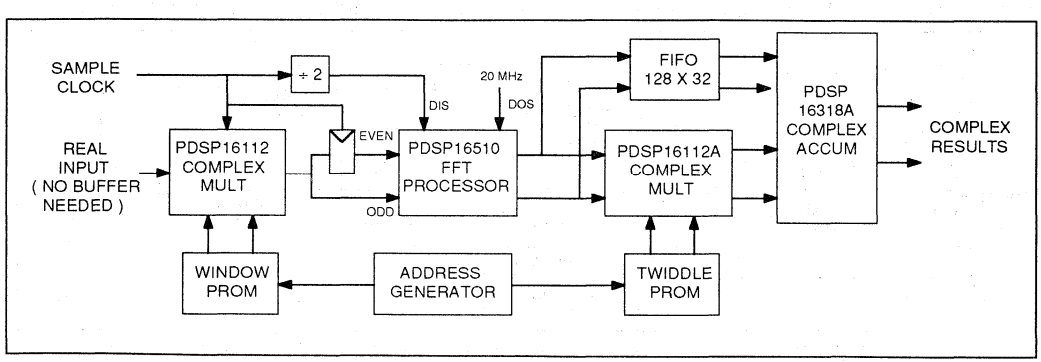


Figure 3. A System to do 512 Point Real Transforms

outputs from the PDSP16510's. The system thus needs an additional complex multiplier to window the data, which cannot be combined with the post twiddle operation needed in the backend butterfly processor. This is not shown in Figure 2. The shifters are needed since it cannot be guaranteed that both devices will produce the same block exponent from the internal variable shift operation, and turning this feature off would produce very poor dynamic range. PDSP1601's can be used for the shift operation, but unfortunately they have to be positioned before the combination of the results, and four devices are needed to shift two sets of 32 bit outputs. More efficient configurations are discussed in the next section.

This direct approach to computing larger transforms can, however, be used to produce an efficient system for 512 point real transforms. Such a system is shown in Figure 3, which illustrates a PDSP16510 configured to perform two simultaneous 256 point real transforms. This system will support incoming sampling rates of up to 19.5 MHz when doing 512 point real transforms (see Table 5 in the datasheet). With 50 % overlapping the rate reduces to 9.7 MHz, and with 75% overlapping it reduces to 4.8 MHz. To support these input rates the output rate should be at least equal to 19.5 MHz sampling rate. Since the PDSP16510 would need a 40 MHz system clock to achieve these throughputs, a convenient solution would be to divide this clock by two and then to use it as the output strobe. Both the PDSP16318A and PDSP16112A will support output clock rates of 20 MHz.

In this system the even samples are applied to the real input pins of the FFT Processor, and the odd samples to the auxiliary pins. No output shifters are needed since both sets of outputs will be internally shifted by the same amount. Since the PDSP16510 will output all the even results followed by all the odd results, it is necessary to buffer the even results in a FIFO. As the odd results are outputed they are twiddled and added to the even results coming from the FIFO.

In the case of real transforms the second half of the spectrum is a repeat of the first half. Thus the PDSP16510 will only output 128 even bins followed by 128 odd bins, even though two sets of 256 samples were applied. Only one PDSP16318 is needed at the output doing a complex add operation; the second half of the results do not exist and the twiddle and subtract is not needed.

This system can use the internal block overlapping features of the FFT Processor. Unfortunately the internal window operator cannot be used, and to perform this function a complex multiplier is needed at the input as shown in Figure 3.

MORE EFFICIENT WAYS OF IMPLEMENTING LARGE TRANSFORMS

Appendix C shows how an N point DFT can be performed by a combination of L and M point DFT's where N = L x M. After the L point transform the results are twiddled by $\exp(-j2\pi ms/N)$ where m = 0 to M-1, and s is the row index. So how should L and M be chosen to make optimum use of the PDSP16510 and its supporting devices?

The most obvious approach is to use two FFT Processors, with an intermediate memory to store the results from the column transforms, and a complex multiplier to apply the intermediate twiddle factor. But this solution has three drawbacks; the memory cannot be a simple FIFO, since an address translation from columns to rows is needed, the internal window operators cannot be used, and results from the column transform will have different scaling factors. The last problem can be avoided by restricting the column transform to 16 points and turning off the internal block floating point option. With such a small transform size the dynamic range should not be compromised, and with the second FFT Processor doing 256 point transforms the system would handle 4096 points. In such a system, however, the window operator can only be applied to the data before it is stored in the input buffer. Thus the system needs two additional complex multipliers, one for the window operator and one for the intermediate twiddle.

This requirement leads to the possibility of making better use of the complex multipliers. Rather than using two PDSP16510's why not make the columns very small and use a complex multiplier and accumulator to perform a straightforward DFT, rather than an FFT? Thus a 2048 point transform can be done by calculating a 2 point DFT followed by a 1024 point FFT. The calculation of a 2 point DFT requires no multiplications, and the window and intermediate twiddles can be combined into one multiply operation.

We have thus chosen L in Appendix C to be 2, and M to be 1024. The row index, s, is thus 0 or 1. The data is thus arranged with samples 0 - 1023 in one row and 1024 - 2047 in the other row. **One** point of each of the two point DFT's is then calculated using samples 0 and 1024, followed by 1 and 1025, up to 1023 and 2047. The even point DFT calculation is just the sum the two inputs, and, since s = 0 in the first row, then the intermediate twiddle is unity . The resulting data is loaded into the PDSP16510,

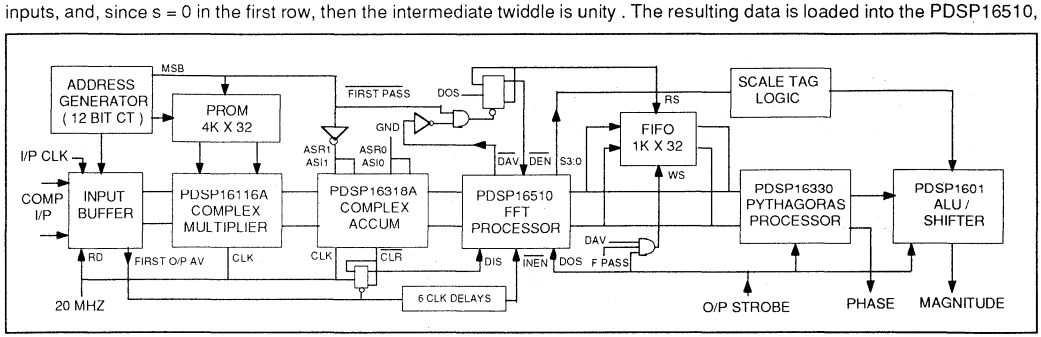


Figure 4. An efficeint system for performing 2048 Point Transforms which can adapted for up to 16384 Points

which does a 1024 point transform to calculate the even results of the 2048 point transform that is required. Since the twiddle values are unity, the PROM should contain the unmodified window operators which are read in the same sequence as the data from the input buffer i.e. 0, 1024, 1, 1025 etc.

The second point of the two point DFT is now calculated, and is simply the difference of the same sequence of values used previously. These must then be twiddled by exp(-j2πm/2048),before being transformed by the PDSP16510 to produce the odd values of the 2048 point transform. This can be done prior to the DFT by storing a second set of window values in the PROM which have been modified by these twiddle factors.

A system which will perform the necessary calculations is shown in Figure 4. The input buffer must handle any necessary block overlapping, and must allow sample 0 to be read out first, followed by sample 1024, then sample 1 and so on. The PDSP16116A performs the necessary complex multiplication using values from the PROM. The PROM must contain a set of 2048 window values plus a second set of modified window values as previously explained. A simple 12 bit counter can be used to provide the address sequences, with the most significant bit providing a page address bit, and the least significant bit used to provide the most significant address bit in each page.

The DEN and FIFO read strobe logic, shown in Figure 4, assumes that the odd results are calculated first. These are then dumped as quickly as possible into a FIFO. The outputs from this FIFO can then be mixed with the even results as they are produced by the FFT Processor during the next pass. The DEN pin on the PDSP16510 can be used to cause its outputs to go high impedance on alternate DOS output strobes. The real and imaginary complex outputs for the PDSP16510 can be converted to magnitude and phase by the PDSP16330 Pythagoras Processor.

The PDSP16318 does a complex subtraction whilst the first set of intermediate values are read into the PDSP16510, and then does an addition for the second set of inputs. Since the arithmetic could generate a 17 bit result, it is necessary to set the shifter within the PDSP16318 such that the 16 output pins for each complex component discard the least significant bit from the accumulator (S2:0 = 011).

The sequence of events within the PDSP16318 is as follows, and produces an input for the PDSP16510 on every other clock cycle (after an initial delay of 3 clock cycles).

1) Load complex point A0. Clear the accumulator (after the next clock edge)
2) Load complex point B0. Transfer A0 to the accumulator (ALU function is Accumulator + A0)
3) Load point A1, Clear the accumulator (after the next clock edge). Do Accumulator + B0 and load the output register.
4) Load point B1. Transfer A1 to the accumulator. A0 + B0 available at the output pins.
5) Load point A2. Clear the accumulator etc

The two sets of outputs produced by the PDSP16510 will have different bit significance, as indicated by the Scale Tag values. This tag indicates the number of left shifts which have occurred in order to compensate for too many right shifts introduced to prevent possible overflow in the internal data path. Thus a smaller scale tag indicates a larger output number. To preserve dynamic range it is necessary to keep the larger set of results, thus the results with the larger scale tag value must be shifted right (divided by 2) by the difference in the scale tag values. This can be done using the barrel shifter within a PDSP1601 ALU. This normalization is best done on the 16 bit magnitude output from the PDSP16330, since the phase outputs will always be correct without any shifts.

The same arrangement can be used to calculate transforms of 4096 points if the PDSP16116 and PDSP16318 are used to generate **each point in turn** of a 4 point DFT. Similarly 8192 points can be transformed if each point of an 8 point DFT is calculated,

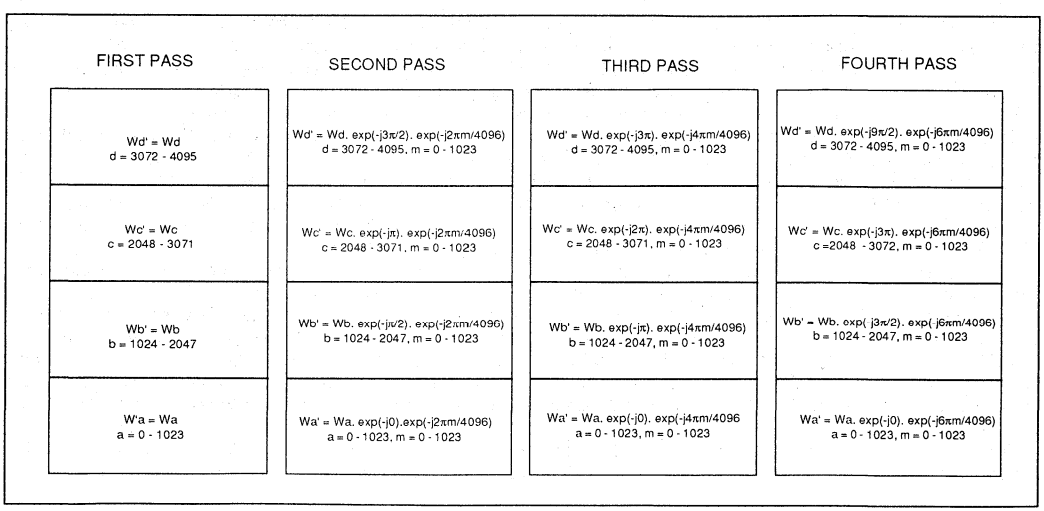


Figure 5. Modified Window Operators needed to perform 4096 point Transforms with one external multiplier

and16384 points can be transformed if 16 point DFT's are done. This will be illustrated using a 4096 point transform.

The original 4096 samples must be arranged in four rows, each containing 1024 columns. Thus Row 0 contains samples 0 - 1023; Row 1 contains samples 1024 - 2047; Row 2 contains samples 2048 - 3071; and Row 3 contains samples 3072 - 4095. To begin the complex multiplier / accumulator calculates the first value in the 4 point DFT using samples 0, 1024, 2048, and 3072. It then calculates the first value using samples 1, 1025, 2049, and 3073 and so on until the first points of all 1024 four point DFT have been calculated.

From the DFT equation given in Appendix A, each value is calculated by a twiddle and summation of the four inputs. The twiddles are expressed as $\exp(-j2\pi kn/4)$ where n is 0, 1, 2, or 3 for the four samples selected, and k = 0 for the calculation of each of the first points or X(0) values. Thus for the trivial case when k = 0;

$X(0) = x(0) + x(1024) + x(2046) + X(3072)$ where X(0) is the first intermediate DFT value.

This calculation is repeated using samples 1, 1025, 2049, and 3073 etc. and the 1024 results are applied to the PDSP16510. This produces results which represent bins 0,4, 8,12 etc. in the 4096 transform actually required.

X(1), X(2), and X(3) must then be calculated using the same groups of 4 inputs, using k = 1 for the calculation of X(1), k = 2 for the calculation of X(2), and k = 3 for the calculation of X(3). These produce results from the PDSP16510 representing bins 1, 5, 9, 13 etc.; followed by 2, 6, 10, 14 etc.; followed 3, 7, 11, 15 etc.

In order to sequentially output the final 4096 bins it is necessary to provide three FIFO's to store the various sets of results. These are then combined with the last set of results before being converted to phase and magnitude by the PDSP16330A.

The PDSP16318 performs the summation of four inputs, and a two bit word growth can occur. The two least significant bits are thus ignored by setting the shift control S2:0 to 010. The results from the four 1024 point transforms will have different scale tag values, and the results must be normalized to the largest set. This is done by detecting the minimum scale tag value and subtracting it from each of the other values. Each set of results is then shifted right by this amount using a PDSP1601.

These twiddles for the 4 point DFT can be combined with the window operator and the intermediate twiddle. This requires that the 4096 original window operators are arranged in four sets, each of which contains four groups of 1024 different values. Each operator in each group is then modified by $\exp(-j2\pi n/4)$ where n is the group number form 0 - 3. The four groups in each set are further modified by $\exp(-j2\pi ms/4096)$ where m = 0 -1023 and s = 0 in the first set, 1 in the second set, 2 in the third set, and 3 in the fourth set. This arrangement is illustrated in Figure 5.

The total PROM size must be 16384 words, addressed as four pages of 4096 words. The first page is used when the first points are being calculated using an address sequence of 0,1024, 2048, and 3072 (to calculate the first point in the first DFT); followed 1,1025,2049, 3073; and so on up to 1023, 2047, 3071, and 4095. The next page is then used to calculate all1024 second points of the DFT, then another page to calculate all the third points, and finally the last page is used to calculate all the fourth points.

Performance

The performance of the system is dictated by the time taken to do the following operations ; load the PDSP16510 with the results of the column DFT's, do a 1024 point transform, and then normalize and produce phase and magnitude outputs. These operations must be repeated for the calculation of every point in the column DFT. Since the maximum clock frequency of the PDSP support devices is 20 MHz, it will take 100 nanoseconds to calculate one point of a 2 point DFT, or 200 nanoseconds to calculate one point of a 4 point DFT, or 400 nanoseconds to calculate one point of an 8 point DFT, or 800 nanoseconds to do one point in a 16 point DFT.

Thus the time taken to load 1024 intermediate results into the PDSP16510 is 102.4 microseconds when 2 point DFT's are done. The transform time itself takes 97.7 microseconds with a 40 MHz system clock, and to this must be added the time to dump the results. It should be noted that the dump rate of the PDSP16510 can be solely dictated by the requirements of the system.

It will actually support dump rates of 40 MHz, and these rates can be sustained if each set of results is loaded into a 40 MHz FIFO (not shown in Figure 4). The dump time is then only 25.6 microseconds as far as the performance calculation is concerned, and the total time needed to produce 2048 results is 2 x (102.4 + 97.7 + 25.6) = 451.4 microseconds. This corresponds to an input sampling rate of 4.5 MHz. It should be noted that the results need only be read out of each FIFO before the next load, transform, and FIFO write operation is complete i.e. data can be read out at the input sampling rate of 4.5 MHz. The combined rate going into the PDSP16330 is then 9 MHz, and standard grade parts can be used. From the complete system point of view, it might be more convenient if the output clock is obtained by dividing down the 40 MHz system clock needed by the PDSP16510. Either 5 or 10 MHz read rates could then be used, but an A grade PDSP16330 would be needed in the latter case.

This 4.5 MHz input sampling rate is the maximum sampling rate possible with this arrangement, and is only achievable when two 40 MHz output FIFO's are provided. Figure 4 , in fact, only shows the need for one output FIFO. In this situation the performance of the PDSP16330 and PDSP1601 limit the input sampling rate, and A grade parts should be used to allow 20 MHz outputs.The results from the second 1024 point transform can then only be dumped at 10 MHz, and are combined with the FIFO output to give a 20 MHz stream into the Pythagoras Processor. A more conservative performance figure is thus obtained if only one 20 MHz FIFO is assumed to be present, which results in a dump time of 51.2 microseconds for one transform and 102.4 microseconds for the other. The total 2048 point calculation time is then 553.8 microseconds, which corresponds to an input sampling rate of 3.7 MHz.

The above calculations are repeated for 4096, 8192, and 16384 point transforms and the results are summarized in Table 1. Both the maximum performance figures using two FIFO's, and the more conservative figures using one slower speed FIFO are given.

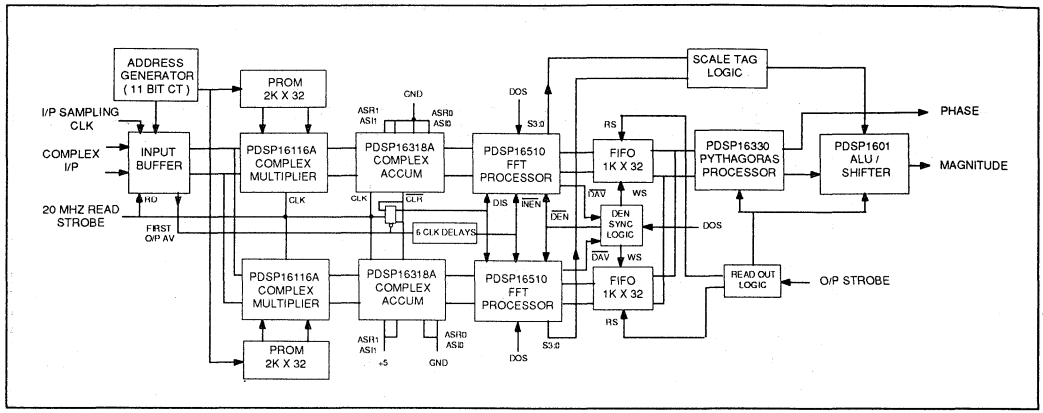


Figure 6. A 2048 point system using two PDSP16510 devices for increased performance

These performance figures can be improved by supplying a complete data path to compute each value in the DFT. Thus two data paths are needed to compute a 2048 point transform, four paths for a 4096 point transform, eight paths for a 8192 point transform, and 16 paths for a 16384 point transform. All the points in any given DFT are then produced simultaneously and applied to their own PDSP16510.

Figure 6 shows the use of two data paths in a 2048 point system, which will support sampling rates up to 9 MHz. These rates can be accomplished with only one PDSP16330A and one PDSP1601A. Because of internal synchronisation within the FFT Processor, one of the data paths may have finished its transform before the other. The paths can be pulled into synchronization by detecting when both DAV signals have gone active, and then generating a common DEN signal which has been synchronized to the DOS strobe. The slower read operations can commence as soon as the FIFO's are not empty. Alternatively both FIFO's can be allowed to fill in their own time , and data then read out when both are full. In this arrangement read and writes need not overlap, but sufficient space must be available in the FIFO's for the next set of results.

Figure 7 is a generic arrangement suitable for any number of data paths, which might be needed to sustain a particular sampling rate. It actually shows four data paths doing a 4096 point transform, with the results going into four FIFO's. These are then read out one after the other to give the sequential results of the 4096 point transform. The four sets of modified window operators are now split between four individual PROMS, but the total contents are the same. The results achieved are also summarized in Table1, and are given for FIFO's with both 40 MHz and 20 MHz writing rates. The reading rates needed are much lower, in fact the rate of combined data going into the PDSP16330 need only be the same as the input sampling rate. The reading rate of the individual FIFO's is proportionally less than this, and depends on the number of data paths in the system.

If the performance achieved with the full complement of additional data paths is too high, then the number of paths can be reduced to suite the sampling rates required.

This technique can be modified to perform 512 point transforms, with the PDSP16510 then doing 256 point complex transforms. In this mode load and dump operation can be concurrent with internal transform operations. With a 40 MHz system clock the transform time is 20.4 microseconds, but the load time is dictated by the 10 MHz maximum rate of producing DFT values from the PDSP16318. This results in a load time of 25.6 microseconds, which is greater than the transform time. The transform time is thus not the limiting factor, and it could be increased to 25.6 microseconds by using a slower system clock.The dump time can also be 25.6 microseconds without restraining the system level performance.

	MAXIMUM SAMPLING RATES			
TRANSFORM SIZE	ONE DATA PATH		L COMPLETE DATA PATHS	
	20 MHz FIFO	2 x 40 MHz FIFO	20 MHz FIFO'S	40MHz FIFO'S
512 (L = 2)	10MHz	- - - - - - - -	20 MHz	- - - - - - - -
2048 (L = 2)	3.7 MHz	4.7 MHz	8.1 MHz	9 MHz
4096 (L = 4)	2.6 MHz	3.1 MHz	11.5 MHz	12.4 MHz
8192 (L = 8)	1.7 MHz	1.9 MHz	14.6 MHz	15.3 MHz
16384 (L = 16)	1 MHz	1.08 MHz	16.9 MHz	17.3 MHz

Table 1. Maximum Sampling Rates

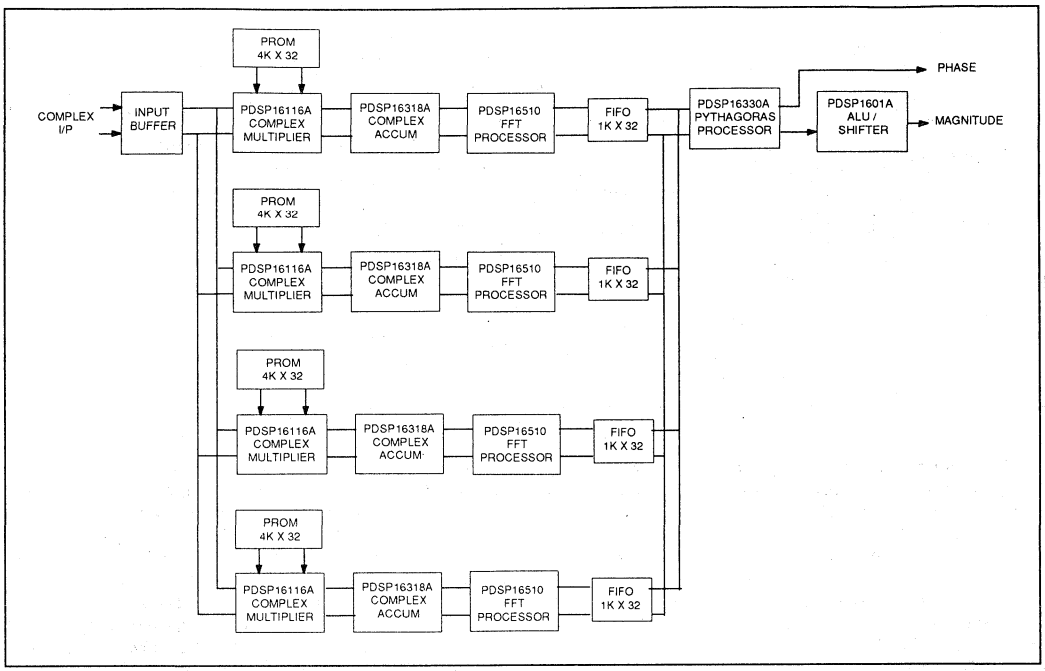


Figure 7. A high performance 4096 point system using four complete data paths

This level of perfromance can be sustained with only one FIFO to store the first set of results, and then dumping the second set of results at 10 MHz. The total time needed for the PDSP16510 to perform two 256 point transforms is thus 2 x 25.6 microseconds, which equates to an input sampling rate of 10 MHz. Two data paths would increase this sampling rate to 20 MHz.

INPUT BUFFERING NEEDS FOR THE PDSP16510 FFT PROCESSOR

BACKGROUND

The PDSP16510 FFT Processor contains 1K x 32 bits of internal RAM, enough to provide working memory for up 1024 point complex transforms. Once this memory is loaded with data no further external intervention is needed. On every pass of the transform, data is read from the RAM using the correct address sequence, and then written back after the butterfly operation. When the data has been completely transformed, it must be read out of the RAM and transferred to the next system element before new data is loaded.

All this, of course, takes many clock cycles, and in the meantime new data is being collected by the acquisition system. If this data is not to be lost it must be stored somewhere for future processing.

For transform sizes up to 256 points this presents no problem to the PDSP1510; it contains sufficient RAM to provide both working storage and input buffering for new data. In fact it contains sufficient RAM to also provide output buffering. This allows a single FFT Processor to handle higher sampling rates than might otherwise be expected.

The input and output buffers allow the time taken to transfer data in and out of the device to be effectively lost at the system level. Thus, whilst the working RAM is being used to transform a set of data, the output buffer can be dumping data previously transformed and the input buffer can be acquiring data to be next transformed. At the system level data is being continuously transformed, assuming, of course, that the time taken to do a transform is no greater than the time taken to load a new set of data.

When 1024 point transforms are to be undertaken no additional internal buffering is possible. Concurrent load, transform, and dump operations are thus not possible, and incoming data must be externally buffered if no information is to lost whilst a transform is in progress. For continuous transforms, the time taken to load this buffer must be greater than or equal to the sum of the time taken to read data from the buffer into the PDSP16510, then to transform it, and finally to transfer to the next device.

At first sight this buffer could be a simple FIFO, albeit a very wide 32 bit FIFO. It would also needs read rates of 40 MHz if maximum throughputs are to be possible. Once this FIFO were full additional logic would have to ensure that at least one location was transferred to the FFT Processor before the next word was written.

Many DSP applications, however, need to overlap data sets in the time domain before they are transformed to the frequency domain. This is the result of the need to apply a window operator to the data before it is transformed. Since only a finite segment of a signal can be observed at any time, discontinuities at the edge of the segment will introduce spectral errors. These are minimized by applying a window operator which weights the data more in the middle and less at the edges. There is thus a danger of missing some information at the edge of the segment, and this is avoided by overlapping the segments. Typically segments need to be overlapped by 50% or 75% to avoid loss of information, but the greater the overlap the less is the data sampling rate that can be achieved.

Overlapping data sets implies that old data must be re-read before new data is appended; an impossible task with a FIFO. For this reason the PDSP16540 Bucket Buffer has been introduced to support the FFT Processor. It allows data sets to be overlapped in 32 word increments, and requires no supporting logic. Although primarily designed to support 1024 point transforms, it can in fact help in smaller cases. The PDSP16510, itself, then supports 50% or 75% overlapping, but the PDSP16540 can be used when different amounts of overlapping are needed. This is discussed later.

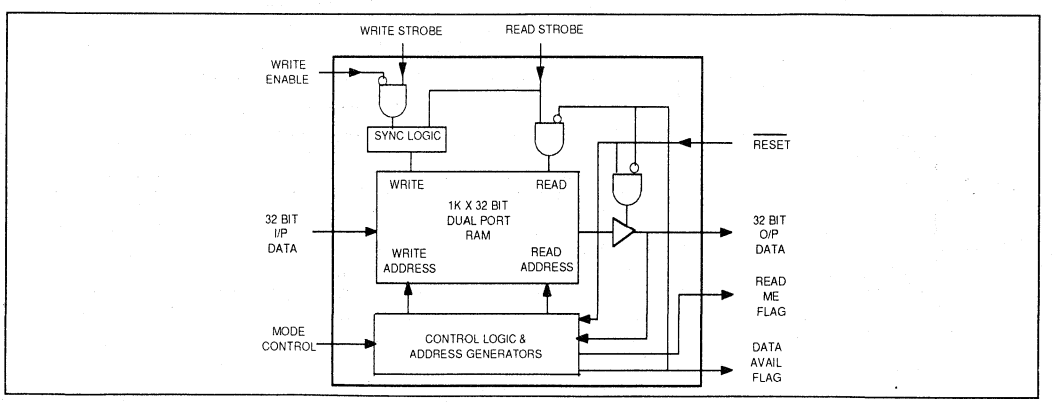


Figure 1. The PDSP16540 Bucket Buffer

THE PDSP16540 BUCKET BUFFER

This device is essentially a 1k x 32 bit synchronous RAM. Being synchronous it requires a continuously available clock, which normally would be the same as the PDSP16510 input and system clocks. It thus has the same 40 MHz maximum rate as the PDSP16510. Note that the data sheet for the PDSP16540 refers to this continuous clock as the read strobe - this does not imply that the strobe should only be present when a read operation is needed.

A write strobe with an enabling signal is needed to write data to the RAM. This write strobe can be asynchronous to the continuous read strobe, and is only needed when data is actually to be loaded. It would normally, however, be the data sampling clock used by the data acquisition circuitry, and thus is expected to be slower than the PDSP16540 read strobe (i.e. PDSP16510 input clock DIS). For example a single PDSP16510 will support continuous 1024 point transforms with sampling rates of some 6.7 MHz, when using 40 MHz clocks. The read strobe for the PDSP16540 is then 40 MHz, and the write strobe is 6.7MHz.

This biased read write ratio makes the use of a true dual port RAM unnecessary. Whenever a write operation is needed the read operation can be interrupted for one cycle, and the write operation actually internally performed with the continuously available read strobe (internal write strobe to read synchronization also takes place).

The device is designed to interface easily to the PDSP16510, and provides comprehensive data overlapping facilities. For correct operation both the block length of the data to be transferred to the PDSP16510, and also the amount of new data in that block must be defined. For commonly used set ups, these two parameters can be defined by tying mode pins high or low. For other alternatives tri-state buffers are needed, connected to up to 16 of the output pins. These are enabled during reset, when these outputs become inputs to an internal latch.

When the programmed amount of new data has been written to the RAM, a Data Available flag (DAV) goes active. This goes in-active for one cycle whenever more data is written to the buffer, and goes permanently in-active when the programmed block length has been transferred. When DAV is active the PDSP16540 will automatically produce new output data on every read strobe edge. The receiving device cannot halt the operation, and it must be dedicated to the transfer task. The DAV signal should be used to provide a clock enable signal for this receiving device.

DAV is the only signal needed to interface to the PDSP16510. For more general applications an additional Read Me Flag is provided. This can be programmed to go active before DAV, and thus warn the receiver that data is about to appear. This signal has no action internal to the PDSP16540.

CONNECTING THE BUCKET BUFFER TO THE FFT PROCESSOR

Figure 2 shows a typical 1024 point system with 50 % block overlapping. Grounding MD0 specifies that 1024 word blocks will be read from the RAM when DAV goes active. Forcing MD2:1 to logical 01 will ensure that DAV goes active when 512 new words have been written to the RAM. Thus the 1024 word block that is transferred to the FFT Processor consists of 512 previously used words and 512 new words. These new words are written to the RAM using the asynchronous Write Strobe, which is also the sampling clock used by the data acquisition circuit. Inputs MD4:3 are really don't care inputs defining when the unused Read Me Flag goes active, but are grounded for electrical reasons rather than leaving them open circuit.

MD5 should be grounded when complex words are to be processed. It should only be tied high if 1024 real transforms are to be performed with no block overlapping (i.e. MD2:0 must be tied low). In this particular case the Bucket Buffer will acquire two blocks of 1024 point real data, through inputs IP15:0, before DAV goes active. These two blocks are then transferred concurrently using all 32 outputs, and the PDSP16510 must be programmed to expect dual real blocks (Control Register Bits 8:6 = 101).

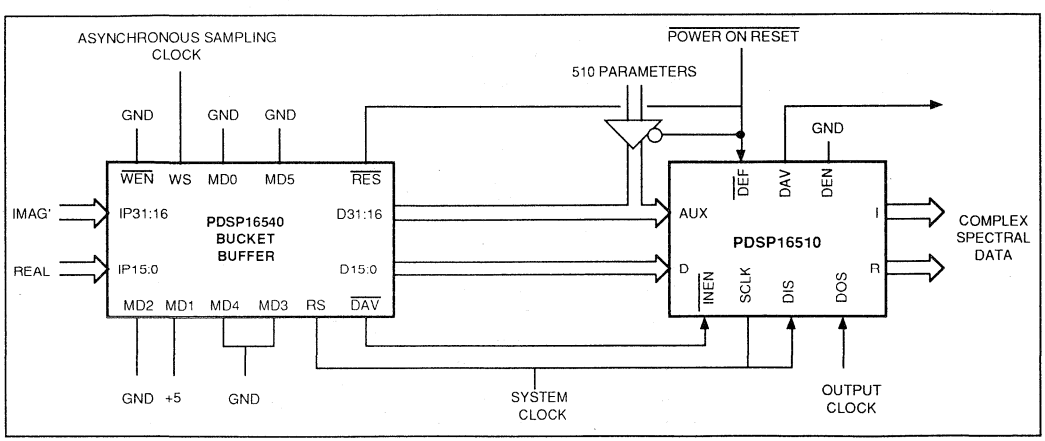


Figure 2. A Typical 1024 Point System with 50% Overlaps

The DAV output is directly connected to the INEN input on the PDSP16510. For correct operation the PDSP16510 must be programmed to use this input as a simple enable i.e. Control Register Bit 12 must be set. The following equation must be obeyed to prevent the loss of any incoming data when doing continuous transforms:

$$NS > 1024B(S/(S - B)) + T + D$$

where N is the amount of new data, S is the input sampling period, B is the read strobe period, T is the transform time which in the case of 1024 point transforms is 3907 system clock cycles, and D is the time to transfer data into the next device.

The factor S/(S - B) arises because the read sequence is interrupted for one B period every time new data is written to the buffer. It thus requires more than 1024 B periods to transfer 1024 words to the PDSP16510. For example if the read rate (B) is 4 times faster than the write rate (S), every 4th read cycle will be inhibited. Thus only 3 out of every 4 read cycles will actually result in data being transfered from the PDSP16540 to the PDSP16510. To achieve the maximum sampling rate possible (i.e. minimum S) data should be transferred in and out of the PDSP16510 at 40 MHz, and the system clock should also be 40 MHz.

Solving for these values gives;

$$NS' \text{ must be } > \frac{25600 \times S}{S - 25} + 123375 \qquad \text{where S is in nanoseconds.}$$

Rearranging the above equation into the standard quadratic form (i.e. S^2 + pS + q = 0) and solving for the routes gives the value for S.

For no overlapping N = 1024 and S must be greater than 150 nanoseconds. The maximum sampling rate is thus 6.66MHz.

For 50% overlapping N = 512, and the minimum S period is 296 nanoseconds. The maximum sampling rate is then 3.37 MHz

For 75% overlapping N = 256, and the minimum S period is 589 nanoseconds. The maximum sampling rate is then 1.69 MHz

Suppose system requirements, for example, dictate a sampling rate of 4 MHz and some overlapping is required. One solution, of course would be to use more than one FFT Processor as explained in the data sheet. The PDSP16540 bucket buffer would then not be needed. Since, in this particular example, the sampling rate achievable with 50 % overlapping is close to the 4 MHz requirement, it may be possible to compromise on the actual overlap used.

Solving the above equation for S = 250 results in the need to load at least 606 new samples before DAV goes active. By setting MD2:1 to 11 it is possible to define the required number of new words in multiples of 32. A 5 bit code is then inputted through a tri-state driver connected to the D9:5 outputs, which become inputs during RESET. This binary code specifies up to 31 additional blocks of 32 above the minimum of 32.

Rounding 606 up to 608 (32 x 19) results in the need to load the code 10010 through pins D9:5 to achieve the overlap possible. The actual percentage overlap is then 40.6% and the 4 MHz sampling rate will be possible.

In a similar manner the Bucket Buffer can be used to provide non standard overlapping when transform sizes smaller than 1024 points are required. Such a system is illustrated in Figure 3. By forcing pin MD0 high it is possible to define block sizes of less than 1024 words. A 5 bit code on pins D4:0, during RESET, defines up to thirty one additional 32 word blocks after the basic 32 word block. Thus to define a 256 word block it is necessary to input the code 00111 via a tri-state driver on pins D4:0.

The calculation needed to define the minimum sampling period with a given overlap is different when 1024 point transforms are not being performed. As explained earlier, the time to transfer data in and out of the PDSP16510 can then be effectively lost

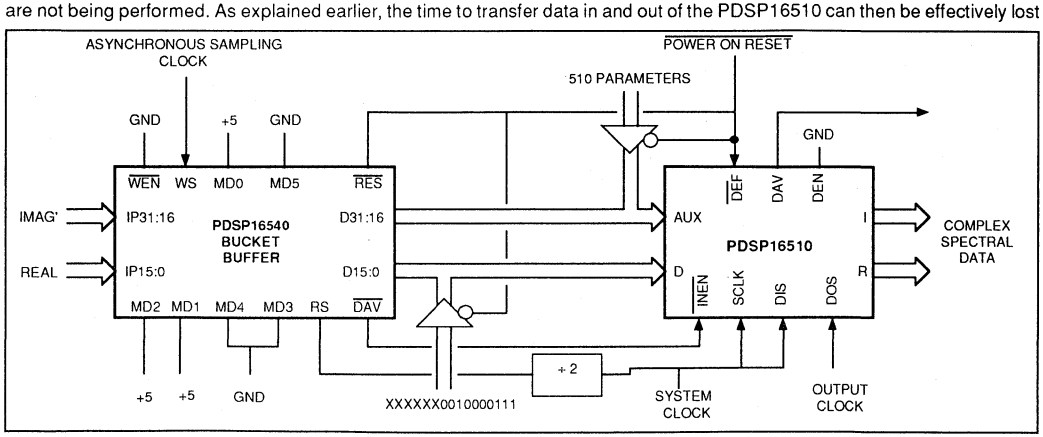


Figure 3. A 256 Point System with Non Standard Overlaps

at the system level. The required equation then simplifies to:

$NS > T$ if transfer times in and out of the PDSP16510 are less than T.
N, S, and T are as previously defined

When concurrent load, transform, and dump operations occur in the PDSP16510, it is not possible for the input clock rate (DIS) to be same as the system clock rate. The actual input rate must be reduced by the factor F from the system clock rate, where F is given by;

$$F = \frac{4}{6 + 0.001L}$$ where L is the system clock low time.

Thus if the system clock rate is to be 40 MHz, the clock low time would be say 12 nanoseconds, and the factor F would be 0.665. The maximum input rate is thus 26.6 Mhz.

In practise this is much greater than that needed to ensure that the time, to transfer 256 words from the Bucket Buffer to the FFT Processor, is less than the transform time. From the PDSP16510 data sheet the time taken to perform a 256 point transform, with a 40 MHz system clock, is 20.4 microseconds. Thus the input clock period needed to load 256 points in that time is 79 nanoseconds: or an input rate of 12.65MHz.

In this example the most convenient approach is to simply divide the system clock by two in order to provide the read strobe for the Bucket Buffer. There is, however, a relationship between the read strobe rate and the maximum write strobe rate. The write strobe period must be at least twice the read strobe period plus 10 nanoseconds. Thus with a 20 MHz read strobe the maximum write strobe rate is 9 MHz.

This writing rate is only achievable with read overlaps up to 50 %. Beyond this a second read rate requirement comes into effect. The write strobe period must also be greater than the read period multiplied by L/N, where L is the read block length and N is the amount of new data. This is another way of saying that the time taken to read the complete block must be no more than the time taken to load the required amount of new data.

In practise with a 20 MHz read strobe these considerations will not limit the writing rate in any way, and the maximum rates will be solely governed by the transform time in the FFT processor. Suppose, for example, we need to support a sampling rate of 7MHz (144 ns period) when doing 256 point transforms with some overlap. Then;

N X 144 must be > 20400 (the transform time)

Thus N must be greater than 142 for 7MHz sampling rates. Since N must be rounded up to a multiple of 32 it is thus necessary to load 160 (32 x 5) new samples in the 256 word block. This requires the code 00100 to be present on pins D15:10 during RESET, and gives 37.5% block overlapping.

Note : In all the above equations any requirement for the input clock (DIS) to be asynchronous to the system clock (SCLK) of the PDSP16510, will have to be modified in a practical system. The PDSP16510 has a requirement that its input and system clocks must be synchronised to each other. It may be possible to burst into the PDSP16510 data at a higher rate than the equations specify, such that DIS is synchronous to SCLK, but that on average the required DIS rate is achieved. When using the PDSP16540 on the input, however, it is very easy to burst data into the PDSP16510.

INCREASE THE PERFORMANCE OF THE PDSP16510 FFT PROCESSOR BY USING MULTIPLE DEVICES

BACKGROUND

A single PDSP16510 FFT Processor ,using a 40 MHz system clock, will support sampling rates up to 12.3 MHz when doing 256 point complex transforms, and up to 6.8 MHz when doing 1024 point complex transforms. These rates can be increased to 40 MHz when several devices are connected in a ring arrangement.

In such a system one device is loaded with a complete block of data, and then starts a transform operation using its internal RAM. In the meantime incoming data is loaded into another FFT Processor which will then start its transform operation when all the data is available. Sufficient devices are needed to ensure that the first device has finished before its turn comes round again for new data.

The PDSP16510 actually supports two multiple device modes of operation. One mode always does separate load, transform, and then dump operations regardless of the actual transform size. The other mode does concurrent load, transform, and dump operations, but cannot be used to perform 1024 point transforms. It can in some circumstances allow less devices to be used in order to achieve a given sampling rate.

Note that an input buffer is not needed in either mode of operation (even when doing 1024 point transforms), and interdevice flags support block overlapping. With the standard 50% and 75% block overlapping no external logic is needed.

Note also that this arrangement is only intended to increase the sampling rates possible with the transform sizes supported by a single device. If larger transform sizes are needed see Application Note AB35.

GENERAL CONSIDERATIONS

Figure 1 illustrates the basic ring arrangement, using three devices for convenience. It can, of course, be expanded to any required number of devices. It shows that both inputs and outputs are commoned together. A block of data is loaded into the first device, then the next block is loaded into the second device, and so on. Sufficient devices are provide to ensure that continuous data can be supported without any loss.

The LFLG output and INEN input are used to co-ordinate the splitting of incoming data between the devices. This requires

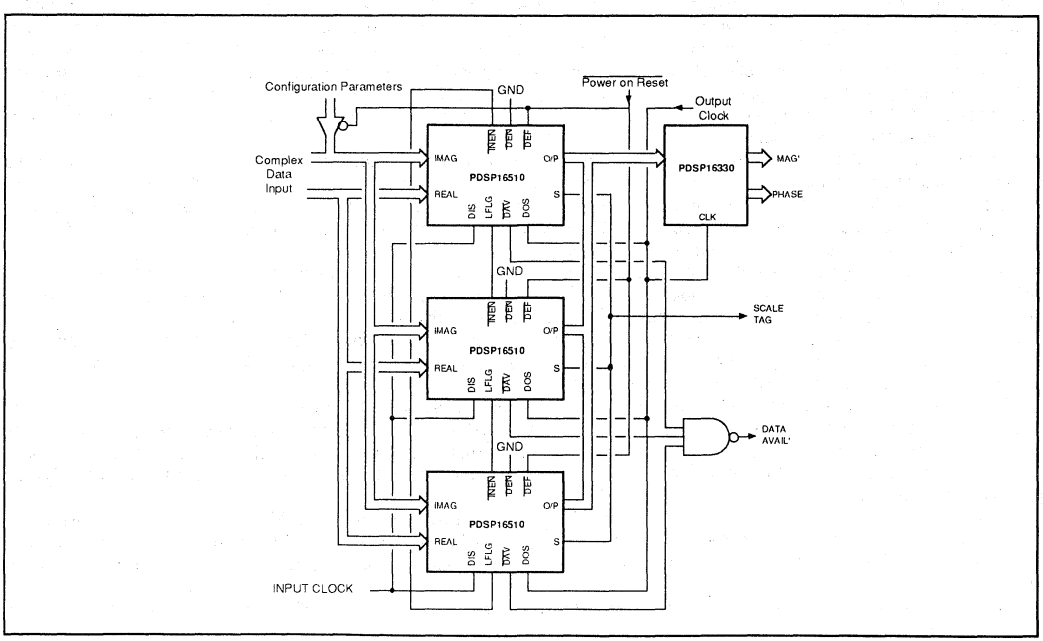


Figure 1. The Basic Multiple Device Arrangement

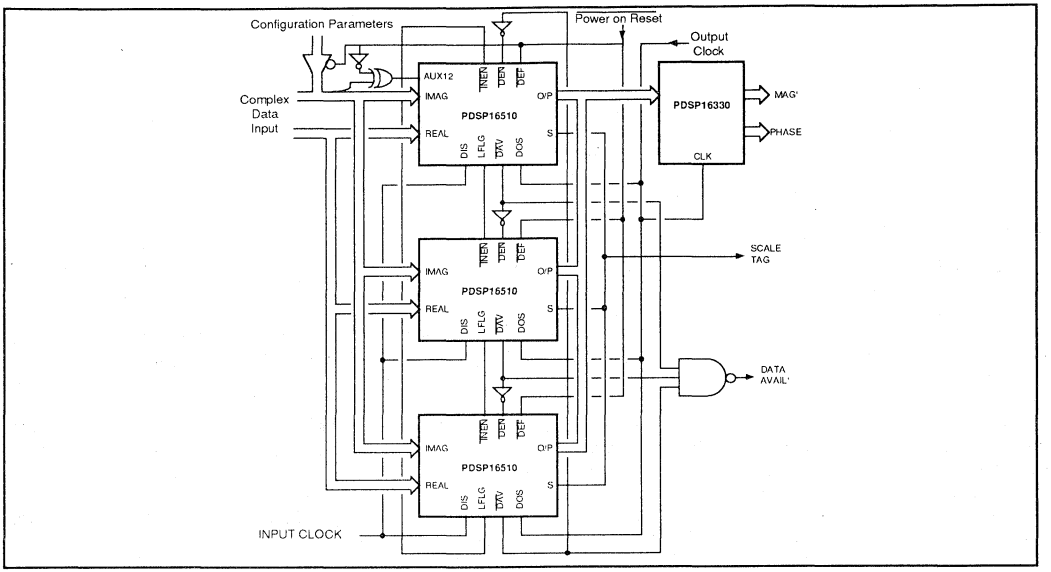


Figure 2. Adaptation of the Basic System

that the input data enabling signal (INEN) is no longer a simple DIS strobe enabling input. Whenever the Control Register specifies a multiple device mode of operation, it becomes a global ,edge activated, block enabling input. When it goes low a new block load operation commences, which will then continue until the programmed number of samples have been loaded. INEN can go back high at any time without causing inputs from the current block to be inhibited (early silicon requires that INEN stays low at least until all the block has been loaded).

The Load Flag (LFLG) goes active high after the first sample has been loaded, and goes low when the programmed number of samples have been loaded. This low going LFLG edge from a previous device provides the low going INEN edge to the next device. Thus once one device has received its full complement of data the next one will start loading data. As a further enhancement the LFLG will go in-active after half the block has been loaded if 50% overlapping is in use, or after a quarter the block has been loaded if 75% overlapping is in use. Thus, if for example, 50% overlapping is in use, the second device will also start loading data half way through the load operation into the first device. Two devices thus receive the same data in order to mechanize the overlap requirement.

By tying all the outputs together the system need only provide one output processor. The actual processing needed on the outputs is application dependent, and is beyond the scope of this article. It is assumed, however, that unless speed requirements make it impossible, the use of only one output processor will provide some economic advantage. It is also assumed that the reason for using multiple devices was to continuously process incoming data, without any loss of information. Thus once results are available they must be passed on to the rest of the system.

This can be achieved by tying all the Data Enable (DEN) inputs low, as illustrated in Figure 1. The Data Available Flag (DAV) will then be synchronized to the output strobe, and will go active when the first result is available on the output pins. The output bus goes low impedance with respect to the same output clock edge which causes DAV to go active. Figure 1 in fact shows all the DAV flags OR'ed together to give a common indicator for the rest of the system. In practice this only makes sense if the dump time is less than the load time. The combined output would then go in-active between individual devices for a period equivalent to the difference between the load and dump times.

For convenience we have so far indicated that all the DEN inputs are tied low, but there is some uncertainty in the time taken to complete a transform once all the data has been loaded. In fact the device uses an internal 12 cycle sequence, which will lead to a 12 system clock variation in the time needed to complete a transform. The number of system clock cycles needed to complete each transform, as given in Table 4 of the data sheet, and are worst case numbers. This uncertainty makes tying DEN low potentially dangerous.

If device two effectively completes its transform in less time than device one, then it could start dumping its results before device one had finished. If DEN is tied low this can only be prevented if the dump time (plus 4 DOS periods) is at least 12 system clock periods less than the load time. DIS and DOS can then not be tied together, and it is usually convenient to derive DOS by dividing down from the system clock.

An alternative approach has, however, been provided which still allows DIS and DOS still to be commoned together.

Whenever the control register specifies a multiple device node of operation, the operation of the DAV / DEN circuitry is modified. IF DEN is not active (i.e. high) when the device is internally about to generate DAV, then the output pin will not "asynchronously" go active as happens in the single device mode. Instead the DAV output pin will stay in-active until DEN goes active low. The output bus will also stay high impedance.

By connecting the inverted DAV output from one device to the DEN input of the next, this second device cannot commence its output sequence until the first one has finished, and its DAV has gone in-active. The DAV output from the second device will go active as soon as its DEN input goes low, but it will still be effectively synchronized to DOS since it is derived from the previous DAV signal going in-active. This arrangement is shown in Figure 2.

When DOS is physically connected to DIS, the combined Data Available Flag shown in Figure 1 will only glitch in-active as one device finishes and the next one starts. This glitch would safely occur after a DOS active edge, but even so the flag would only usefully indicate the initial delay from start up before valid results are obtained. When a reliable flag is needed to indicate the end of a set of results, then each PDSP16510 should be provided with a D type latch. This is set by the inactive going edge of DAV and reset when DOS again goes low.

The circuit shown in Figure 1 needs an edge after power on in order to initiate the load procedure into the first device. Rather than providing external logic to generate a start pulse which is OR'ed into the first INEN line, an alternative scheme is supported. By setting bit 12 in the Control Register contained within the first device, it is possible to cause the power on reset signal (DEF) to initiate a load procedure.

All Control Registers are loaded from the common AUX port whilst DEF is active, and we now require one bit in one of the registers to be different from the others! The easiest way to mechanize this is to include an EX-OR gate in the AUX12 input to the first device. The other input is driven from the DEF signal such that it causes a logical inversion as the Control Register is loaded, but not when imaginary data is loaded. This is also shown in Figure 2.

SAMPLING RATES POSSIBLE WITH SEPARATE LOAD TRANSFORM, AND THEN DUMP (MODE 2)

This mode can be used with all transform sizes and the maximum DIS and DOS rates can theoretically be equal to the system clock rates used. The DIS rate is the data sampling rate and can, of course, only be equal to the system clock rate if sufficient devices are provided in the ring to make this sensible at the system level. The DOS rate can be any rate greater than or equal to the system clock rate, and would normally be limited by the capabilities of the output processor.

The number of devices, N, needed to achieve a sampling period of S with a block size of n, is governed by;

$$NnS > nS + PK + D \qquad \text{where D is less than } nS$$

and K is the system clock period, P is the number of system clock periods needed to complete a transform as given in Table 4 of the datasheet, and D is the total dump time allowing for the 4 extra DOS periods needed for the internal output circuitry.

With 50% block overlapping the above equation becomes;

$$NnS > 2(nS + PK + D) \qquad \text{where D is less than } nS/2$$

With 75% overlapping it becomes;

$$Nns > 4(nS + PK + D) \qquad \text{where D is less than } nS/4$$

Table 1 gives the maximum sampling rates possible with 3, 4, 5, or 6 devices and output rates of 20 MHz and 40 MHz. It covers transform sizes of 256 and 1024 complex points.

	1024 POINT COMPLEX TRANSFORMS						256 POINT COMPLEX TRANSFORMS					
Number of	Dump at 20 MHz			Dump at 40 MHz			Dump at 20 MHz			Dump at 40 MHz		
Devices	0%	50%	75	0%	50%	75%	0%	50%	75%	0%	50%	75%
3	13.7	6.8	-	16.6	8.2	-	15.3	7.6	-	19	9.5	-
4	20.6	10*	-	24.8	16.6	-	22.9	10*	-	28.5	19	-
5	27.4	10*	5*	33.2	20*	8.2	30.6	10*	5*	38	20*	9.5
6	34.3	10*	5*	40*	20*	10*	38.4	10*	5*	40*	20*	10*

* indicates that the sampling rate is limited by the maximum dumping rate

Table 1. Maximum Sampling Rates with separate load transforms and dumps. Where sampling rate is asynchronous to SCLK, a PDSP16540 (or similar) is assumed on the input.

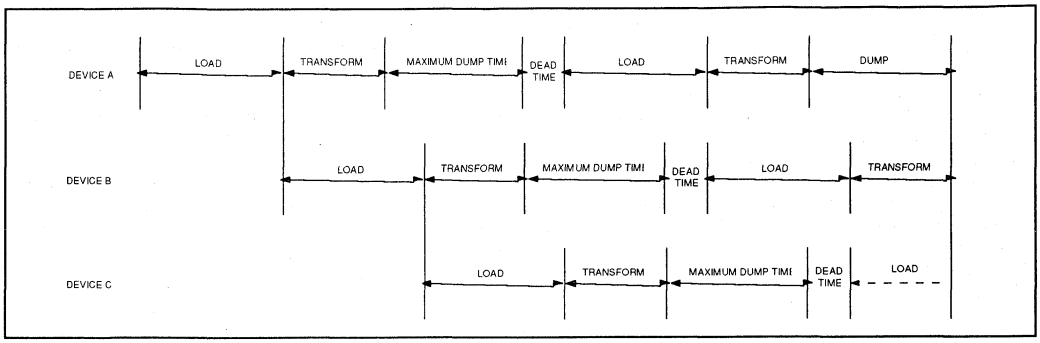


Figure 3. Sequence of events in a 3 device system doing separte load, transforms and then dumps

Figure 3 shows the sequence of events taking place in such a system without overlaps, and Figure 4 shows the sequence in a five device system doing 50% overlaps. It should be noted that the time taken to dump the results must be no more than the time taken to load the block of data (if you put more in than you take out, then something has to give). If 50% block overlapping is used the dump must be complete in half the load time, and one quarter the load time if 75% overlapping is needed. If these criterion are not met, then one device will not have finished dumping before the next one starts. Thus two sets of outputs would be enabled at the same time. Remember that the dump time can easily be made faster than the load time when required.

SAMPLING RATES POSSIBLE WITH CONCURRENT LOAD, TRANSFORM, AND DUMP (MODE 1)

In this mode transfers in and out of the PDSP16510 are concurrent with transform operations. Internal RAM restrictions do not allow this mode to be used with 1024 point transforms. For other sized transforms the sampling rates possible are theoretically much higher for a given number of devices. A limitation is, however, imposed on the maximum I/O rates, which can no longer be increased up to the system clock rate. Instead the rates are reduced to a factor, F of the system clock rate where F is given by;

$$F = \frac{4}{6 + 0.001\text{ØL}}$$

where ØL is the system clock low time

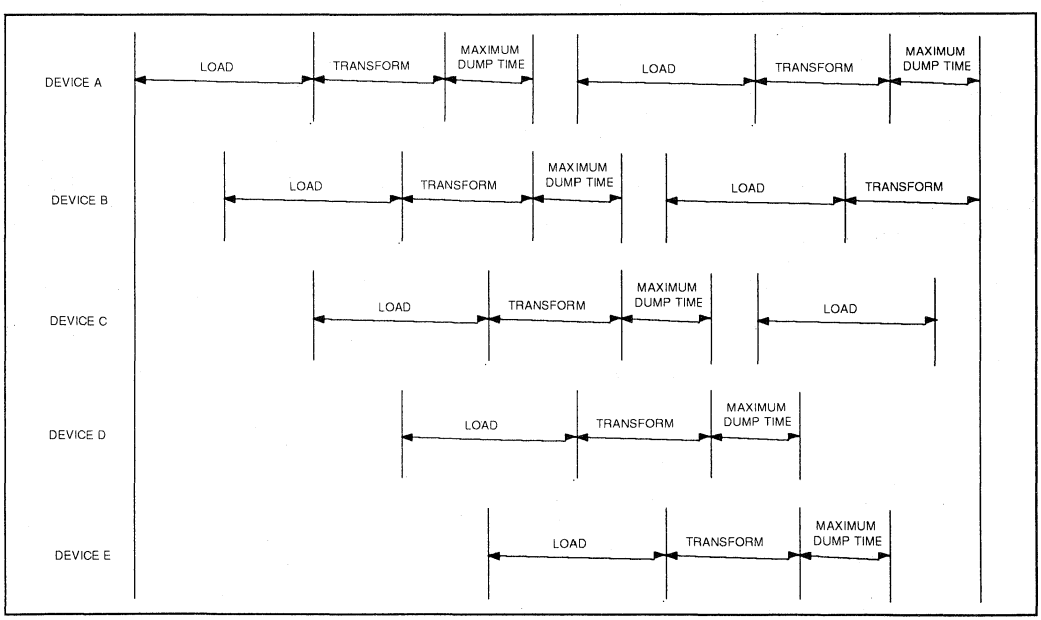


Figure 4. Sequence of events in a 5 device system with 50% overlaps

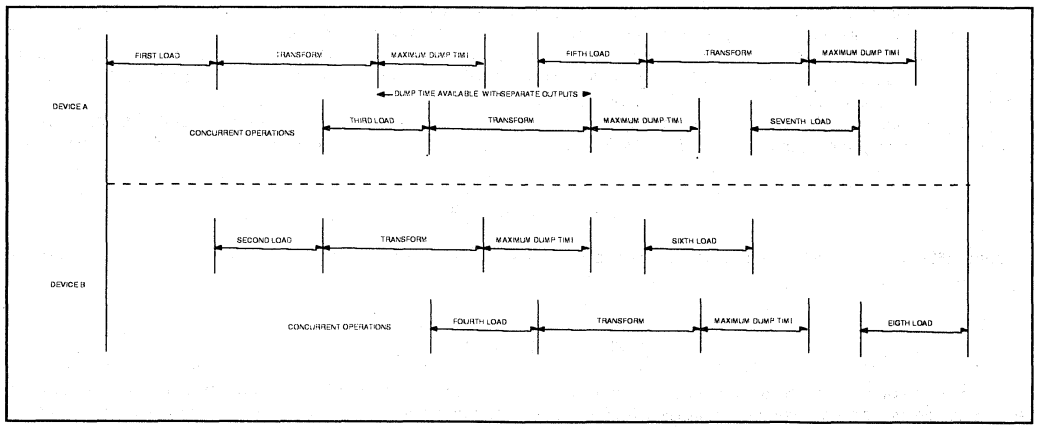


Figure 5. Sequence of events in a 2 device system with concurrent I/O Operations

With a 40 MHz system clock the low time might well be 15 nanoseconds. The factor, F, then becomes 0.66. The maximum theoretical I/O rate is thus 26.6 MHz. In this mode there are no benefits to be gained by increasing the output rate above the input rate (except when necessary because of overlaps). DIS and DOS are thus normally commoned together. In fact the device provides an internal divide DIS by or 2 or 4 feature. Thus the DIS and DOS pins can be externally connected to a source to match the DOS requirements, with the internal DIS strobe internally divided down to the correct frequency for 50% or 75% overlaps.

With N devices the theoretical sampling period, S, ignoring the F factor and with no overlapping is governed by;

$$NnS > PK + 4 \text{ DOS periods}$$

where P is the number of clock periods needed to complete the transform and K is the system clock period.

Figure 5 illustrates the sequence of events which occur with a two device system, with the outputs joined together. With a 40 MHz system clock, and common DIS and DOS, the theorectical maximum input sampling rate given by the above equation is 24.6 MHz when doing a 256 point complex transform. This sampling rate is just less than the limit which would be imposed by the factor F, but all other transform sizes supported by this mode of operation would be limited by the factor F, to sampling rates of 26.66 MHz. If each PDSP16510 has its own output processing circuit, then the outputs would not be joined together and each

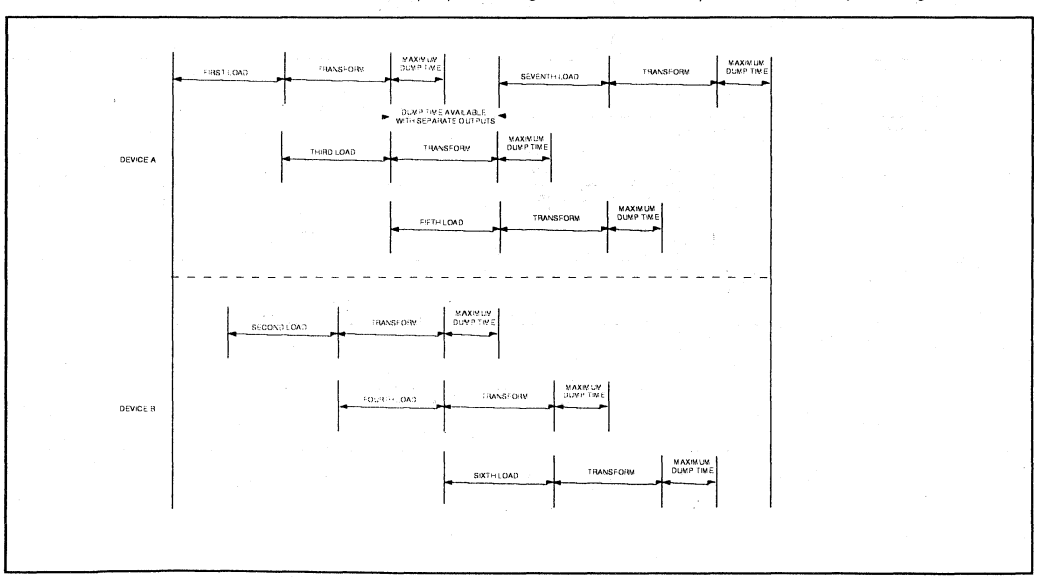


Figure 6. Sequence of events in a 2 device system with concurrent I/O and 50% overlaps

In this mode two devices can be used to gave the same performance when doing 50% overlaps as a single device with no overlaps. But the dump must be completed in half the load time if the outputs are commoned together. This does not limit the performance when doing 256 point complex transforms, and two devices will handle 50% overlaps at up to 12.3 MHz sampling rates. All other sizes are limited to up to 13.3 MHz sampling rates by the F factor, unless each device has its own output processing circuitry. Figure 6 illustrates the sequence of events in such a system.

As long as each PDSP16510 has its own output processor, then extra devices can be added as needed to increase the overlapped sampling rate up to that defined by the F factor i.e. 26.66 MHz. The minimum sampling period down to this limit is governed by;

$$NnS > 2(PK + 4DOS)$$

With 75% overlapping at least four devices are needed, and the minimum sampling period under the same conditions as above is given by;

$$NnS > 4(PK + 4DOS)$$

When all the outputs are commoned the dump must be completed in one quarter the load time. Since the maximum output rate is 26.66 MHz, then the maximum input rate is 6.66 MHz. For all transform sizes this is much less than suggested by the above equation. Thus separate output circuits must always be provided if the maximum performance is to be achieved.

Note that if the input or output rate chosen is asynchronous to SCLK, then a PDSP16540 (or similar) is assumed at the PDSP16510 interface.

MULTIPLE CONCURRENT TRANSFORMS

The PDSP16510 will support 4 concurrent 64 point complex transforms, or 8 concurrent 64 point real transforms. When the performance is increased by using multiple devices configured in MODE 1, a double LFLG transition is provided to support block overlapping. This is illustrated in Figure 7.

The LFLG output goes high after the first sample is loaded, and then low half way through the first sub block if 50% overlaps are in use. This transition is used to instigate the load procedure into the second device. LFLG then returns high and goes low again half way through the last sub block. This second low going transition is used to instigate a new low procedure in the first device.

Note that once a load procedure has started, the occurrence of a second edge will not effect the device in any way and thus each device only responds to an edge as shown in Figure 7. Note also that in this arrangement the DAV / DEN connection MUST be made, even if DIS and DOS are not commoned. This ensures that each device has an equal amount of time to dump its data.

This double LFLG transition also supports 75% overlapping with four devices. The first low going edge occurs 25% through the first sub block, and the second low going edge 25% through the last sub block.

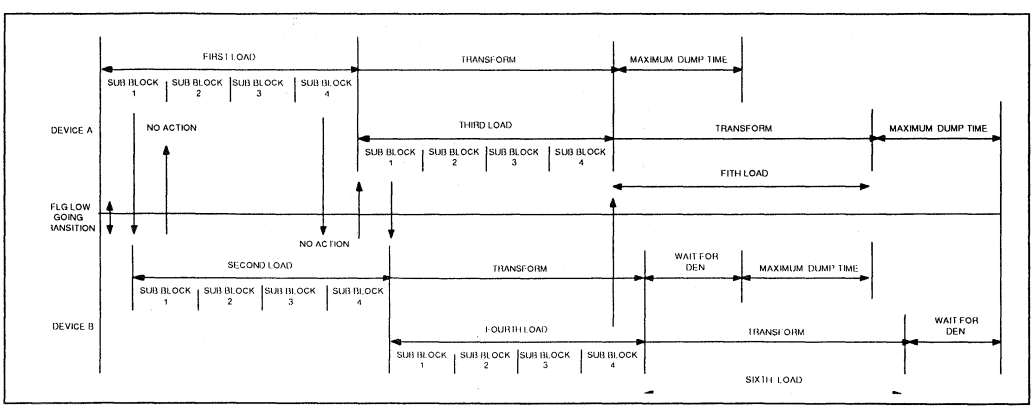


Figure 7. Sequence of events when performing multiple concurrent transforms.

THE PCS PDSP16510 SIMULATOR (Version V1.7)

PCS is a standalone program, running under DOS on PC platforms, which will perform a functional simulation of GEC Plessey Semiconductor's PDSP16510 FFT Processor. The model in the simulator is bit-accurate which means that it is accurate down to the least significant bit in replicating the function of the FFT processor.

The C language device model, which forms the heart of the PCS simulator, is supplied in source code format. This allows a system incorporating the PDSP16510 to be simulated, in software, such that its performance may be characterised and optimised prior to the prototyping stage.

The PDSP16510 FFT Processor

The PDSP16510 calculates Fast Fourier Transforms of up to 1024 points at sampling rates of up to 40MHz. It uses a decimation in time radix four algorithm to calculate both forward and inverse transforms. The device contains its own RAM, which allows new data to be loaded whilst transforming the last data block. The PDSP16510 is also able to dump transformed data whilst simultaneously loading and transforming other data blocks. These three operations: data load, data transform and data dump may all be performed concurrently, if required.

The PDSP16510 also provides built-in data windowing functions: both Blackman-Harris and Hamming windows are supported without the need for any external components, and without adversely affecting the data throughput rate of the device.

The PCS Simulator

For a device as complex as the PDSP16510, the need to be able to predict whether a given level of performance can be met, prior to system design and implementation, is great. It may prove to be difficult to realise this need if published performance data is the sole source of information. The principle of the PCS simulator is that it allows users to predict the in-system performance of this device with user-defined input data. The simulator also allows the user to ask "what if" questions by varying transform size and window operators to gauge their effect without the disadvantages of committing any design to hardware.

PCS offers five options from the master menu:

1. Edit Input Data File
2. Edit Control File
3. Run Single Pass Simulator
4. Run Batch Simulator
5. Return To DOS

1. EDIT INPUT DATA FILE

PCS provides a simple file editor which allows the entry of hexadecimal complex data points in a form suitable for entry to the PDSP16510 simulator. The editor offers block copy and block delete functions to ease the entry and correction of large data sets. The editor also incorporates a generate option which may be used to generate signals composed by the addition of a number of complex or real sinusoids of varying frequency and amplitude.

Upon selecting option 1 from the master menu, a two digit filename should be entered. All PCS filenames take the form

PCS##.EXT

##	=	a user-defined two figure decimal number
EXT	=	one of a series of extensions used to denote the file type: input data file, control file, output data file etc.

The menu, displayed at the bottom of the screen, offers the following options:

Fetch
Scroll
Copy
Insert
Delete
Generate
ESCape

An option is chosen by pressing the key shown in parentheses in the menu. This is normally the first letter of the option, e.g. F for Fetch.

The upper part of the screen is dedicated to displaying the input data entered in the selected file. The column headings in this area are Cyc, RIN and IIN. These are cycle number, real data component and imaginary data component respectively.

1. Fetch

Allows the user to move the display to a given cycle number.

2. Scroll

Scrolls the display upwards by one cycle each time it is invoked.

3. Copy

Allows a block of data to be copied from one part of the file and appended to the end of the file.

4. Insert

Used to insert data at a given point in a file. To insert the first data point in a new file, press carriage return when prompted for the cycle number.

5. Delete

Deletes all input data between two given points in the file.

6. Generate

This option is used to generate a signal consisting of a number of sinusoids of varying frequency and amplitude. For complex transforms, a maximum of four different sinusoids may be combined. For real transforms, each of the two real input signals may be composed of two different sinusoidal components.

Generate also offers the ability to load an externally generated tabular data file as an input data file. The file should have two columns, separated by at least one space character. The name should be of the standard PCS## format with the extension .DAT. Each column should hold 16 bit hexadecimal data; the first column representing real values and the second column imaginary values. An extract from such a file is shown below.

```
00FA 65B2
ABA3 562E
0000 34A2
12D2 8F02
```

For both internally and externally generated input data files, it should be noted that for an n point transform, the file should contain at least 3n data points. This is required such that the simulator has sufficient data to perform one complete load-transform-dump sequence. If a sufficient number of data points are not supplied, the data will be padded with zeros when loaded into the simulator. When Generate is used to create sinusoidal inputs, a file of the correct length is created automatically by the software.

Generate also has the added benefit of automatically generating a control file of the correct length. This is true for all three generate options: sinusoidal inputs, inverse transforms and externally supplied tabular data.

When Generate is selected, the following prompts will be displayed:

Forward or Inverse transform *	Transform type
Size	Size of transform
Real or Complex	Type R or C to select real or complex transform
Overlap	Percentage by which data is overlapped. Valid responses are 0%, 50% and 75%
External data supplied	Load data held in an external file ?

If external data is not supplied, then the subsequent prompts will request the frequencies and amplitudes of the sinusoids which comprise the input data stream.

Window Operator	You may choose a Rectangular, Hamming or Blackman-Harris window operator.
Overflow Detection (Y/N)	If the response to this question is Y, then the simulator will assume that bit 3 of the mode control word is set. See data sheet for further information.

* See example 3 for further details on inverse transforms

Once all the parameters have been entered, the samples will be generated and stored in the required file.

Pressing Escape returns control to the master menu.

2. EDIT CONTROL FILE

The control file defines the state of the INEN (Input Enable) and DEF (Reset) signals for each cycle of the input data file. If the Generate option is used to create the input data file, the control file will be generated automatically. The control file should contain three cycles for every data point in the data input file.

If the control file is longer than the input data file (.DIN) then the input file will be recycled until the end of the control file is reached. Conversely, if the control file is shorter than the input data file, the simulation will terminate at the last cycle defined in the control file.

If the control file is to be generated manually, the editing options available are similar to those for input data file creation; namely Fetch, Scroll, Copy, Insert and Delete.

Automatically generated control files contain nine preamble cycles, which are used to reset the device and, thereafter, the three cycles per data point required by the simulator. This means that for a 256 point transform, for example, the input data file will contain 768 points and the control file 2313 cycles.

3. RUN SINGLE PASS SIMULATOR

The simulator takes the control and data files specified by the user as the basis of the simulation run. The options offered by the simulator are described below:

1. Halt

This is used to temporarily or permanently halt a simulation run. A record is kept of how many cycles had been simulated and the simulator may be restarted from that point by using the Run option.

2. Run

Starts the simulator from the cycle shown in the status display.

Once the simulation run has been completed, interrupted by reaching a breakpoint or paused by the user, a new menu is displayed which offers the following options:

Scroll
Fetch
Extract
Escape

Scroll and Fetch are used to view the data in the same way as when editing an input data file. Extract generates a file, called PCS##.RES, which contains two columns of data; the first being the real component and the second the imaginary component of each frequency bin of the transform.

3. Breakpoint

Allows the user to define the cycle at which the simulator will pause prior to starting the simulation run, thereby allowing the results generated up to the breakpoint to be viewed.

4. Plot

Presents a graphical view of either the input or the output waveform. It also displays the magnitude of the complex output.

5. Initialise

Resets the cycle number to 1.

6. Variables

This option is used to define the variable watchlist, i.e. which variables will be displayed after each cycle when the simulation is completed or paused. Placing an 'X' next to a variable name adds that variable to the watchlist, pressing carriage return advances to the next variable. The variables that may be added to the watchlist are:

Input Variables:	RIN	Real input data
	IIN	Imaginary input data
Control Variables:	INEN	Active low signal which starts load process
	DEF	Active low signal which resets model
Output Variables:	ROUT	Real output data
	IOUT	Imaginary output data
	S3_0	Accumulated block floating point (BFP) shift value
	DAV	Data available signal
State Variables:	DUMP	Output data memory pointer
	LOAD	Input data memory pointer
	STAGE	Number of FFT pass
	GROUP	Number of butterfly group
	SAMPL	Number of butterfly
	WKSP	Beginning of work space address
	OPSP	Beginning of output space address
	MODE *	FFT mode word (Auxilliary Data Input)
	IPSHF	Butterfly input data BFP shift value
	OPSHF	Butterfly output data BFP shift value
	DLSHF	Delayed output data BFP shift value
	OVFLW	BFP overflow flag
Memory Variables:	MEM0-7	Memory word 0-7 x (offset + 1)

* Bit 15 of the MODE variable indicates the end of a valid load process and the start of the butterfly processing. This is not used in the real device. Refer to the data sheet for mode word format.

The display allows a total of twelve variables to be displayed simultaneously.

7. Escape

Returns to the master menu.

4. RUN BATCH SIMULATOR

This option has been included to speed up those simulation runs where a trace file, listing the values of a number of variables for each cycle, is unnecessary. In batch mode, up to six simulations may be performed serially, with each taking only two thirds of the time required in single pass mode, on average. The output of the simulator is a PCS##.RES file for each input file listing real and imaginary frequency bin data. The options offered by the batch simulator are:

1. Queue

The input data filenames are specified using this option. Up to six filenames may be entered, each separated by a carriage return.

2. Run

Initiates a simulation run for all the files selected via the Queue option.

3. Abort

This option will abort the simulation of the current input file and start the simulation of the next input file in the queue.

4. Halt

Aborts the current simulation and returns control to the user. Selecting Run at this stage will start the simulation process once more from the first file in the queue.

5. Escape

Returns to the master menu.

SIIMULATION EXAMPLES

Example 1 - Square wave using external data file

This example demonstrates how an external data file may be used to supply the data points for a simulation run.

The first task is to generate a text file, using a text editor, describing the square wave. The filename should be of the form PCS##.DAT, where ## is a two figure number between 00 and 99. The contents of the file will describe a square wave where the real component varies between zero and positive full scale values with the imaginary component always set to zero. Hence, the file should look like this:

0000 0000
(30 lines as above)
0000 0000
7FFF 0000
(30 lines as above)
7FFF 0000

This basic 64 line block should be repeated 12 times to yield a file 768 lines long. This is three times the required transform size, namely 256 points, in order to feed the simulator enough data points to perform a complete load-transform-dump cycle.

Now, invoke the PCS program and follow the steps listed below:

<CR>	Displays the master menu (note: <CR> = Carriage Return)
1	Selects Edit Input Data File option
## <CR>	Where ## is the name of the PCS##.DAT file containing the square wave data
G	Selects Generate option
F	Selects forward transform
256 <CR>	Selects 256 point transform
C	Complex transform
0 <CR>	0% overlap
Y	Signifies that an external .DAT file is the source of the input data
R	Use a rectangular window function
N	No overflow detection

The software will now start generating the .DIN file and displays the current sample number near the bottom of the screen. In total, 767 samples will be generated. When sample generation is complete, the prompt "View Data Y/N" will be displayed. Press N at this point to continue to the next phase.

Now type the following:

3	Selects single pass simulator option
## <CR>	Define input data file name
P	Select Plot
I	Select input signal
R	Selects real part of input signal
1	Zoom factor 1

The amplitude-time plot of the input signal is displayed. It can seen that it varies between zero and positive full scale with three cycles in total. To run the simulation type the following:

ESCAPE	Returns to the simulator menu
V	Select variables option. Select the following variables only: RIN IIN INEN DEF ROUT IOUT S3_0 DAV For the remainder, press <CR> when prompted
0 <CR>	To specify zero memory offset.
R	Starts the simulation run.

The simulator will run till cycle number 2313. When the simulation is complete, the trace file will be displayed. It lists the cycle number in the first column and the values of each of the watchlist variables after each cycle. Fetch and Scroll may be used to inspect this file. Extract creates an output file, named PCS##.RES, which lists the real and complex components of each of the frequency bins in tabular hexadecimal form. Pressing ESCAPE returns to the simulator menu.

When the simulator menu is displayed, type the following:

P	Select Plot
M	Magnitude of output data
2	Zoom factor 2

This will display the magnitude of the forward fast Fourier transform of the square wave. As expected, harmonics of the fundamental frequency can be seen with their amplitude decreasing as frequency increases.

Example 2 - 1024 Point With Sinusoidal Data

In this example, the Generate function will be used to create a waveform composed of two sine waves of different frequency and amplitude. To do this, follow the instructions below:

Invoke the PCS program and type the following:

<CR>	Displays master menu
1	Select Edit Input Data File
## <CR>	Where ## is the name to be given to the new data file
G	Invokes Generate function
F	Forward transform
1024 <CR>	Size of transform
C	Complex
0 <CR>	0% overlap
N	No external data file
10 <CR>	Frequency of first signal
0.8 <CR>	Amplitude of first signal
Y	Signifies that another signal is to be added to the input signal
20 <CR>	Frequency of second signal
0.4 <CR>	Amplitude of second signal
N	Signifies that no more sinusoids are to be added to the input signal
H	Hamming window
N	No overflow detection

The software now generates the required input waveform, which is 3071 cycles in length. The hexadecimal input data may be viewed at this stage. To continue to the next stage press N at the "View Data Y/N" prompt.

To simulate the device with the input defined above:

3	Selects single pass simulator
## <CR>	Specify input file name
P	Plot
I	Input waveform
R	Real component
1	Zoom factor

This displays the form of the input wave.

ESCAPE	Returns control to the simulator menu
V	Define watchlist. Select the first eight variables (as in example 1)
0 <CR>	Memory offset
R	Runs the simulation

The simulation runs to 6150 cycles. When complete, the trace file may be viewed. Pressing ESCAPE returns to the simulator menu. Now type:

P	Plot
M	Magnitude
3	Zoom factor

This will display the magnitude of the fast Fourier transform calculated by the simulator. The two peaks generated by the two sinusoids are clearly visible.

Note that higher frequency components peak is 6dB lower than that of the lower frequency peak. This is as predicted by theory.

Example 3 - Generating Inverse Transforms

Inverse transforms may be generated using output data files produced by PCS or by employing a user generated data file containing frequency data. The procedure employed to generate an inverse transform from both file formats is essentially the same.

1. User Generated Data Files

As with forward transforms, the PCS simulator accepts data files containing two columns of data, seperated by at least one space character, where the first column represents the real component of the data and the second column the imaginary component. For inverse transforms, each row of the data file represents a particular frequency bin; the first row being the D.C. bin and so on.

The inverse transformation of a pure sinusoid will be performed. This will illustrate clearly the link between the input data file containing frequency information and the output signal calculated by the simulator. The first step is to create a file 256 lines long, called PCS##.DAT. The contents of this file should be as shown below. This file may be easily generated using a line editor with block cut and paste facilities.

```
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
7FFF 0000
0000 0000
(248 lines of zero data)
0000 0000
```

Invoke PCS and type the following when the master menu is displayed:

1	Edit Input Data File
## <CR>	Enter name of .DAT file
G	Select Generate option
I	Inverse transform
256 <CR>	Selects 256 point transform
C	Complex data
0 <CR>	0% overlap
Y	Signifies that an external file holds the data
N	No overflow detection

The software will now start generating data samples. After the 255th sample, the warning "Insufficient data: padding with zero" will be displayed. This is due to the fact that the simulator always expects sufficient data to carry out a complete load transform dump cycle, whereas the data file contains only one third of the data required for such a cycle. However, padding the data with zeros gives the same end result. When the prompt "View Data Y/N" is displayed, press N to continue to the next phase:

3	Selects single pass simulator
## <CR>	Define input data filename
R	Run simulation

The simulation will run for 2313 cycles. Now type:

<ESCAPE>	Returns to simulator menu
P	Select plot option
O	Output signal
R	Real component
2	Zoom factor

The display will show a sinusoid whose first peak is at the left hand edge of the graph. Now type the following:

<CR>	To select a further plot
O	Output signal
I	Imaginary component
2	Zoom factor

The display shows another sinusoid of equal amplitude and frequency to the first, but lagging in phase by 90°.

2. PCS Generated Data Files

All PCS simulation runs allow the user to produce a .RES file listing the contents of each of the frequency bins in tabular format (see section 3, paragraph 2 for information on the Extract option). The data contained in this file is in the correct format to be fed directly into PCS as a .DAT file.

In order to use the .RES file in this manner it must be renamed from PCS##.RES to PCS##.DAT via the DOS RENAME command. Ideally a new filename should also be chosen, e.g. rename PCS01.RES to PCS02.DAT. This reduces filename confusion as other files with the name PCS01 will already exist in addition to PCS01.RES. Once the file is renamed, the procedure for calculating an inverse transform is exactly the same as that described above for user generated .DAT files.

Additional Example Files

The PCS distribution disk contains three external data files comprised of test data taken from the silicon compiler used to design the PDSP16510. Multiple 64 point transform data is provided in the file FFT64.DAT which includes four different signal blocks of 64 points each. Thus the 256 output points show four different responses in sequence. Normal 256 point transform data is provided in the file FFT256.DAT and 1024 point transform data is provided in the file FFT1024.DAT. All files are run with a rectangular window function applied to the data. To use these files they must first be copied to files which PCS recognises as external data files, i.e. they should be copied to filenames of the form PCS##.DAT. See example 1 for further information on external data files.

APPENDIX 1

PDSP16510 FFT Processor Model

Although the internal algorithms have been developed to mimic those in the device, the internal structure and method of processing are merely functional and not gate level equivalents. Pipeline effects on data values have been accounted for but the model does not provide an exact representation of device operation in real time.

The interface for this model has been rationalised for clarity and does not provide all the control signals used by the real device. The model incorporates complex data I/O paths which are controlled by INEN and DEF signals. These are considered sufficient to provide an accurate functional simulation of the device. Load and dump clocks are simulated internally and although load and dump rates are varied according to the active FFT process they are obviously tied to the system clock, represented by the simulator call.

The real device performs four butterflies in 12 system clock cycles. This model incorporates only one data path structure and is set to process one butterfly every three cycles, thus completing four butterflies in 12 cycles or calls from the simulator. This infers that for transform sizes with fewer or an equal number of butterflies (16, 64 or 256 point), each sample in the data file must be entered over three cycles. Output data will also be spread over three cycles. In order to fit 1024 point transform simulations into the maximum cycle count of 9999, the butterfly process rate has been increased to one per cycle. The data file need only repeat sample data over two cycles to allow one complete transform process (1280 cycles) to complete within the loading period (2048 cycles). This mechanism was developed to permit the model to handle the extended I/O periods required by overlapped transforms and does not represent any structure in the real device.

The GENERATE function in the input data editor allows for this pseudo clock structure. If you are using the INSERT function, this clock structure must be accounted for.

Internal state variables are used merely to monitor the state of the FFT process and do not represent any registers, storage or control structures in the real device. The memory area is defined as an 8x256 word array and the simulator will trace any column of 8 words by entering a memory offset value from 0 to 255 in the memory variable list. The memory is partitioned by each FFT process according to its particular needs. All FFT processes use a load space in which to deposit input data, a work space in which the butterfly processes are executed and an output space from which completed transforms are clocked out. This arrangement permits loading, processing and dumping of data to be simultaneous processes. The load space is normally twice the size of the selected transform to permit overlapped sampling modes. The work space and output space are equal to the size of the transform. Thus, for a 64 point transform the load space is 128 words long (offsets 0 to 15), the work space is 64 words long (offsets 16 to 23) and the output space is also 64 words long (offsets 24 to 31).

Model Limitations

Although the model was designed to be bit accurate, tests indicate that bit 0 of the result is not always the same as that produced by the PDSP16510 when processing identical data.

FREQUENCY SYNTHESISER APPLICATIONS

SP5070 2.4GHz FREQUENCY SYNTHESISER

In the block converter type of receiver shown in Fig.1, the local oscillator signal to the first mixer is a fixed frequency and is often controlled by a dielectric stabiliser. A more stable control of frequency may be obtained by using a phase locked loop synthesiser with crystal reference, such as the SP5054 or SP5055. Although either of these products could be used in such an application, the need for a 16-bit input word to select the operating frequency is a disadvantage when the device is situated at the remote end of the receiver downlead. Local generation of the necessary data word using CMOS logic elements or sending a suitably coded data word along the downlead are possible solutions to the problem, but it may be simpler to use the SP5070 fixed frequency synthesiser. The SP5070 can synthesise any frequency in the range 300MHz to 2.4GHz when fed with the appropriate reference.

The C-band satellite signals cover the range from about 3.67 to 4.17GHz and usinq a frequencv doubling mixer with low side oscillator injection, down conversion to the 950-1450MHz standard IF range will occur if the oscillator frequency is set at 1.36GHz. Since the multiplication ratio between the local oscillator and the reference input to the SP5070 is 256, a 5.3125MHz crystal reference will be required, as shown in Fig 2. A similar system but with a much greater degree of local oscillator multiplication could be used in a block down converter for 12GHz DBS reception.

The SP5070 can also be used for head end tuning in single conversion receivers by feeding a variable reference frequency along the downlead from the indoor unit. Since the reference is at a very different frequency from the IF the two can be easily separated with a minimum of filtering.

The variable reference frequency for this type of system is best generated using a low frequency synthesiser contained in the indoor unit, and a system using the GPS NJ8820 is shown in Figs 2 and 3.

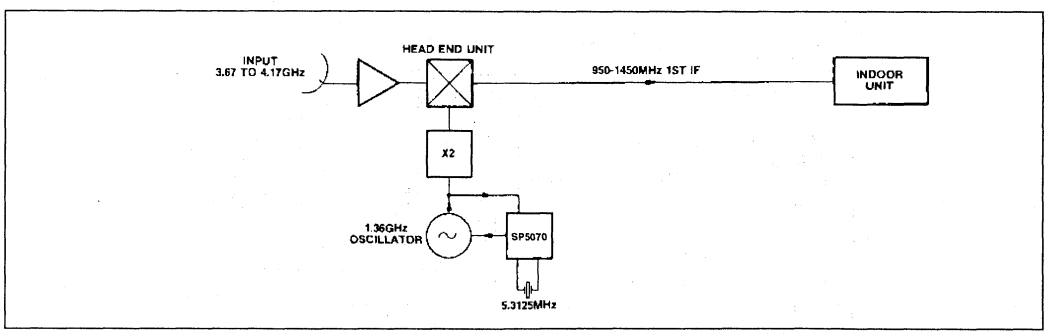


Figure 1: Synthesised Block Down Converter System

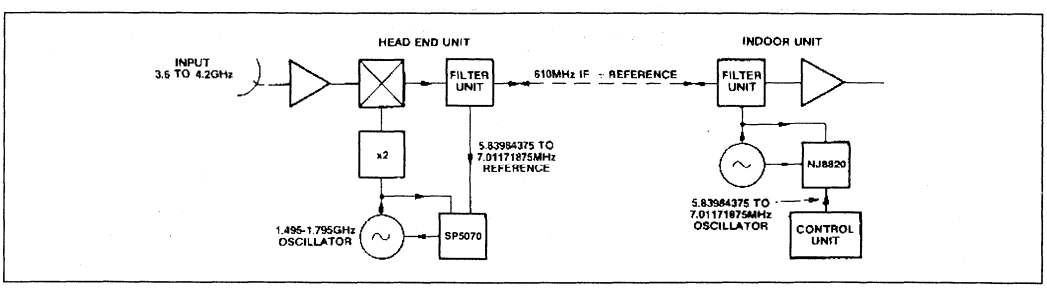


Figure 2: Block Diagram of Synthesised Single Conversion Receiver

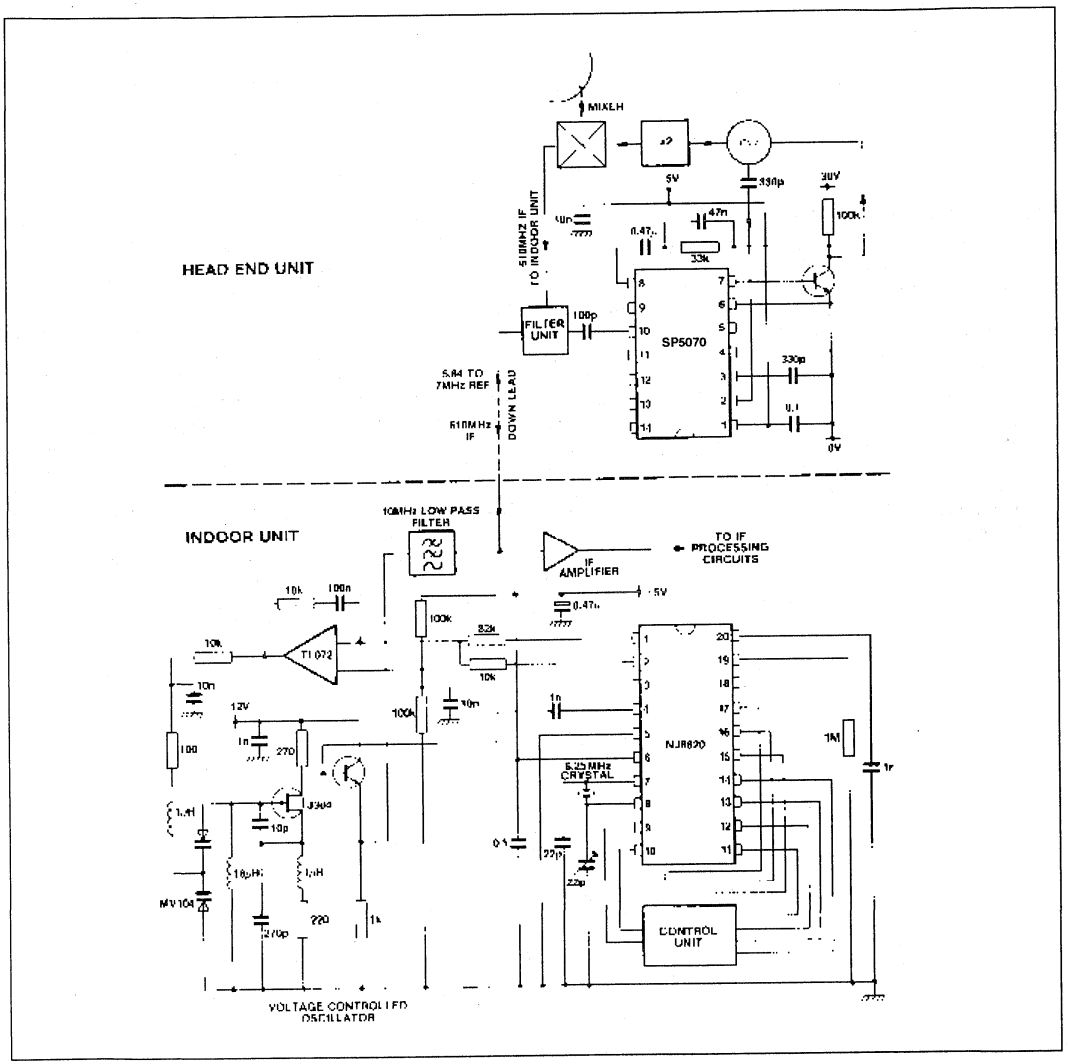


Figure 3: Circuit of Double Synthesiser

Using a frequency doubling mixer or x2 multiplier and assuming a 3.6 to 4.2GHz tuning requirement, 610MHz IF and a low side local oscillator, the required oscillator frequency range will be 1.495 to 1.795GHz.

The ratio of reference frequency to synthesised frequency of the SP5070 is 256, giving a reference requirement to be produced by the NJ8820 of 5.83984375 to 7.01171875MHz. Similarly if the step size at the mixer is set at 10MHz the reference step becomes 19.53125kHz.

Although these numbers are beginning to look somewhat formidable, the NJ8820 is capable of producing the required output if a 6.25MHz reference crystal is used with the reference counter programmed to divide by 160, or 320 including the fixed divide by 2. Frequency adjustment to anywhere in the required range can now be obtained by setting the ratio of the N counter in the NJ8820 as follows:

$$\text{Step size of NJ8820} = \frac{\text{crystal reference frequency}}{160 \times 2}$$

$$= \frac{6.25\text{MHz}}{320}$$

$$= 19.53125\text{kHz}$$

Programming input for reference counter.

= binary 160

= 00010100000

To tune a minimum frequency of 5.83984375MHz (for a mixer LO input of 2.99GHz) requires input to the NJ8820 N counter of:

$$\frac{5.83984375\text{MHz}}{19.53125\text{kHz}} = 299$$

= 0100101011

NOTE: Using this scheme the ratio at the NJ8820 N counter is equal to the local oscillator mixer input frequency in GHz x 100. For example, if the LO input to the mixer is required to be 3.15GHz the ratio will be 315 or binary 0100111011.

The flexible programming ability of the NJ8820 will allow a receiver using this system to be controlled using either a microprocessor or a multi-position switch in conjunction with a PROM as shown in the NJ8820 data sheet.

SP5054 2.6GHZ SYNTHESISER

Block conversion receivers generally produce a first IF ranging from 950MHz to 1450MHz in the case of the US C-band services, and from 950MHz to 1750MHz for the proposed DBS services. Using a high side local oscillator necessary to obtain the required tuning range, and with a European standard 480MHz 2nd IF the required frequency range will be 1430MHz to 2230MHz. Although calculating a suitable reference frequency to just cover the maximum requirement will give the smallest step size and therefore greatest resolution if fine tuning for AFC is used, the step size for any data bit does not coincide with the 19.18MHz standard DBS channel spacing, possibly increasing the complexity of the control software. A better solution might be to increase the reference frequency to 4.795MHz giving a rather curious minimum step size of 0.14984375MHz but producing a 19.18MHz step for the 27 data bit.

For a C-band system, a suitable reference frequency might be 5MHz giving a 20MHz step for the 27 data bit with a minimum step size of 0.15625MHz and a theoretical maximum synthesised frequency of 2.5598GHz, well above that required for a 612MHz IF.

REMOTE PROGRAMMING OF SP5000 SERIES SYNTHESISERS

Although remote programming of SP5000 series synthesisers appears complex at first sight, with a requirement for Chip Enable and Data Clock signals as well as the frequency data, the task can be greatly simplified using the circuit shown in Fig 6.

Obviously it is most convenient to have only a single downlead between the head end and indoor units of a satellite receiver, and therefore the system shown in Fig 6 sends data along the downlead at a relatively low frequency (125kHz) which can be easily filtered from the IFsignal. The data is sent as a burst of 125kHz, representing a '1', and a logic '0' by the absence of signal. The duration of each logic bit is 64 cycles of 125kHz equivalent to a time period of 0.512ms (see Fig.5).

Data Clock and Chip Enable inputs are generated locally from the data input to avoid having to encode these on the overworked downlead, the process being initiated by the leading edge of the first data bit which must always be logic 1. Since the first data bit is used only by the band select or ccntrol outputs, this causes no frequency setting limitation and the second bit is still available for use as a polarisation setting control.

CIRCUIT DESCRIPTION (FIG.6)

The 567 phase locked loop tone decoder chip is set to detect the bursts of 125kHz, producing a low output at pin 8 when the input is present. Loop and output filter components are selected to give fast response consistent with reasonable noise performance. As the first bit in the data stream must always be a logic '1', the negative-going edge at pin 8 produced at the beginning of bit 1 is used to trigger the R-S flip-flop formed by two CMOS NAND gates thus initiating the decoding process. Pin 8 also provides the data input to the SP5000 series device whilst the R-S flip-flop provides Chip Enable.

Once the R-S flip-flop is triggered, the output of the 567 oscillator, at or very close to 125kHz (depending on the presence or lack of 125kHz at the input) drives the 4040 counter. After 32 cycles of the 125kHz input data stream the Q6 output on pin 2 goes high providing a data clock signal to the synthesiser in the centre of the 64 cycle data period. Data clock pulses will continue from pin 2 until all 16 data bits are clocked, when the Q10 output on pin 14 goes high resetting the R-S flip-flop and terminating the chip enable signal. The R-S flip-flop also resets the 4040 leaving the system to be retriggered by the next data stream.

A suitably encoded data stream can be generated under

program control from a microprocessor or perhaps more easily by gating under program control the divided output from the microprocessor oscillator (often 4MHz, which, when divided by 32 gives 125kHz).

A low pass filter such as that shown in Fig.6 should be inserted between the downlead and data generating logic to prevent harmonics from the logic section interfering with the picture when fine tuning is used. The same filter will also prevent loading of the IF output by the logic.

Although as shown above there are various down conversion systems applicable to satellite reception, all have a requirement for some form of control system. A microprocessor used in this control function usually gives greatest flexibility allowing decoding of remote control and local keyboard inputs, generation of input data for synthesisers, channel display and a program memory feature using a single component.

MICROPROCESSOR CONTROL

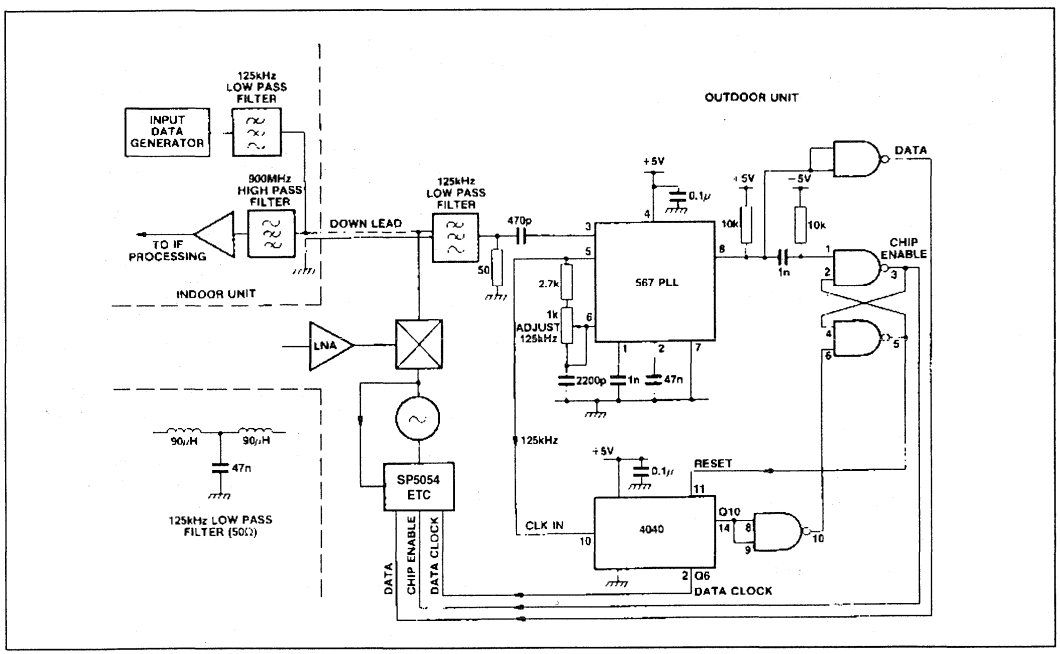


Figure 4: Remote Data Receiver Circuit Diagram

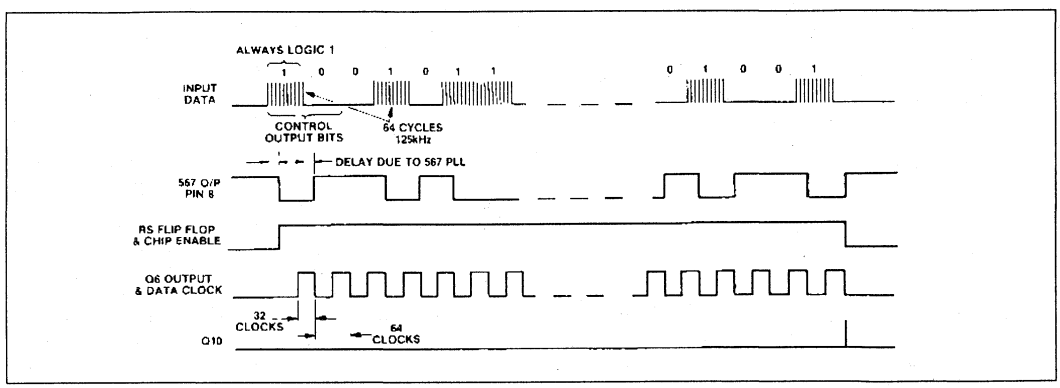


Figure 5: Remote Data Receiver Waveforms

COMPOSITE VIDEO INTERFACING FOR THE VP520S

(Supersedes February 1996 version, AN205 - 1.1)

The existing H.261 evaluation board for the GPS H.261 chipset requires video input from a Gen-locked RGB digital camera and outputs analog RGB and sync for display on an RGB monitor. This is an expensive solution and most people prefer to use a composite video input signal and display on a TV monitor. This application note is intended to provide a reference design for composite video input and output.

The solution used here is provided by four devices from Philips Semiconductors. For the video input three devices are required; TDA8708A, SAA7157 and SAA7151(Note: these three devices may be replaced in the future with the forthcoming Philips SAA7111 VIP Video Input Processor). To provide a CVBS output signal the SAA7188A is used.

The TDA8708A is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32MHz and an input selector.

The SAA7157 Clock signal generator circuit (SCGC) generates all clock signals required for a digital TV system suitable for the SAA7151. The circuit operates in either the phase-locked loop mode (PLL) or voltage controlled oscillator mode (VCO).

The SAA7151 is a digital multistandard colour-decoder (DMSD2-SCART) having two 8-bit input channels, one for CVBS or Y, the other for chrominance or time-multiplexed colour-difference signals, it decodes digital TV signals with line-locked clock in PAL, SECAM and NTSC standards (CVBS or S-video) as well as RGB signals coming from a SCART/peri-TV connector.

8-bit CVBS data (digitized composite video) are fed to the SAA7151. The data rate is 27MHz.

The SAA7188A digital MPEG-compatible Video Encoder (DENC2-M) encodes digital luminance and chrominance into analog CVBS and simultaneously S-Video (Y/C) signals. NTSC-M and PAL B/G standards are supported.

The basic encoder function consists of subcarrier generation and color modulation as well as insertion of synchronization signals. Luminance and chrominance signals are filtered according to the standard requirements RS-170-A and CCIR-624.

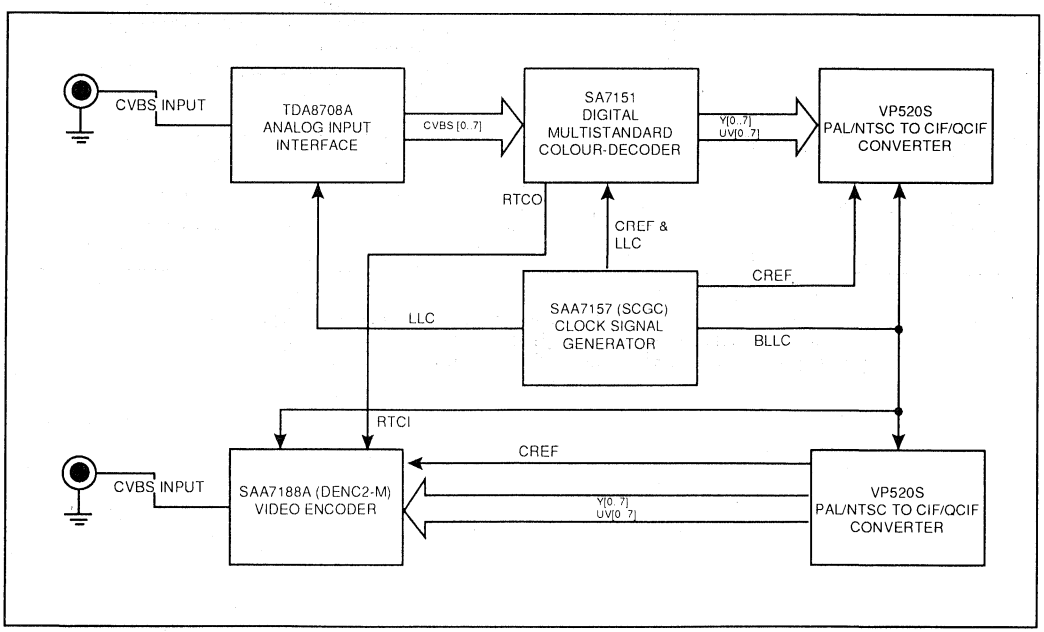


Fig.1 block diagram

SAA7151 PROGRAMMING DETAILS

Function	Subaddress	Data (Hex.)	Result
increment delay	00	64	64 increment delay - set up for generating LLC using DTO etc.
H-sync HSY begin	01	35	35 position of start of sync level synchonisation pulse for PAL
H-sync HSY stop	02	0A	position of start of sync level synchonisation pulse for PAL
H-clamp HSY begin	03	F8	position of start of black level synchonisation pulse for PAL
H-clamp HSY stop	04	CD	position of end of black level synchonisation pulse for PAL
H-sync after PHI1	05	FE	programmable hsync position - not used by H.261 design, Href indicates active video
luminance control	06	01	luminance control - CVBS input, no pre-emphasis, notch filter selected for PAL subcarrier
hue control	07	00	hue control - set to 0 degrees for PAL selected
control #1	08	1F	PAL for forced colour standard and colour killer threshold
control #2	09	1F	SECAM colour killer etc - irrelevant
PAL switch sensitivity	0A	90	PAL switch sensitivity
SECAM switch sensitivity	0B	90	SECAM switch sensitivity - irrelevant
control #3	0C	08	general purpose outputs (unused), chroma gain controlled by loop
control #4	0D	40	colour killer on, UV outputs straight binary, irrelevant SECAM bits
control #5	0E	B0	CCIR levels, colour on, syncs enabled, chroma from CVBS input
control #6	0F	90	auto field detect, 625 lines, PLL closed, TV mode
control #7	10	62	auto standard off, 4:2:2 format
chroma gain reference	11	4F	chroma gain
control #8	12	C0	enable YUV buses, normal vertical noise reduction

NOTE
1. These values are provided for reference and will need some adjustment for individual applications.
2. Refer to SAA7151 data sheet for detailed meaning of register settings.
3. Refer to Philips 1994 Desktop Video Data Handbook for details of I^2C timing details.

SAA7151 PROGRAMMING DETAILS

Function	Subaddress	Data (Hex.)	Result
NULL	00	00	
NULL	39	00	
Input_Port_Control	3A	0C	input_port_control, select straight binary YUV format
			OSD LUTs, CCIR 601 Colour Bars
OSD_LUT_Y0	42	6B	White
OSD_LUT_U0	43	00	White
OSD_LUT_V0	44	00	White
OSD_LUT_Y1	45	52	Yellow
OSD_LUT_U1	46	90	Yellow
OSD_LUT_V1	47	12	Yellow
OSD_LUT_Y2	48	2A	Cyan
OSD_LUT_U2	49	26	Cyan
OSD_LUT_V2	4A	90	Cyan
OSD_LUT_Y3	4B	11	Green
OSD_LUT_U3	4C	B6	Green
OSD_LUT_V3	4D	A2	Green
OSD_LUT_Y4	4E	EA	Magenta
OSD_LUT_U4	4F	4A	Magenta
OSD_LUT_V4	50	5E	Magenta
OSD_LUT_Y5	51	D1	Red
OSD_LUT_U5	52	DA	Red
OSD_LUT_V5	53	70	Red
OSD_LUT_Y6	54	A9	Blue
OSD_LUT_U6	55	70	Blue
OSD_LUT_V6	56	EE	Blue
OSD_LUT_Y7	57	90	Black
OSD_LUT_U7	58	00	Black
OSD_LUT_V7	59	00	Black
Chroma_Phase	5A	3F	phase of sc relative to h-sync
Gain_U	5B	7D	Gains set for White-Black = 100IRE
Gain_V	5C	AF	Gains set for White-Black = 100IRE
Gain_U_MSB, Black_lev	5D	2D	Gains set for White-Black = 100IRE
Gain_V_MSB, Black_lev	5E	3F	Gains set for White-Black = 100IRE
NULL	5F	00	Gains set for White-Black = 100IRE

NOTE
1. These values are provided for reference and will need some adjustment for individual applications.
2. Refer to SAA7151 data sheet for detailed meaning of register settings.
3. Refer to Philips 1994 Desktop Video Data Handbook for details of I^2C timing details.

SAA7151 PROGRAMMING DETAILS (cont'd)

Function	Subaddress	Data (Hex.)	Result
X-Col_Select	60	40	PAL cross colour filter on
Standard_Control	61	06	864 pixels per line, PAL encoding, No real-time control of sc
Burst_Amplitude	62	48	Amplitude of colour burst for PAL
Subcarrier_0	63	CB	Subcarrier frequency
Subcarrier_1	64	8A	set to PAL-B/G
Subcarrier_2	65	09	
Subcarrier_3	66	2A	
Line21_Even_0	67	67	Closed captioning not used
Line21_Even_1	68	68	Closed captioning not used
Line21_Odd_0	69	69	Closed captioning not used
Line21_Odd_1	6A	6A	Closed captioning not used
Encod_Crtl, CC_Line	6B	81	Closed captioning not used - encode inputs on VP port
RCV_Port_Control	6C	20	Syncs active hi, vref on RCV1, hblank on RCV2
RCM, CC-Mode	6D	00	Closed captioning & RCM outputs not used
H-Trigger	6E	0F	Can adjust output hsync referred to input with this
H-Trigger	6F	01	Can adjust output hsync referred to input with this
Fsc_Res_Mode, V-Trigger	70	80	reset subcarrier every eight fields for PAL
Begin_MP_Request	71	F9	RCM2, RCV2 outputs not used
End_MP_Request	72	86	RCM2, RCV2 outputs not used
MSBs_MP_Request	73	60	RCM2, RCV2 outputs not used
NULL	74	00	
NULL	75	00	
NULL	76	00	
Begin_RCV2_out	77	F9	RCM2, RCV2 outputs not used
End_RCV2_out	78	86	RCM2, RCV2 outputs not used
MSBs_RCV2_out	79	60	RCM2, RCV2 outputs not used
Field_Length	7A	70	length of field in half-lines (624 Lines)
First_Act_Line	7B	17	first active line after blank in lines (Line 23)
Last_Act_Line	7C	67	last active line before vertical blank (Line 615)
MSBs_Field_Ctrl	7D	22	msbs of above

NOTE
1. These values are provided for reference and will need some adjustment for individual applications.
2. Refer to SAA7151 data sheet for detailed meaning of register settings.
3. Refer to Philips 1994 Desktop Video Data Handbook for details of I^2C timing details.

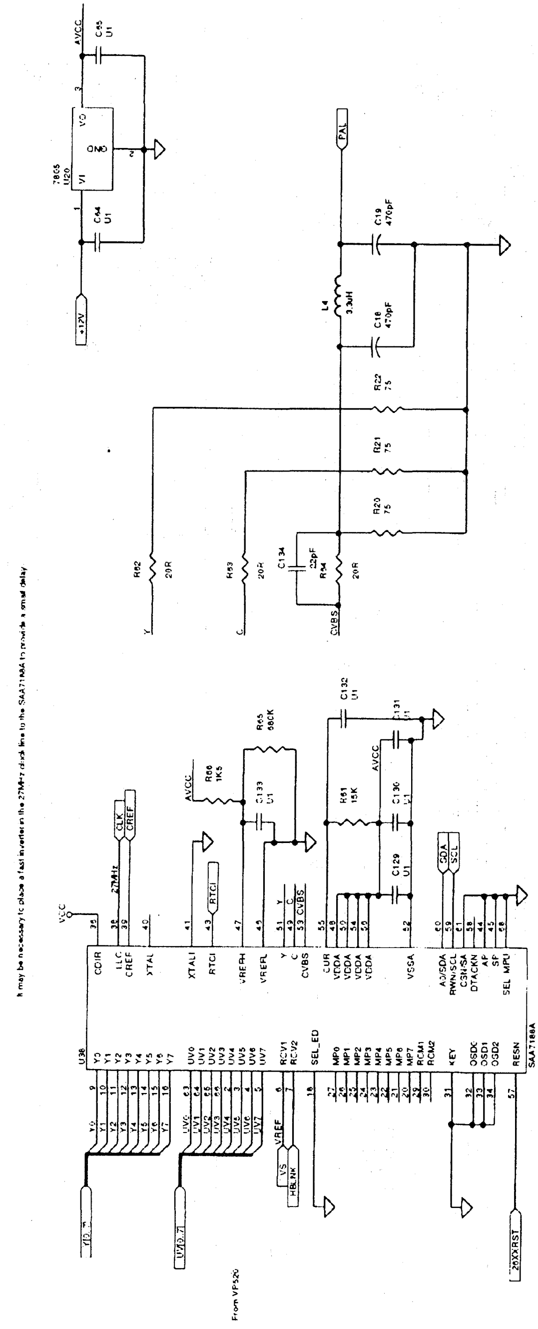

+12V
AVCC
7805
PAL
L4
3.3uH
C19
470pF
C18
470pF
R22
75
R21
75
R20
75
R62
R63
20R
CVBS
CLK
CREF
27MHz
RTCI
SDA
SCL
VS
HBLNK
From VP520
SAA7186A

Fig.2

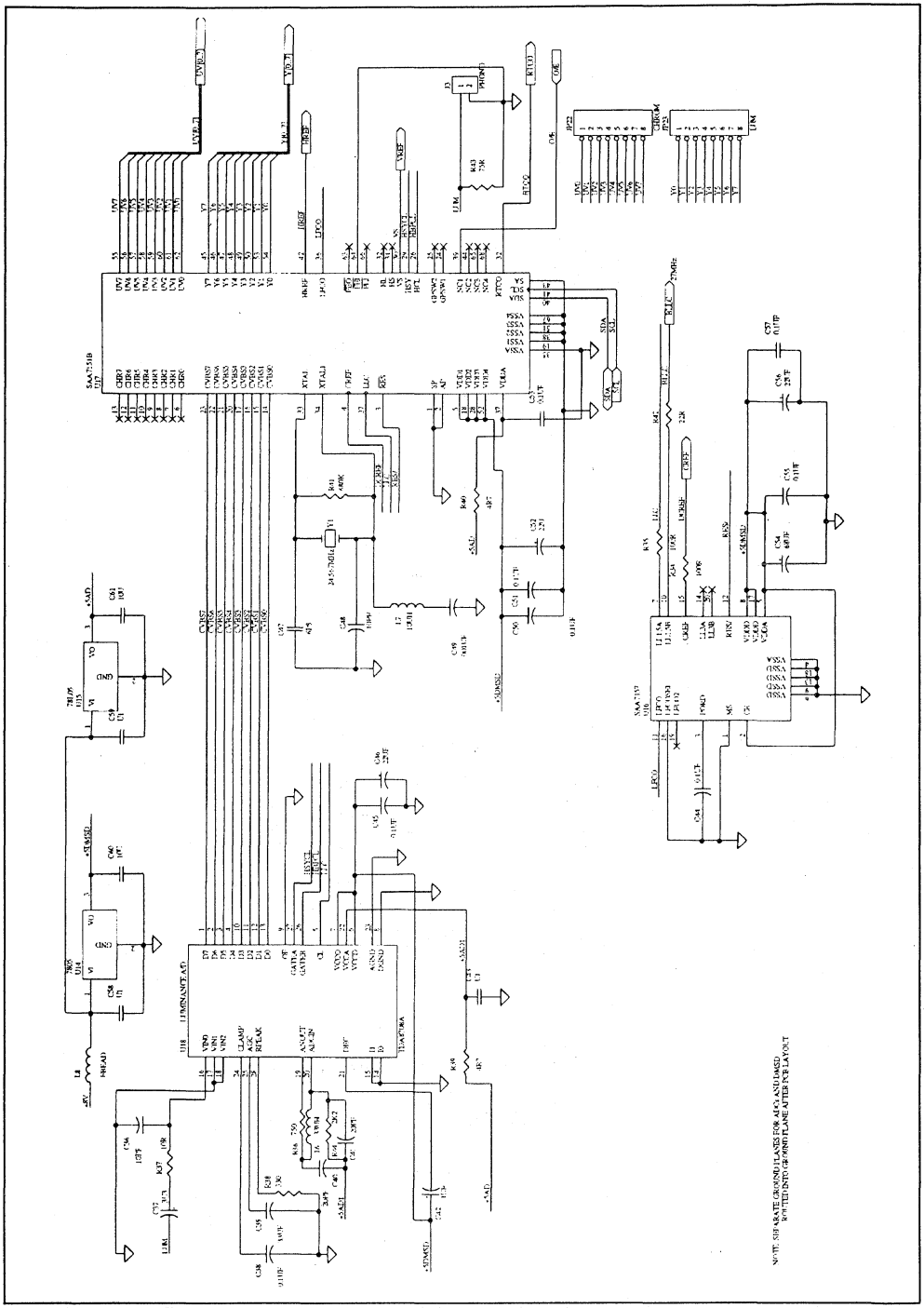


Fig.3

INTERFACING TO THE VP5311/VP5511 VIDEO ENCODER

INTRODUCTION

All references in this document to VP5311 equally apply to the VP5511. Interfacing the video encoder in a complex digital video system requires an understanding of how the encoder synchronizes itself to the rest of the system. The VP5311 simplifies the digital to analog interface by integrating the whole composite encoding function in a single chip. Only a small number of external components are required. It is the digital system interface, however, that has several different implementations depending on the particular system requirements. The purpose of this application note is to describe the different interfacing options on the VP5311 as well as describe the genlock and closed captioning features.

SYSTEM DATA FLOW AND SYNCHRONIZATION

In a typical video system, such as a cable or satellite set top box, there are two sources of video information. One is digital and consists of the primary source of programming material. The other is analog and is sourced by on screen display-OSD, PIP tuner, external antennae, or other analog overlay sources. To control the synchronization of these sources to the actual television receiver a master/slave arrangement is required. Analog video arrives asynchronously with respect to the digital video data, and they both need to be properly synchronized with respect to the NTSC/PAL timing requirements of the receiver. The master/slave synchronization is handled between the video encoder and the MPEG-2 decoder. The VP5311 can work in either master or slave mode to enable it to interface to all MPEG decoders including master or slave only mode decoders.

The driving factor forcing this synchronization are the timing requirements of NTSC and PAL television receivers. In these receivers, synchronization signals in the video source material control the vertical and horizontal timing. There are a precise number of these signals and their timing requirements are very strict to allow compatibility with a wide variety of sources and backwards compatibility with millions of televisions purchased over several decades. In addition to the horizontal and vertical synchronization, colour televisions require a colour burst signal immediately following the horizontal sync. This is a 9 cycle sinusoid of a specific frequency. The receiver needs to phase and frequency lock to this signal in order to properly extract colour hue and saturation information from the video signal source.

SLAVE MODE INTERFACE

A video output subsystem is shown below in Fig.1. In this mode, the MPEG-2 Video Decoder is the master while the VP5311 VEC slaves to it.

In this system PIP, OSD, or analog video from an external source can be overlaid on the digital video source. This is inserted and controlled through a switch on the output of the VP5311 and it's filters. Genlock (the process of synchronising Hs, Vs and the colour sub-carrier) can only be achieved, when the video encoder is in slave mode. In this mode the MPEG-2 decoder synchronizes the HS and VS of the digital video to the analog source and it then outputs the digital video with the embedded TRS (Timing Reference Signals) codes. These codes contain blanking information, field identification, and active video synchronization which is inserted prior to the beginning of the active video line data, corresponding to CCIR Rec 656. This data stream has the formats shown in Fig.2.

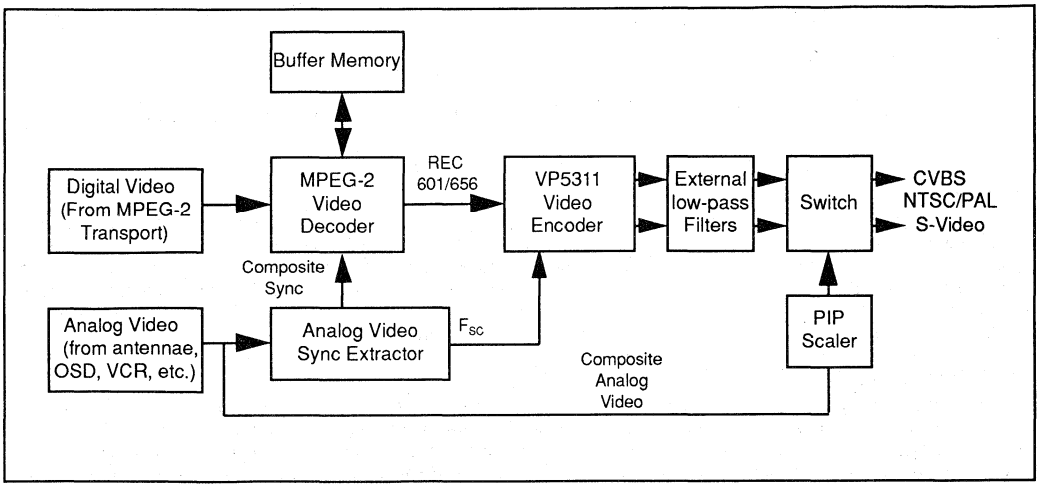
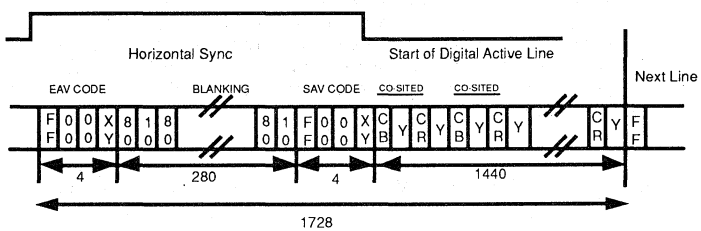


Fig.1 Video Encoder Slave Interface



The XY byte in the EAV and SAV codes has the following bit definitions:

1	F	V	H	P_3	P_2	P_1	P_0

F = 0 during field 1
1 during field 2

V = 0 outside field blanking
1 indicates that this is a field blanking period

H = 0 in SAV (Start of Active Video)
1 in EAV (End of Active Video)

P_3, P_2, P_1, P_0 are protection bits that depend on the states of the previous 3 bits. There function is to allow the correction of 1 bit errors and detection of 2 bit errors.

Fig.2 CCIR Recommendation 656 Data Format for 625/50 system

The REC 656 data consists of 1728 8-bit samples per line for PAL systems while the NTSC system has 1716 samples per line. Each system has 1440 active video samples, while PAL has 12 more blanking codes to give it a total of 1728 samples. The video encoder receives this information at 27 MHz through an 8-bit port. As it receives data, the EAV and SAV codes are decoded and the appropriate digital synchronization signals and field specific colour subcarrier phase (either 0° or 180°) are generated. The active video consists of alternating luma samples separated by either a C_b or C_r sample. It can be seen that there will be 720 luma samples per line while there will be 360 chroma pairs per line. The chroma pairs will be combined with every other luma sample to form a co-sited sample. CCIR REC 656 specifies a 27 MHz sample clock rate, which means the luma data rate is 13.5 MHz, while each chroma sample has a 6.75 MHz rate. Fig. 3 below shows the block diagram of the VP5311:

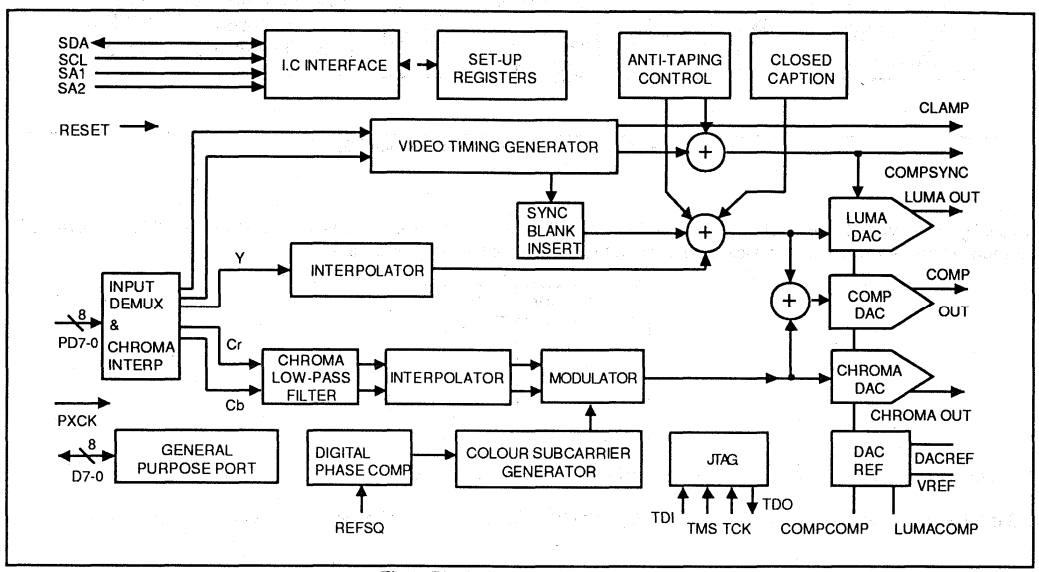


Fig.3 Block diagram of the VP5311

As the VP5311 receives the active video, the chroma samples are filtered and interpolated up to a 27 MHz rate where they are modulated together at the colour sub-carrier frequency, F_{sc}. The luma samples are also interpolated up to 27 MHz. The interpolation process for both the luma and chroma paths are quite simple. The algorithm takes two samples, averages them and then inserts the result between the two original samples. The end result of the interpolation process is that the output rate is doubled from the nominal 13.5 MHz, to 27 MHz. This helps to minimize the sinx/x distortion and quantizing noise that is inherent in digital sampling. After interpolation, the luma samples are combined with the synchronization signals coming from the video timing generator. The luma and chroma data is then converted to analog through three 9-bit DACs. Two DACs are used for S-Video applications where the luma and chroma are separate. The 3rd DAC is used for composite video where the luma and chroma data are numerically summed prior to being converted.

MASTER MODE INTERFACE

The previous example showed the VP5311 operating as a slave to the MPEG-2 decoder. Other systems require the video encoder to operate as the master to control data flow from the MPEG-2 decoder's buffer to the output video monitor. In Master Mode, the video encoder generates HS/VS/FC outputs, that connect to the MPEG-2 decoder. When the decoder receives the Hrizontal Sync control signal, it then outputs the field after a short delay. The synchronization between the MPEG-2 decoder and the VP5311 is critical as the television receiver is expecting a steady stream of video along with the precise sync signals that are embedded in it. This is illustrated in Fig.4.

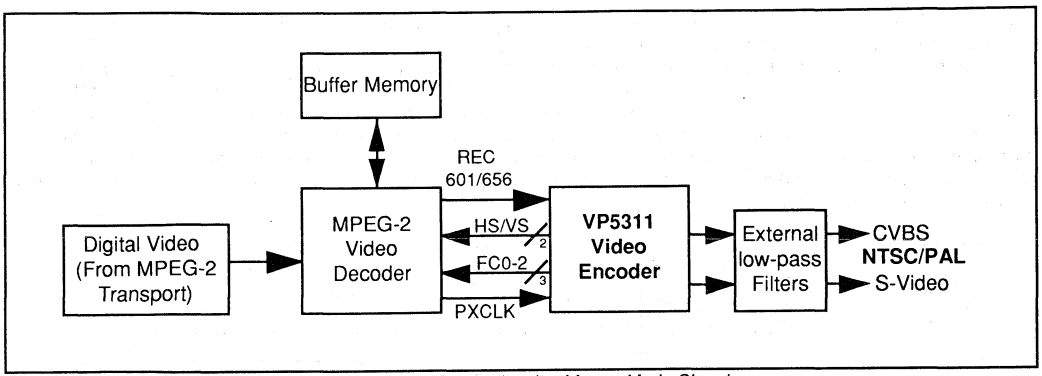


Fig.4 VP5311 Master showing Master Mode Signals

To configure the VP5311 for master mode the TRSEL bit in the GPSCTL register must be set to a '1'. Once in this mode, the GPP (General Purpose Port) is automatically configured to produce the following outputs:

Pin Number	Function
3	VS
4	HS
5	FC0
6	FC1
7	FC2

VS is the start of the field sync datum, in the middle of the equalisation pulses.

HS is the line sync which is used by the preceding MPEG2 decoder to define when to output digital video data to the VP5311.

FC0 - 2 are the field count outputs, defined in the table below:

FC2	FC1	FC0	Field
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Note that only fields 1 - 4 are used in NTSC, so FC2 is not used. In PAL fields 1-8 are used.

The VP5311 asserts the HS signal a certain time prior to the time that the television receiver actually requires a particular line of video. This is because there is an inherent delay through the video encoder and the MPEG decoder. The delay through the MPEG decoder is known as the pipeline delay and will be different with each manufacturer's MPEG decoder. To accommodate this delay, the VP5311 can be programmed to advance the timing offset of the HS pulse it presents to the MPEG decoder. This is illustrated in Figure 5 below. The programmed value is a number that represents the number of 13.5 MHz pixel clocks between the time the HS pulse goes active to the time that the decoder puts the first sample on the bus.

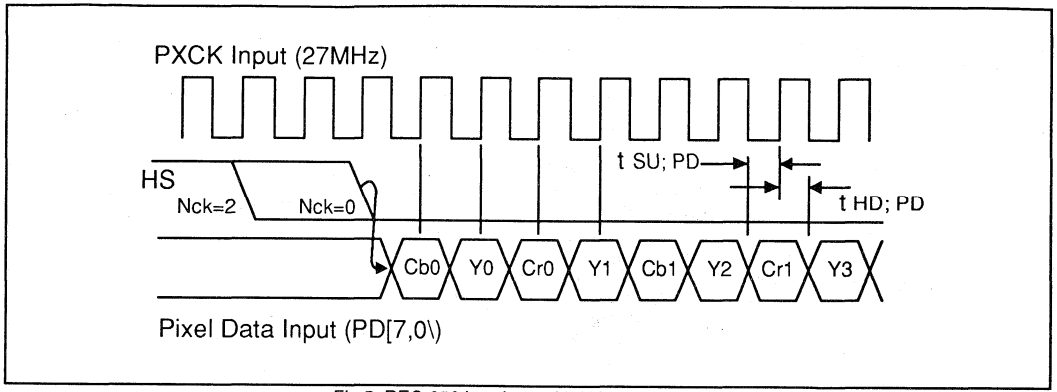


Fig.5 REC 656 interface with HS output timing

PROGRAMMING HS OFFSET

The position of the falling edge of HS relative to the first data Cb0, can be programmed in HSOFFM-L registers, see Figure 5. This is done by programming a 10 bit number called HSOFF into the HSOFFM and HSOFFL registers, HSOFFM being the most significant two bits and HSOFFL the least significant eight bits. A default value of 07EH is held in the registers.

The value to program into HSOFF can be looked up in the table below:

For NTSC and PAL-M:

Nck	HSOFF	Comment
0 to 120	126 to 6	HS normal (64 cks)
121 to 138	863 to 801	HS pulse shortened*
184 to 857	800 to 127	HS normal (64 cks)

For PAL-B, G, H, I, N:

Nck	HSOFF	Comment
0 to 131	137 to 6	HS normal (64 cks)
132 to 194	869 to 807	HS pulse shortened*
195 to 863	806 to 138	HS normal (64 cks)

*HS pulse shortened means that the width of the pulse will be less than the normal 64 13.5MHz clock cycles.

Where Nck = number of 13.5MHz clock cycles between the falling edge of HS and Cb0 (first data I/P on PD7-0), see Figure 5. Decreasing HSOFF advances the HS pulse, (numbers are in decimal).

The interruption in the sequence of HSOFF values is because the HS signal is jumping across a line boundary to the previous line as the offset is increased. The register default value is 7EH, and this sets Nck to 0, ie. the HS negative edge and Cb0 are co-incident in NTSC mode.

Example 1, if an offset of eight 13.5MHz clock cycles is required (pipeline delay of 592.6ns) then:

HSOFF = 126 - 8 = 118 (76H) for NTSC

HSOFF = 137 - 8 = 129 (81H) for PAL

Example 2, if an offset of 300 13.5MHz clock cycles is required (pipeline delay of 22.222us) then:

HSOFF = 800 + 184 - 300 = 684 (2ACH) for NTSC

HSOFF = 806 + 195 - 300 = 701 (2BDH) for PAL

GENLOCK

When combining video from different sources, the Horizontal Sync, Vertical Sync. and colour sub-carrier phase need to be synchronized, as shown below:

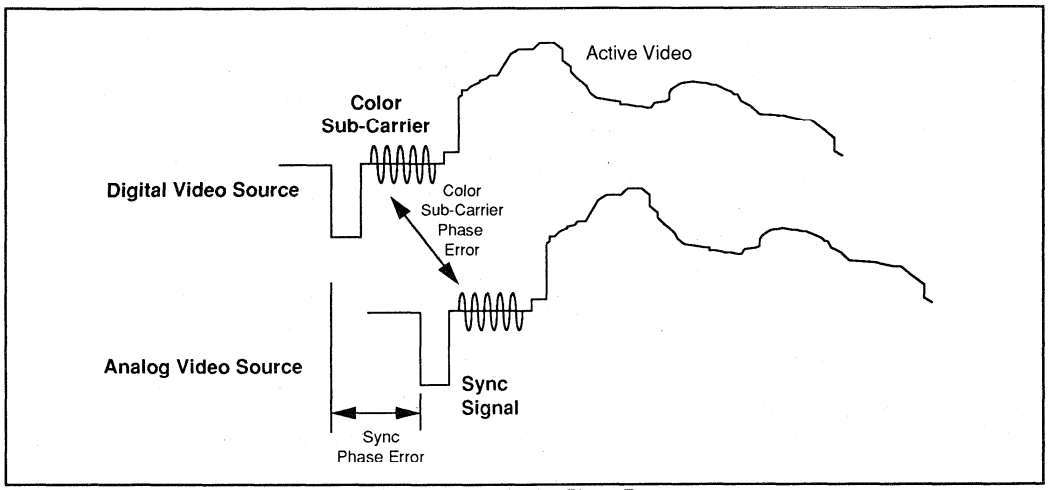


Fig.6 Synchronization Phase Errors

The process of synchronizing Horizontal Sync (HS), Vertical Sync (VS), and the colour sub-carrier is known as Genlock. Synchronizing HS and VS is required so that the analog video overlay is properly positioned on top of the video originating from the digital video source. For this process, the genlock circuit needs to remove the synchronization phase errors.

Obtaining colour sub-carrier synchronization is required for a very different reason. In Figure 6 above it implies that by removing HS and VS phase errors, the colour sub-carrier synchronization would occur by default. However, the colour sub-carrier phase from two different sources can vary significantly. The video receiver aligns its colour sub-carrier phase to the colour burst signal of the incoming video. No colour hue and saturation information would be present, if the receiver were phase locked to the colour burst of the digital source, and the information being displayed was from the analog source. Thus, colour sub-carrier genlock is required to maintain hue and saturation accuracy when video information is being displayed from one source while the video receiver is synchronized to the colour sub-carrier of another.

VP5311 GENLOCK

The VP5311 implements colour sub-carrier genlock. It requires the use of an external circuit that extracts the synchronization signals as well as providing a colour sub-carrier signal, as indicated in Figure 7. This signal is a continuous square wave that is phase locked to the colour sub-carrier of the incoming analog video signal. Horizontal and Vertical Sync genlock must be performed in a separate circuit, the MPEG-2 decoder being the logical location. There are several different circuits that perform this HS/VS sync extraction and colour sub-carrier generation.

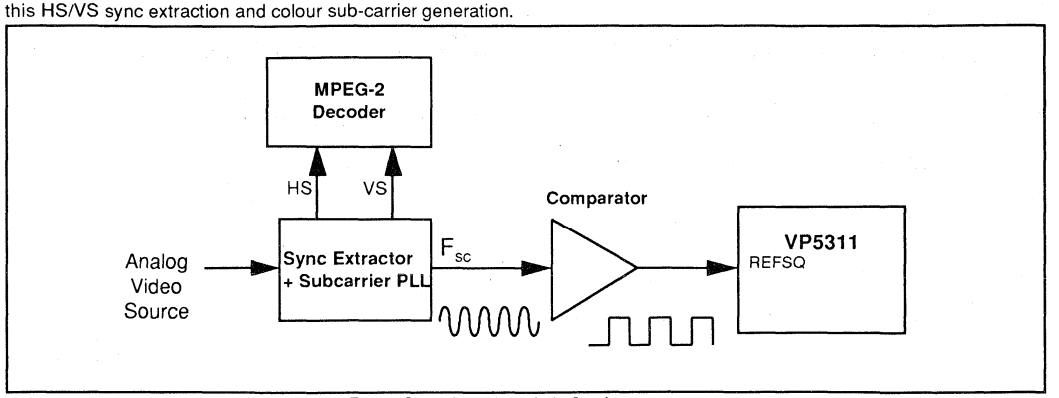


Fig.7 Generic Colour Sub-Carrier extracror

When genlocking to an external analog source, the digital source needs to slave to the analog signal. As analog video arrives asynchronously, the MPEG decoder must be synchronised to the extracted analog HS & VS signals, Fig.7. The MPEG decoder will then generate a REC656 data stream with the embedded synchronisation bytes and the VP5311 locks to these in slave mode, effectively locking to the analog source.

The subcarrier is recovered from the analog source and converted to a digital level signal and then input to the REFSQ pin. A digital phase locked loop, in the VP5311, then locks its own internally generated subcarrier to the incoming square wave. Once genlock has been achieved the digital signal can be overlaid on top of the analog one (or vice versa), this is useful for OSDs, PIP etc..

This sync extractor and subcarrier PLL circuit can use a variety of video decoder products presently available. Several of these are low-cost for use in high volume, consumer TV markets; some devices combine HS and VS into a composite sync which may need to be separated externally. The colour-subcarrier signal will be a continuous frequency (particular to NSTC or PAL system) and phase aligned to the colour sub-carrier of the source. Since this is a sinusoidal signal and the VP5311 expects a digital square wave, a squaring function needs to be implemented. A comparator with TTL output operation would fulfil this function. The VP5311 will then phase lock its colour subcarrier generator to that of the external analog source.

CLOSED CAPTIONING

Introduction

The VP5311 has the facility to generate closed caption data on line 21, as used on NTSC systems in the USA. Closed captions are used as a means of subtitling programs to assist people with poor hearing or for an alternative language to the audio channel. Full screen format text can also be sent and displayed.

The data to be displayed needs to be sent over the I²C bus to the VP5311 and this document describes how this software should operate.

Closed Caption System

This is specified in the EIA-608 Line 21 Data Services for NTSC and should be referred to for further information. Field 1 is used for normal caption service while field 2 tends to be reserved for special use such as a second language.

Two bytes of data are coded on the line 21 of each field, see Figure 8, below. The data is coded as NRZ data with odd parity after a clock run-in and framing code. The clock run-in frequency = 0.5034965MHz which is related to the nominal line period, D = H / 32 or D = 63.55555556 / 32µs.

Two types of data are sent, printing and non-printing characters. The latter are two byte pairs that are transmitted twice on successive frames and are used for control purposes, such as the display position. Printing characters are text to be displayed on the screen; generally ASCII code is used with odd parity in the MSB, but there are some other codes for special and non-English characters.

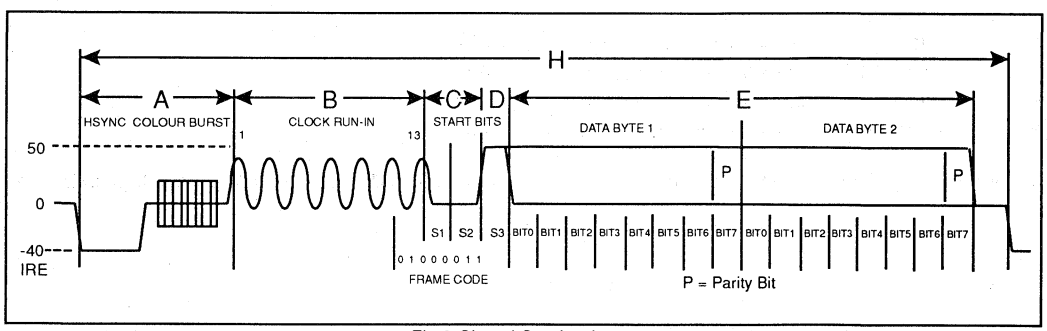


Fig.8 Closed Caption format

Interval	Description	Encoder minimum	Encoder nominal	Encoder maximum
A	H-sync to clock run-in	10.250µs	10.500µs	10.750µs
B	Clock run-in[2, 3]		6.5D (12.910µs)	
C	Clock run-in to third start bit[3]		2.0D (3.972µs)	
D	Data bit[1, 3]		1.0D (1.986µs)	
E	Data characters[4]		16.0D (31.778µs)	
H	Horizontal line[1]		32.0D (63.556)	
	Rise / fall time of data bit transitions[5]		0.240µs	0.288µs
	Data bit high (logic level one)[6] Clock run-in maximum	48 IRE	50 IRE	52 IRE
	Data bit low (logic level zero)[6] Clock run-in minimum	0 IRE	0 IRE	2 IRE
	Data bit differential (high - low) Clock run-in differential (max. - min)	48 IRE	50 IRE	52 IRE

Notes

1. The Horizontal line frequency f_H is nominally 15734.26Hz ±0.05Hz. Interval D shall be adjusted to $D = 1/(f_H \times 32)$ for the instantaneous f_H at line 21.
2. The clock run-in signal consists of 7.0 cycles of a 0.5034965MHz (1/D) sine wave when measured from the leading to trailing 0 IRE points. The sine wave is to be symmetrical about the 25 IRE level.
3. The negative going midpoints (half amplitude) of the clock run-in shall be coherent with the midpoints (half amplitude) of the Start and Data bit transitions.
4. Two characters, each consisting of 7 data bits and 1 odd parity bit.
5. 2 T Bar, measured between the 10% and 90% amplitude points.
6. The clock run-in maximum level shall not differ from the data bit high level by more than ±1 IRE. The clock run-in minimum level shall not differ from the data bit low level by more than ±1 IRE.

DESCRIPTION OF VP5311 OPERATION

Five registers are used in the VP5311 for closed caption, four to store the data to be transmitted (**CCREG1 - 4**) and one to control the operation (**CCTL**). These are detailed below:

Address	Reg Name	Description
F0	**CCREG1**	1st byte to be encoded onto line 21, field 1
F1	**CCREG2**	2nd byte to be encoded onto line 21, field 1
F2	**CCREG3**	1st byte to be encoded onto line 21, field 2
F3	**CCREG4**	2nd byte to be encoded onto line 21, field 2

Note in the above 4 registers the MSB is ignored, this is the parity bit automatically added by the VP5311, odd parity is used.

F4		**CCTL**		1st byte to be encoded onto line 21, field 1				
bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	F2EN	F1EN

Only two bits are contained in the **CCTL** register, F1EN enables closed captioning onto line 21 field 1, F2EN is the same but for field 2. By default both bits are at '0' disabling closed captioning.

When a byte is received into a **CCREG** register it is encoded on the next available field, the registers are then set to the null byte (80H). Null bytes are ignored by the decoder (except for non-printing characters, see above), so gaps in the transmission of characters do not matter as long as these are filled with null characters. The 7 cycles of clock run-in and the odd parity bits are automatically added by the VP5311 before transmission.

Software Operation

Normally at initialisation the F1EN bit from reg **CCTL** is set to a '1' to enable closed caption on line 21 field 1. If encoding on line 21 field 2 is required the F2EN bit is set (both can be set if desired).

Two or four characters are programmed into the **CCREG**s for transmission. To ensure correct timing of the data relative to the field number the software should read the **HANC** register, address 06H (shown below).

bit	7	6	5	4	3	2	1	0
	-	-	DFI2	DFI1	DFI0	-	-	ACTREN

DF2-0 Digital Field Identification, read only.
000 = Field 1, 011 = Field 4

The software should mask out all bits except bits 4 & 3. In NTSC mode, the field counter runs 0-3 for fields 1-4, this field number should be stored. It is preferable to transmit a character pair over the I²C at the beginning of field 2 and 4 for line 21 field 1 encoding, and at the beginning of field 1 and 3 for line 21 field 2 encoding. This should ensure that the data is programmed before the relevant encoding field occurs. To prevent the current data from being overwritten, before the next byte pair is sent to the VP5311, the software should check that the field number has incremented by 2 from the previously read number.

Note that the non-printing characters used for control of the decoder are required to be sent twice i.e. on consecutive frames, this provides some error protection. If the software is interrupted before sending the second pair and therefore misses the next frame it is necessary to repeat the control character transmission from the start. This is not really a problem with printing characters as the VP5311 will send a 'null' character by default if it receives nothing. The 'null' character is ignored by the decoder.

Example of caption Coding

Information sent is shown with corresponding line data (2 bytes) in hex, without parity, below:

Caption Mode

EDM	**EDM**	**RDL**	**RDL**	*Information Sent*
142c	142c	1420	1420	*Hex data, no parity*

R1M	**R1M**	**RDL**	**RDL**	**HE**	**LL**	**Osp**	**fr**	**om**	**spG**	**PS**
1140	1140	1429	1429	4845	c4c4c	4f20	6672	6f6d	2047	5053

R3M	**R3M**	**RDL**	**RDL**	**VP**	**53**	**2sp**	**CI**	**os**	**ed**	**spC**	**ap**	**ti**	**on**
1240	1240	1429	1429	5650	3533	3220	436c	6f73	6564	2043	6170	7469	6f6e

R5M	**R5M**	**RDL**	**RDL**	**fo**	**rsp**	**NT**	**SC**	**spo**	**nNU**	**spl**	**in**	**esp**	**21**
1540	1540	1429	1429	666f	7220	4e54	5343	206f	6e80	206c	696e	6520	3231

R14M	**R14M**	**RDL**	**RDL**	**Ha**	**ve**	**spa**	**spn**	**ic**	**esp**	**da**	**y!**
1440	1440	1429	1429	4861	7665	2061	206e	6963	6520	6461	7921

Text Mode (same message)

RT	RT	H E	LL	Osp	fr	om	spG	PS	N/L	N/L	*Information Sent*
142b	142b	4845	c4c4c	4f20	6672	6f6d	2047	5053	142d	142ad	*Hex data, no parity*

RT	RT	VP	53	11	spsp	Cl	os	ed	spC	ap	ti	on	N/L	N/L
142b	142b	5650	3533	3131	2020	436c	6f73	6564	2043	6170	7469	6f6e	142d	142d

RT	RT	fo	rsp	N T	S C	sp o	n NU	sp l	in	esp	21	N/L	N/L
142b	142b	666f	7220	4e54	5343	206f	6e80	206c	696e	6520	3231	142d	142d

RT	RT	H a	ve	sp a	spn	ic	esp	da	y!	N/L	N/L	N/L	N/L
142b	142b	4861	7665	2061	206e	6963	6520	6461	7921	142d	142d	142d	142d

Abrieviations:

EDM Erase Non-Displayed Memory
RnM Row n Monochrome (Display position is row n, where n is replaced by a number)
RDL Resume Direct Loading
RT Resume Text
SC Show Caption
N/L New Line
NU NULL
sp SPACE

MASTER MODE TIMINGS

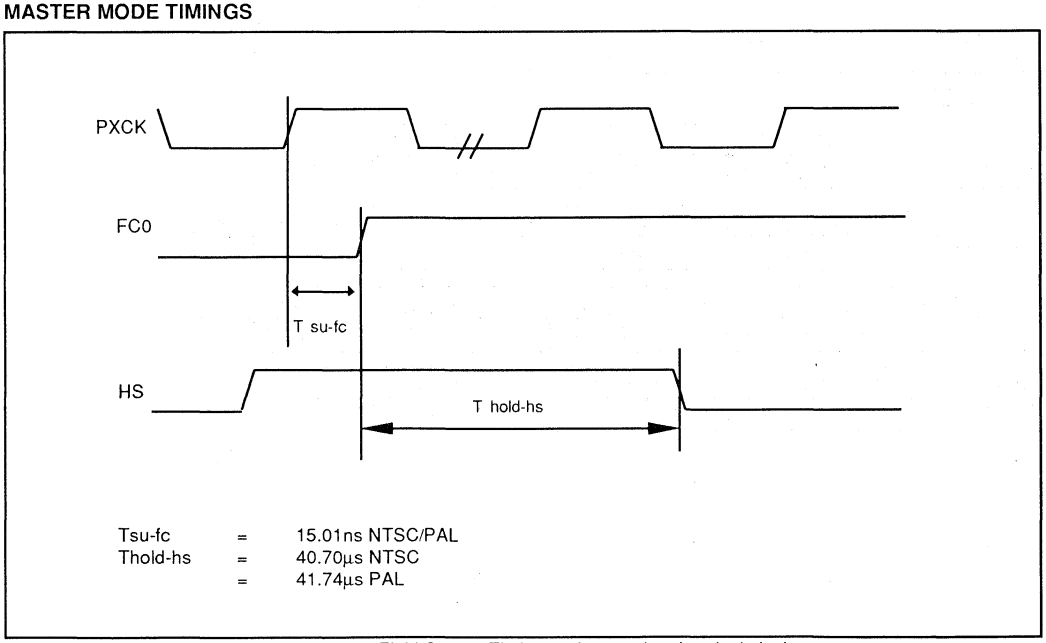
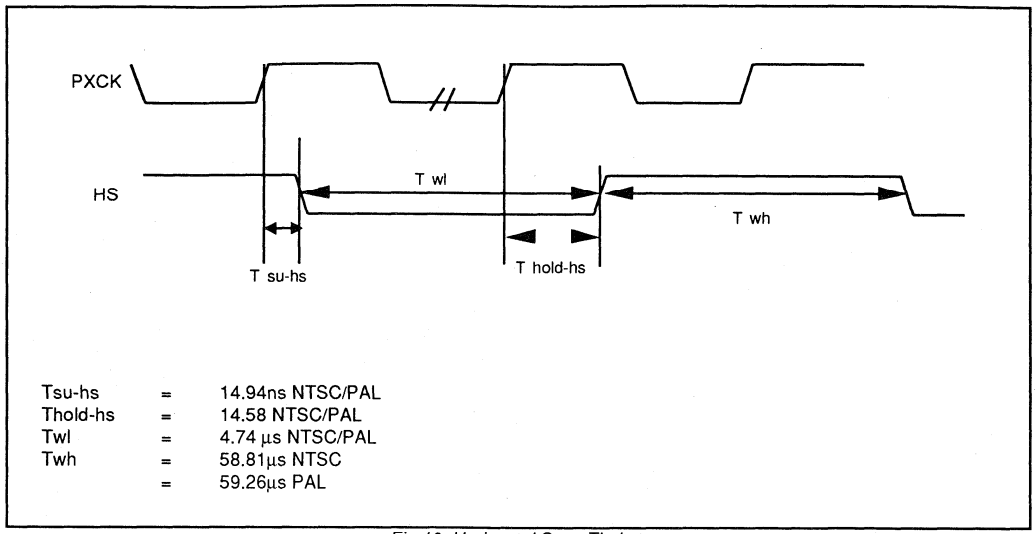
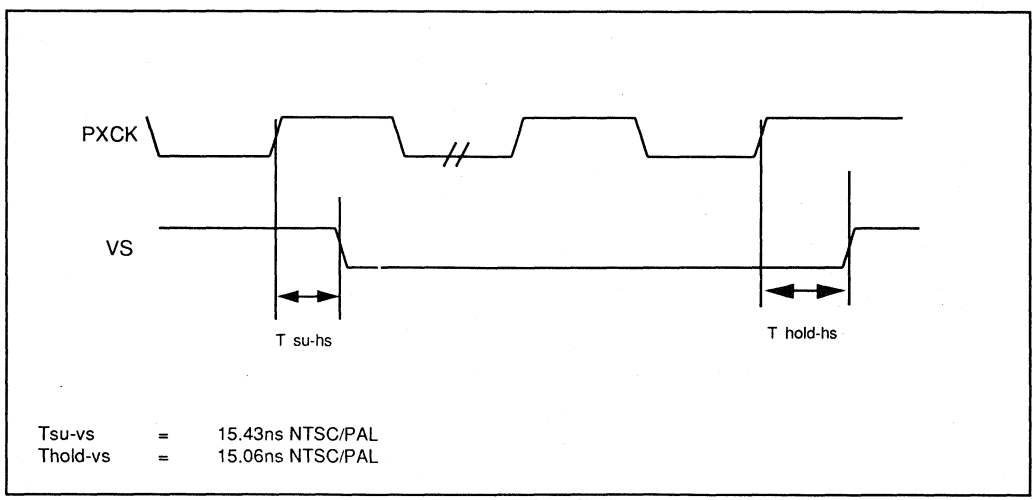


Fig.9 VP5311 Field Control Timings referenced to the pixel clock



Tsu-hs	=	14.94ns NTSC/PAL
Thold-hs	=	14.58 NTSC/PAL
Twl	=	4.74 µs NTSC/PAL
Twh	=	58.81µs NTSC
	=	59.26µs PAL

Fig.10 Horizontal Sync Timings



Tsu-vs	=	15.43ns NTSC/PAL
Thold-vs	=	15.06ns NTSC/PAL

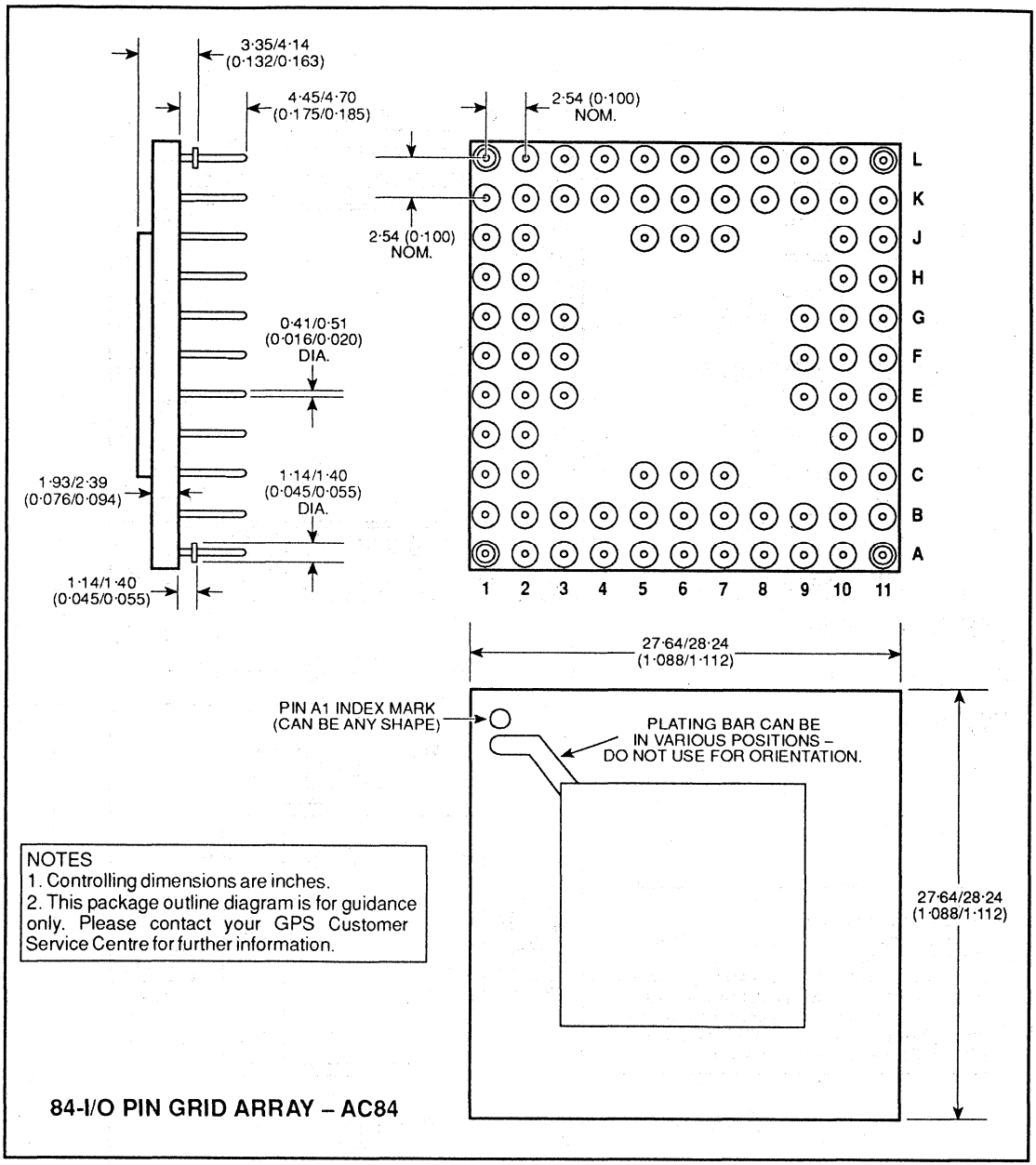
Fig.11 Vertical Sync Timings

Section 11
Package Outlines

NOTES

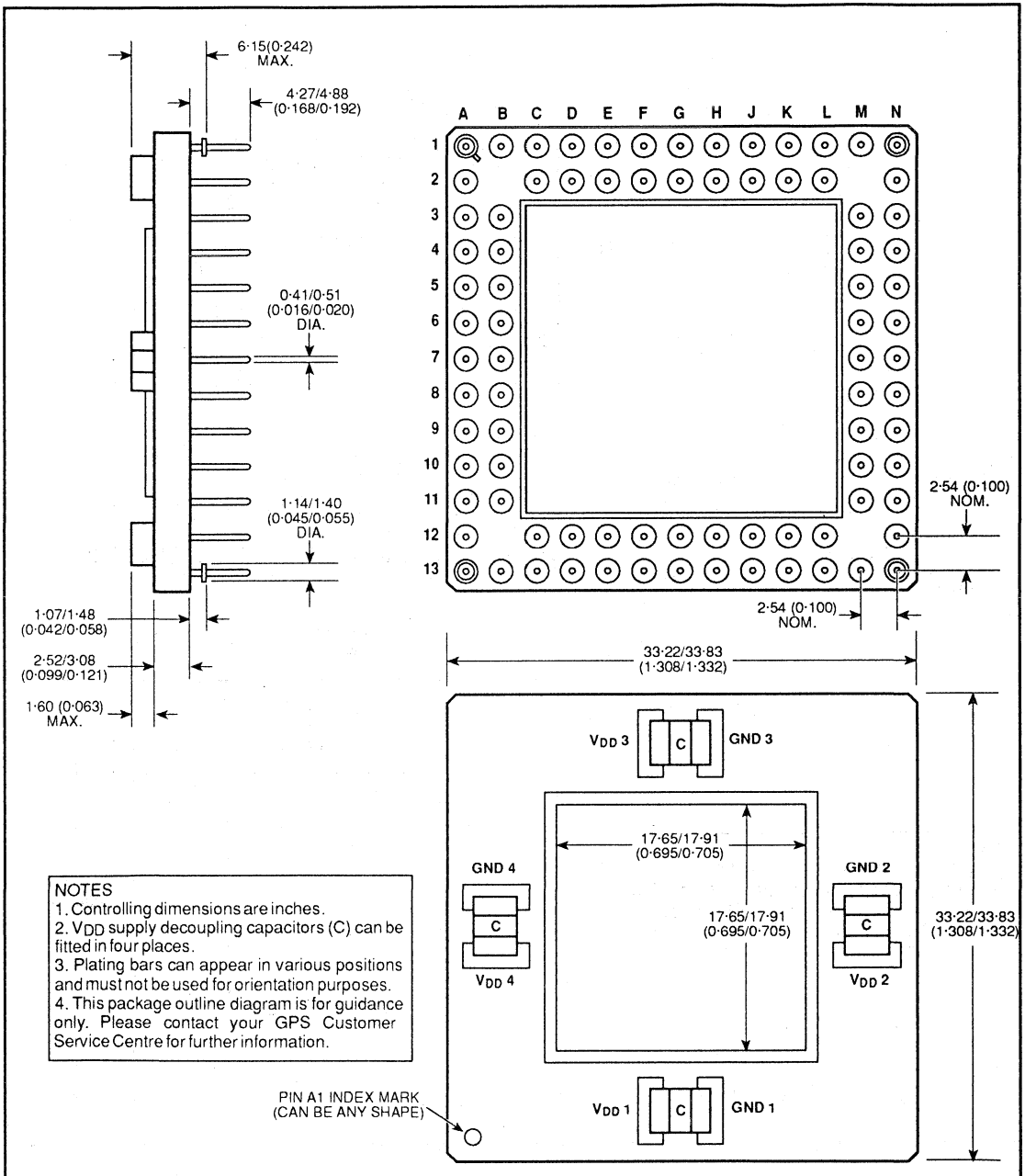
1. Dimensions are shown thus: mm (in).
2. Unless otherwise indicated, controlling dimensions are in inches.
3. All package outline diagrams are for guidance only. Please contact your nearest GPS Customer Service Centre for further information.

GEC PLESSEY
SEMICONDUCTORS



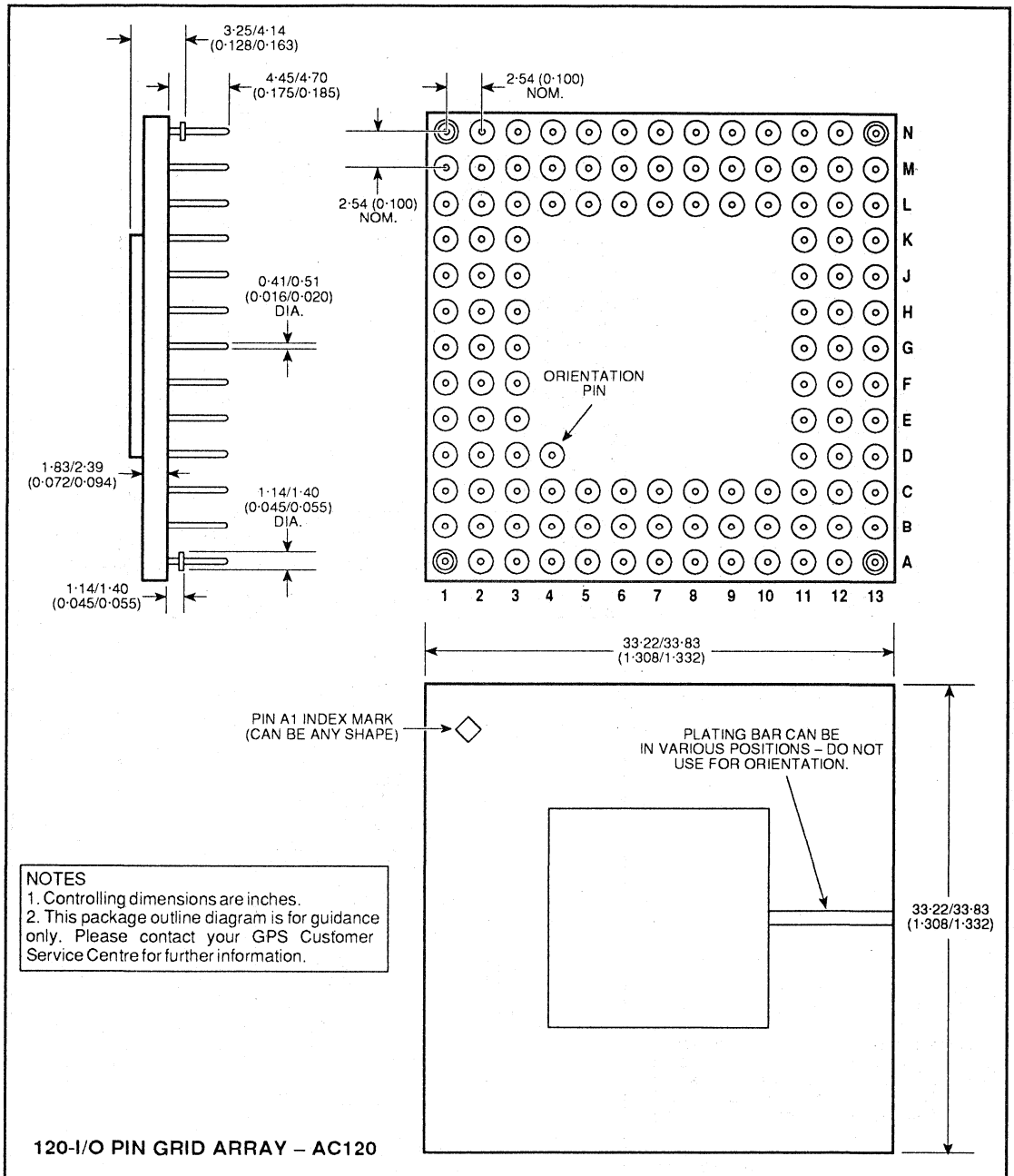
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

84-I/O PIN GRID ARRAY – AC84



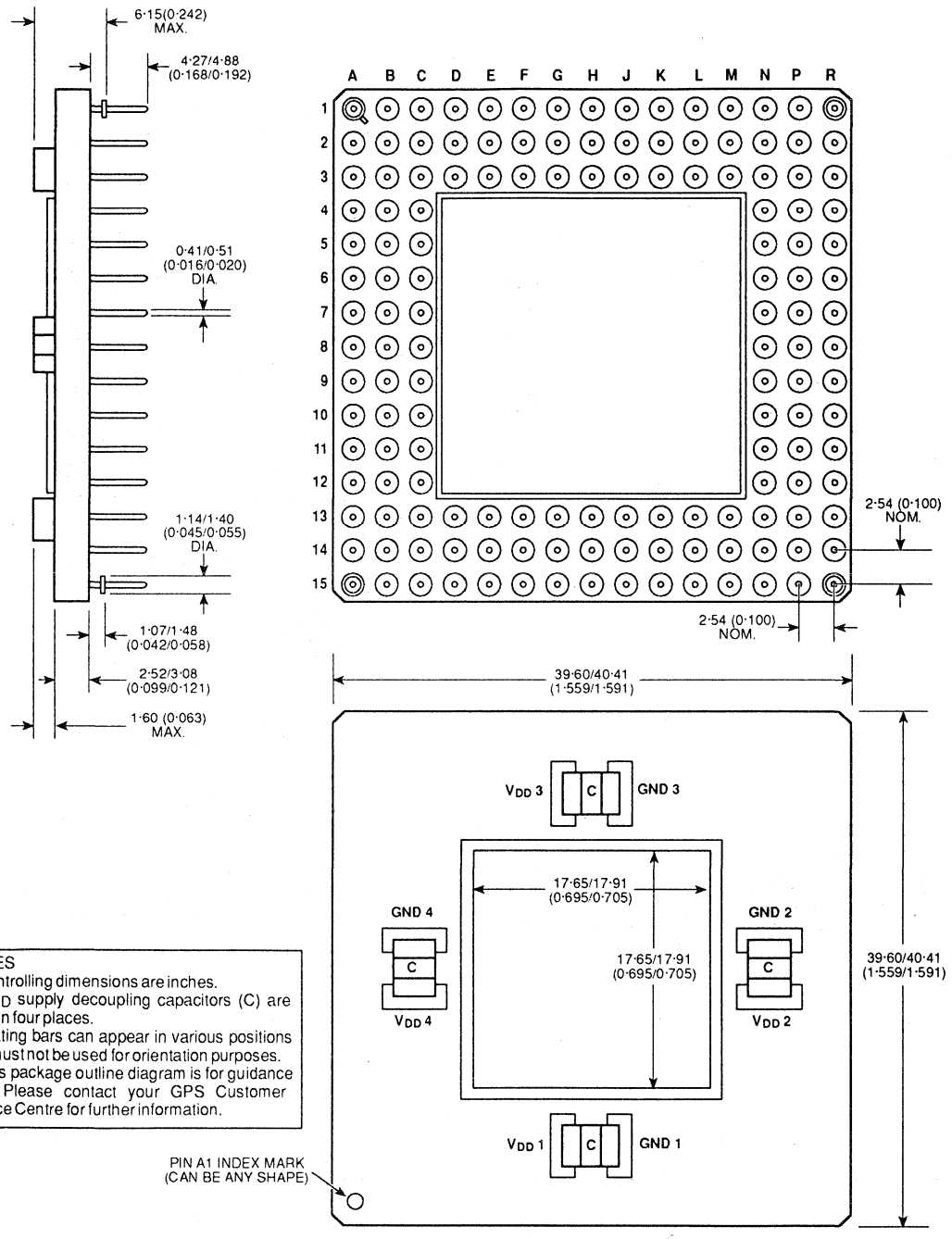
NOTES
1. Controlling dimensions are inches.
2. V_{DD} supply decoupling capacitors (C) can be fitted in four places.
3. Plating bars can appear in various positions and must not be used for orientation purposes.
4. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

84-I/O PIN GRID ARRAY – AC84 (POWER)



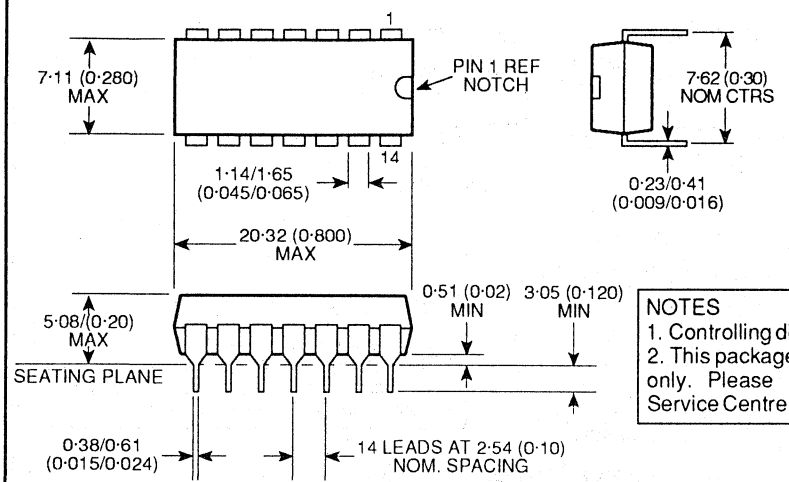
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

120-I/O PIN GRID ARRAY – AC120



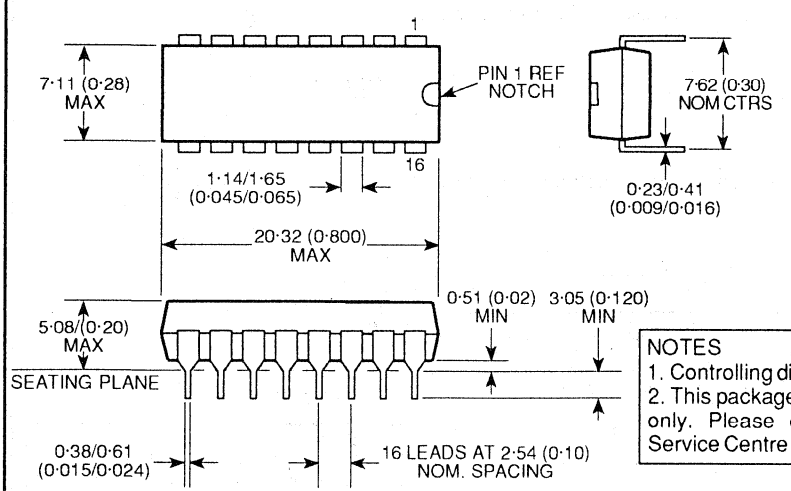
NOTES
1. Controlling dimensions are inches.
2. V_{DD} supply decoupling capacitors (C) are fitted in four places.
3. Plating bars can appear in various positions and must not be used for orientation purposes.
4. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

144-I/O PIN GRID ARRAY – AC144 (POWER)



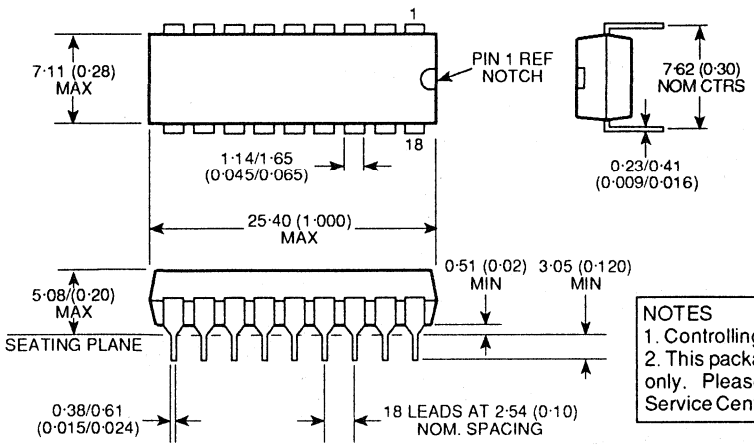
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

14-LEAD PLASTIC DIL – DP14



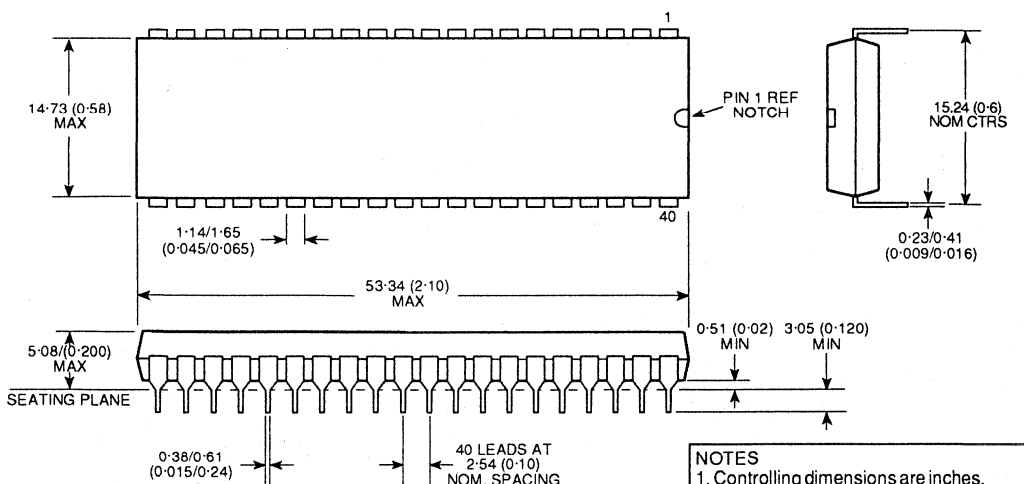
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

16-LEAD PLASTIC DIL – DP16



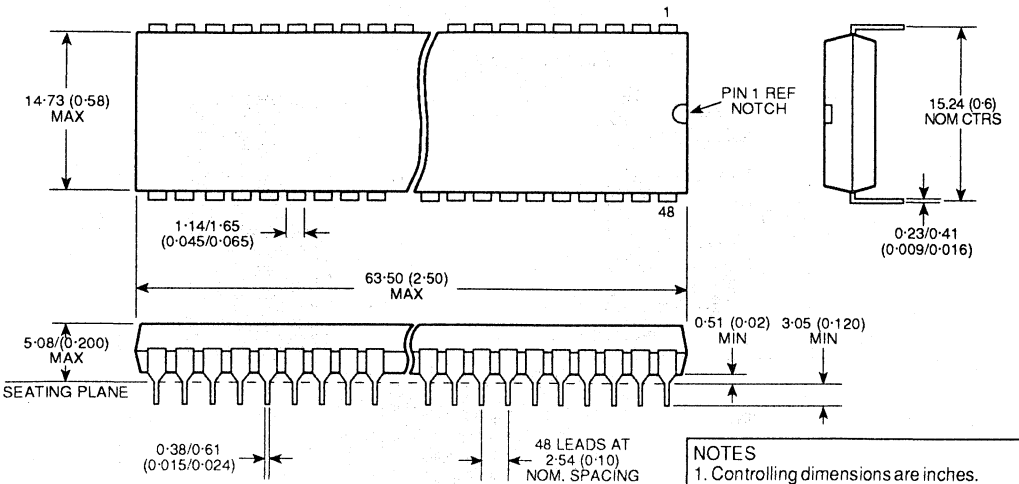
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

18-LEAD PLASTIC DIL – DP18



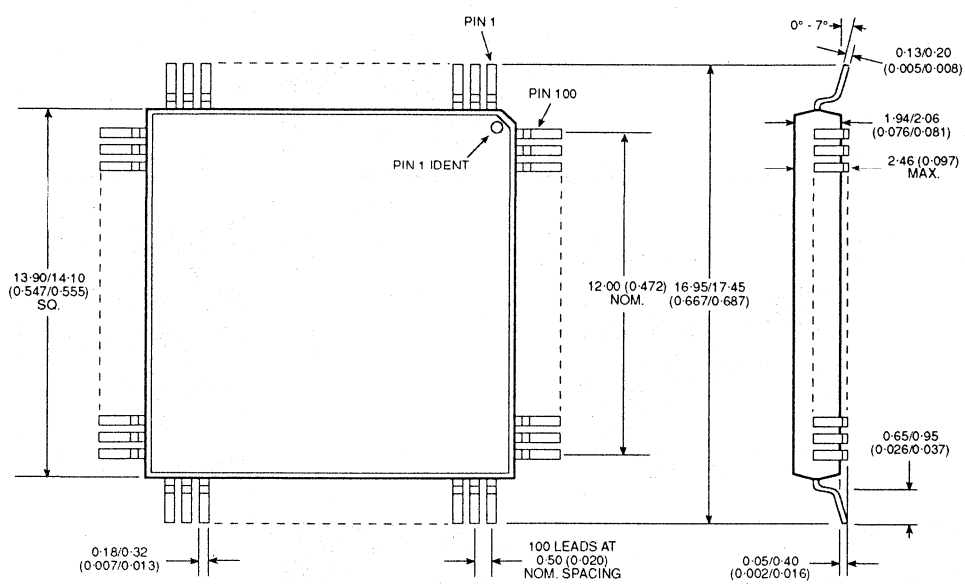
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

40-LEAD PLASTIC DIL – DP40



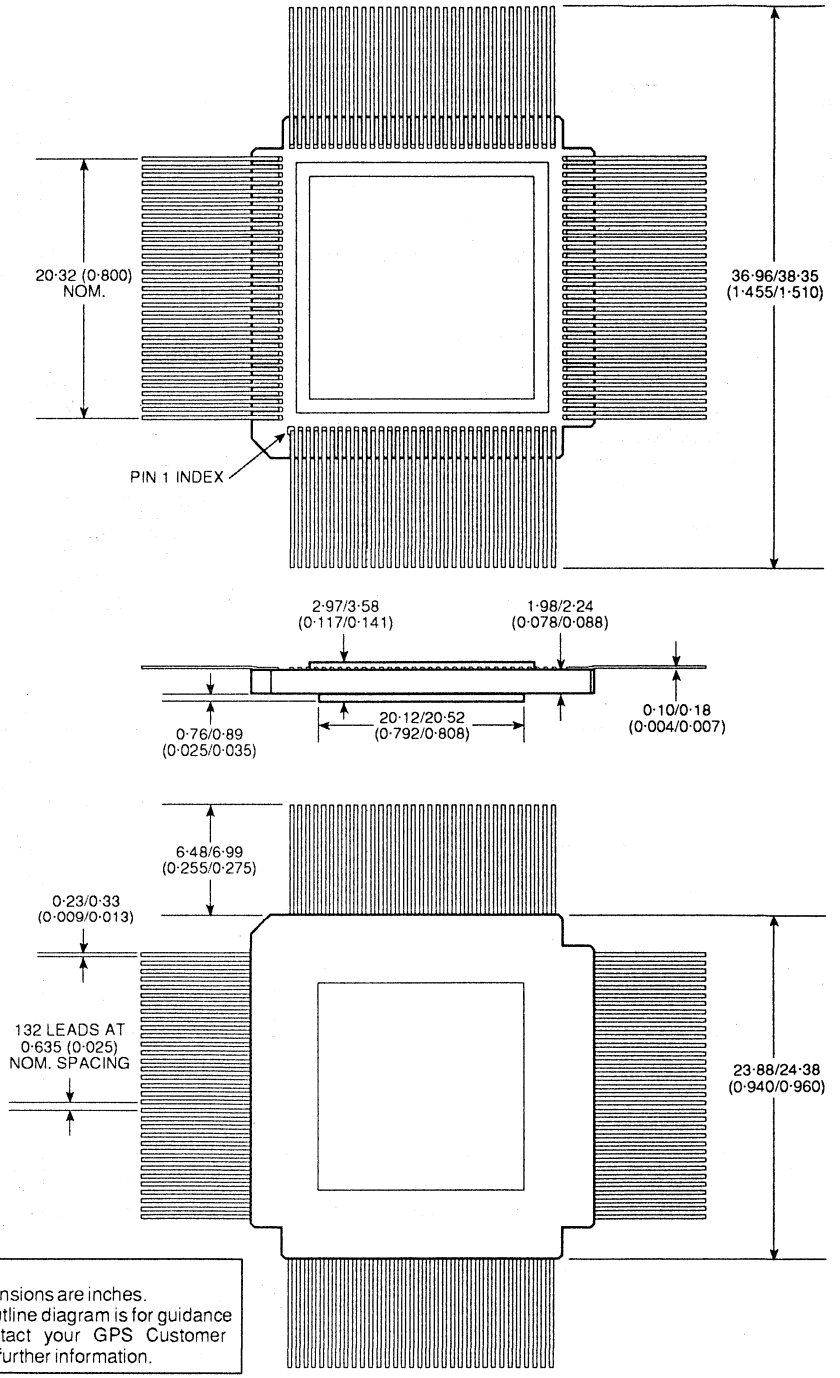
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

48-LEAD PLASTIC DIL – DP48



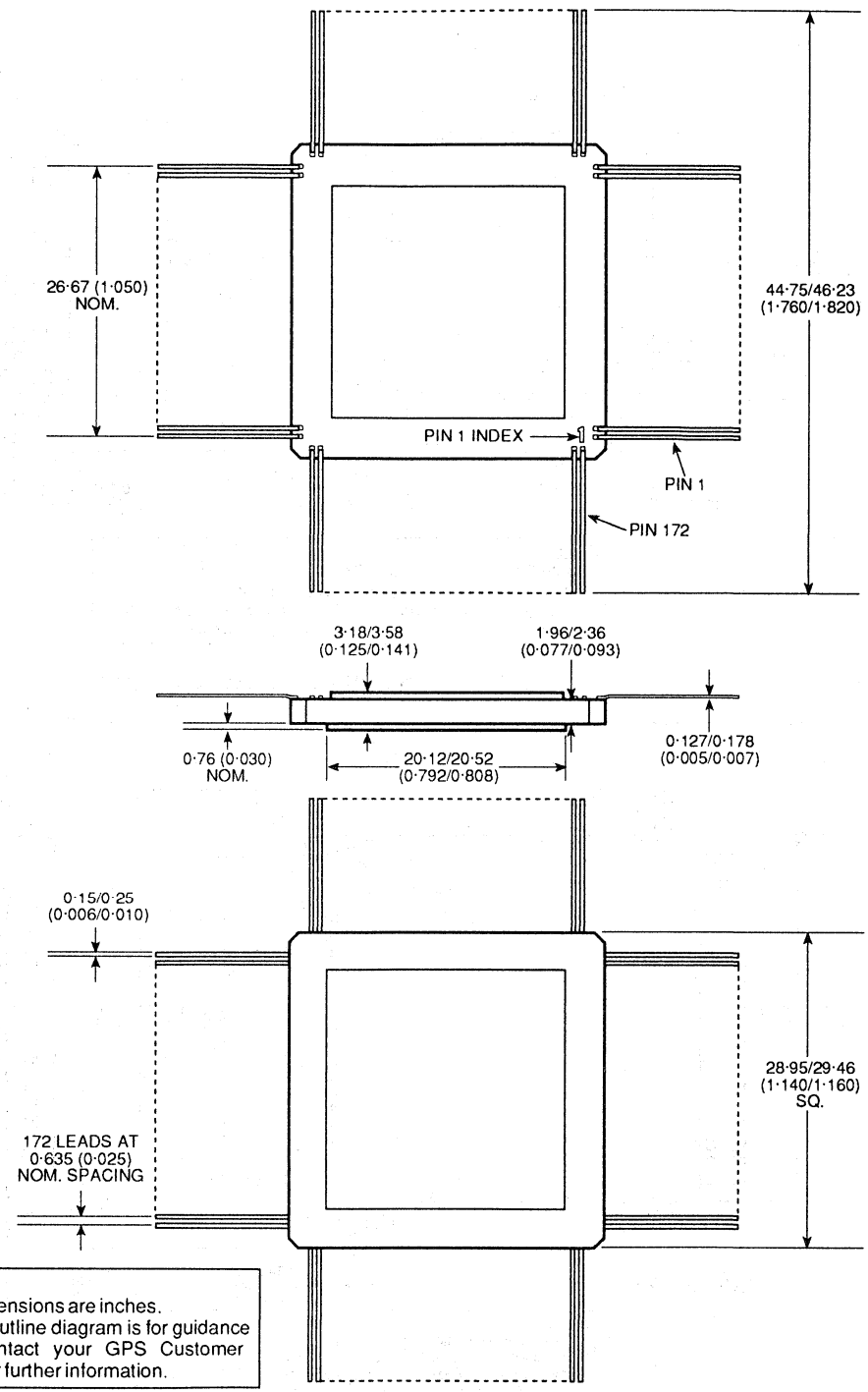
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

100-LEAD FINE PITCH PLASTIC QUAD FLATPACK – FP100



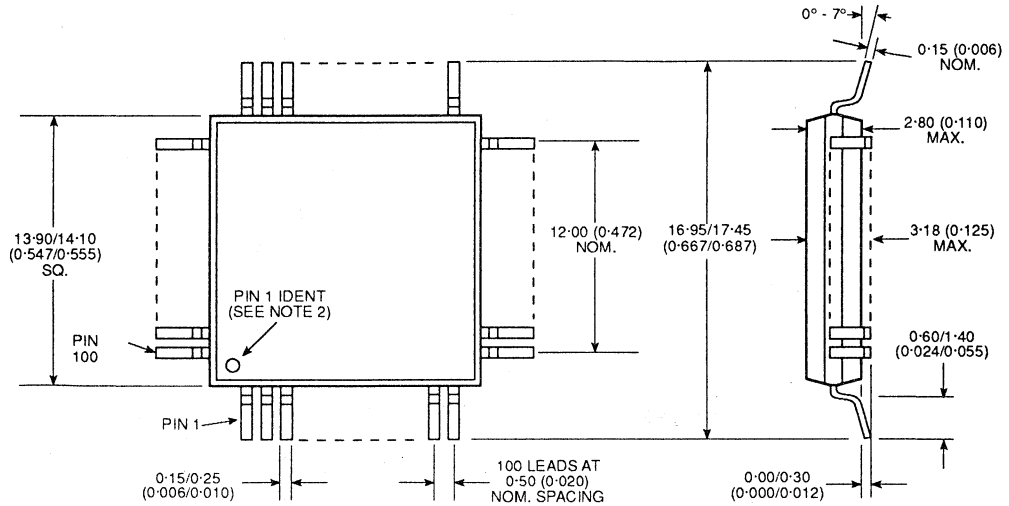
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

132-LEAD CERAMIC FLATPACK - GC132
(POWER PACKAGE)



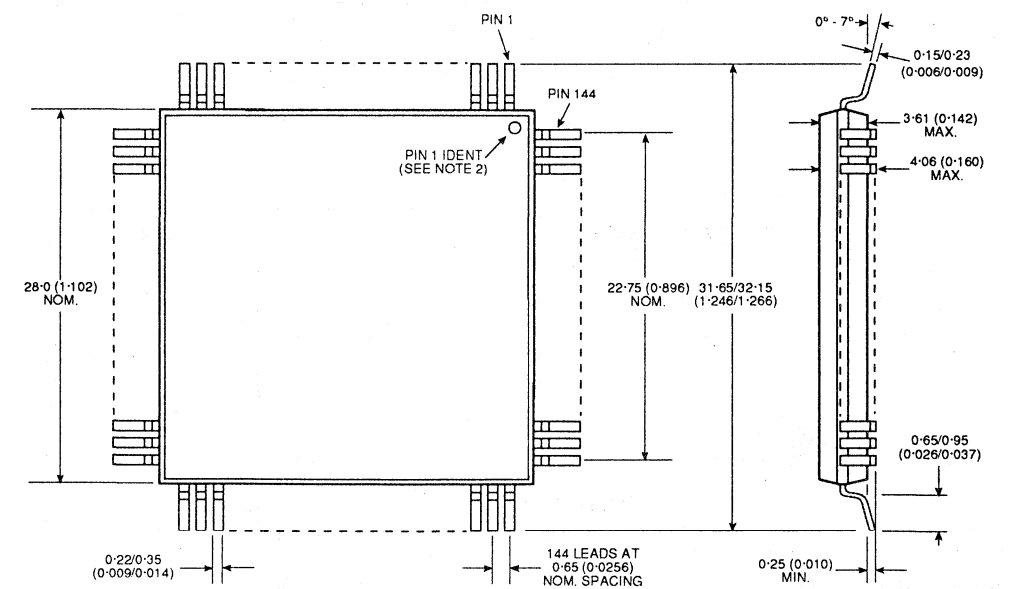
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

172-LEAD CERAMIC POWER FLATPACK - GC172 (POWER)



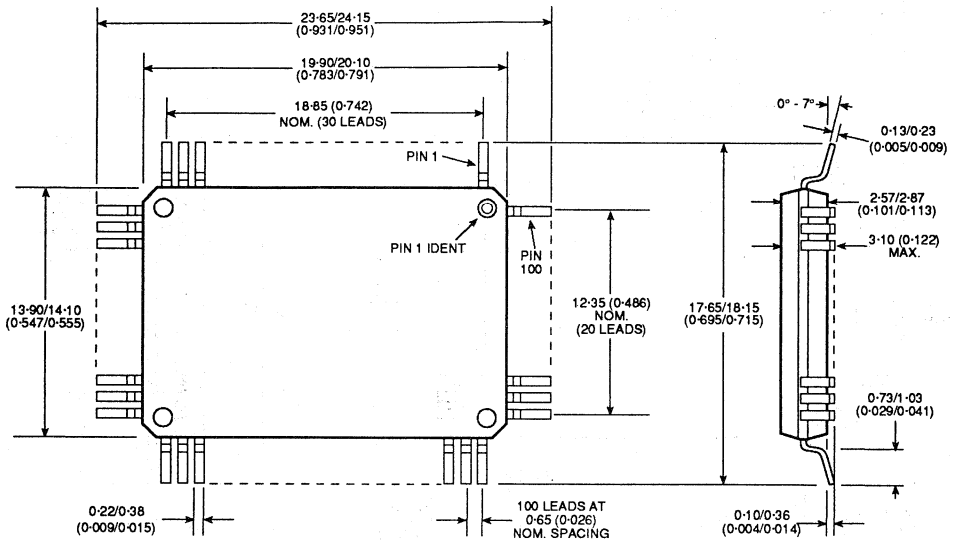
NOTES
1. Controlling dimensions are millimetres.
2. Pin 1 identification can be either a dot or a cut-out.
3. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

100-LEAD CERAMIC QUAD FLATPACK – GG100



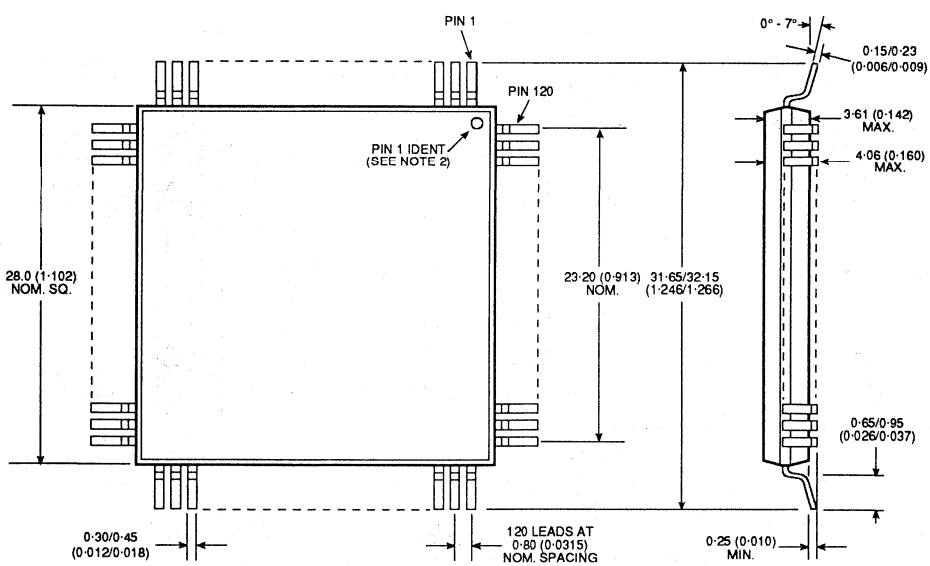
NOTES
1. Controlling dimensions are millimetres.
2. Pin 1 identification can be either a dot or a cut-out.
3. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

144-LEAD CERAMIC QUAD FLATPACK – GG144



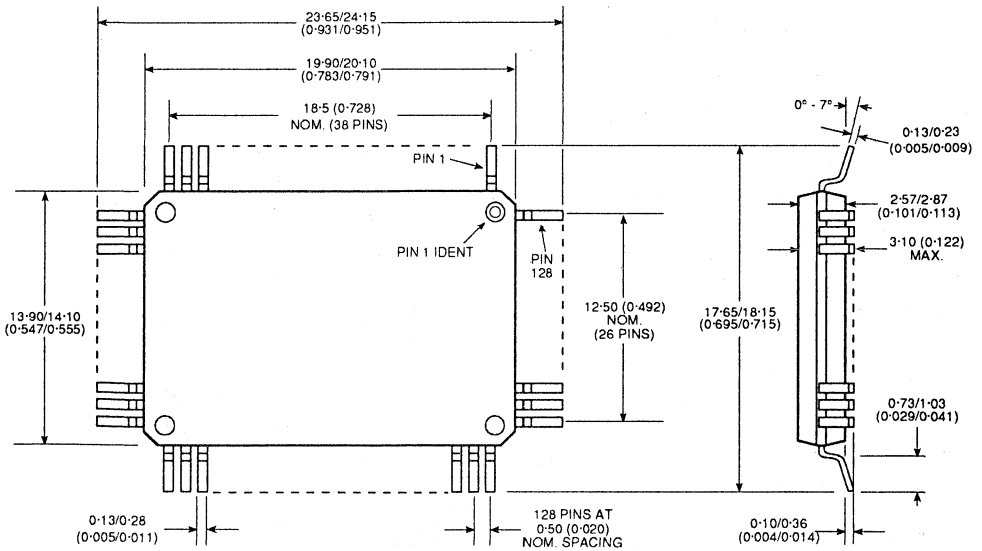
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

100-LEAD POWER PLASTIC QUAD FLATPACK (RECTANGULAR) – GH100/R



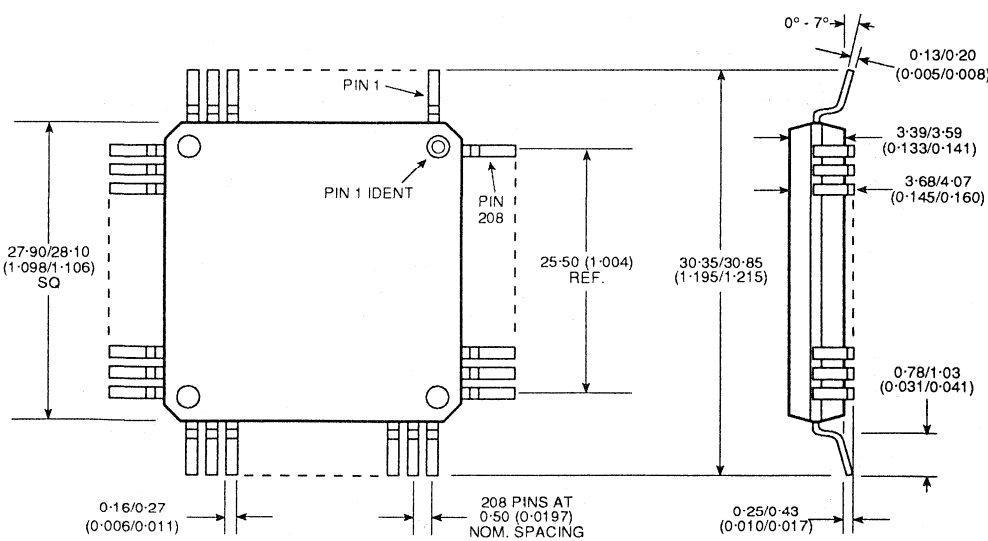
NOTES
1. Controlling dimensions are millimetres.
2 Pin 1 identification can be either a dot or a cut-out.
3. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

120-LEAD PLASTIC POWERQUAD FLATPACK - GH120



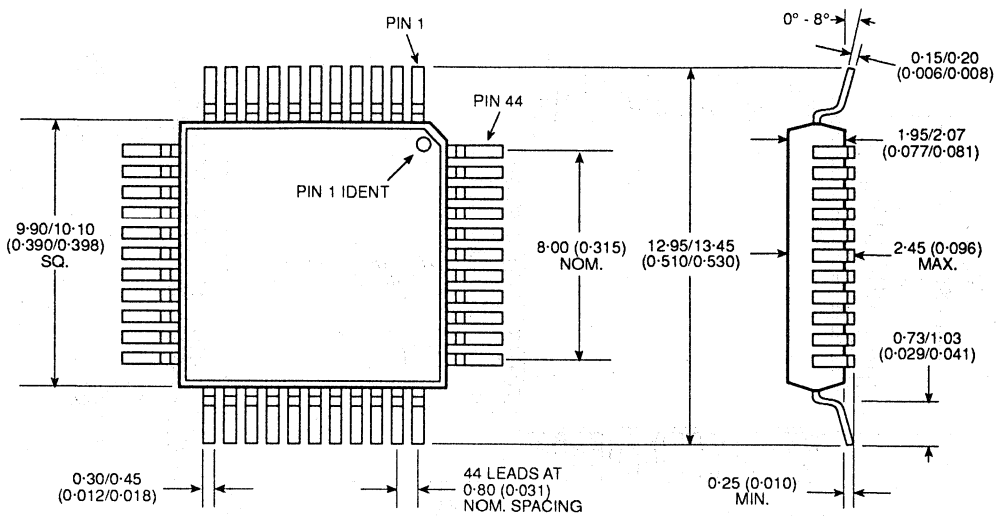
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

128-PIN POWER PLASTIC QUAD FLATPACK (RECTANGULAR) – GH128/R



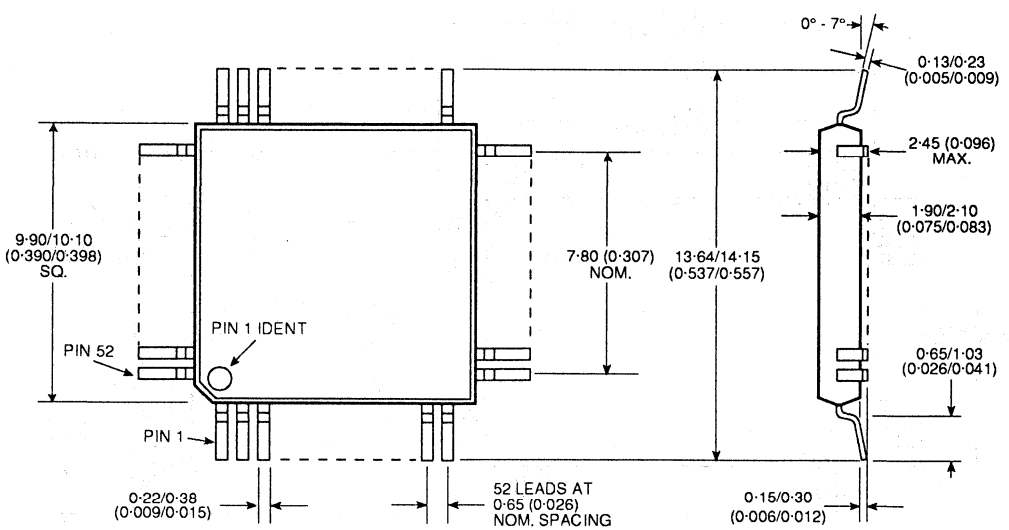
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

208-PIN POWER PLASTIC QUAD FLATPACK – GH208



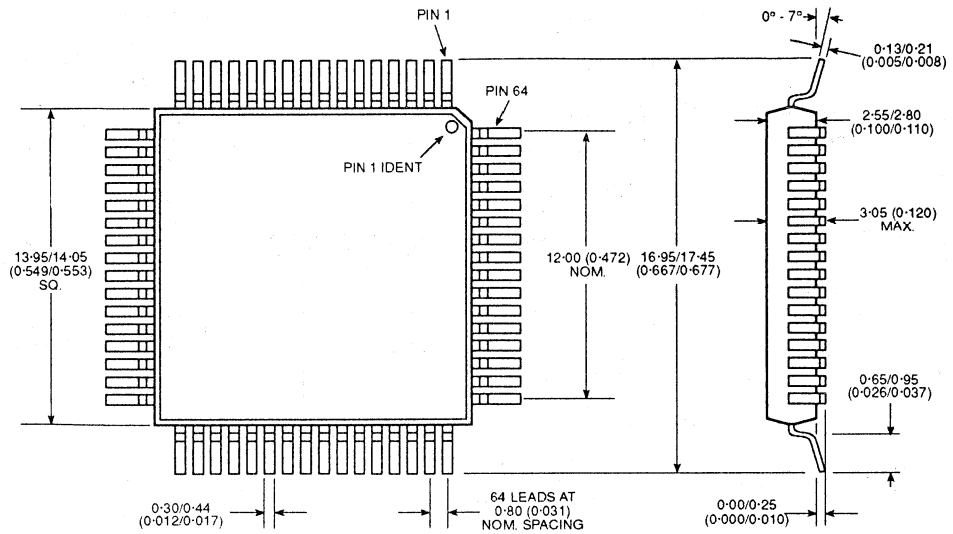
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GEC Plessey Semiconductors Customer Service Centre for further information.

44-LEAD PLASTIC QUAD FLATPACK – GP44



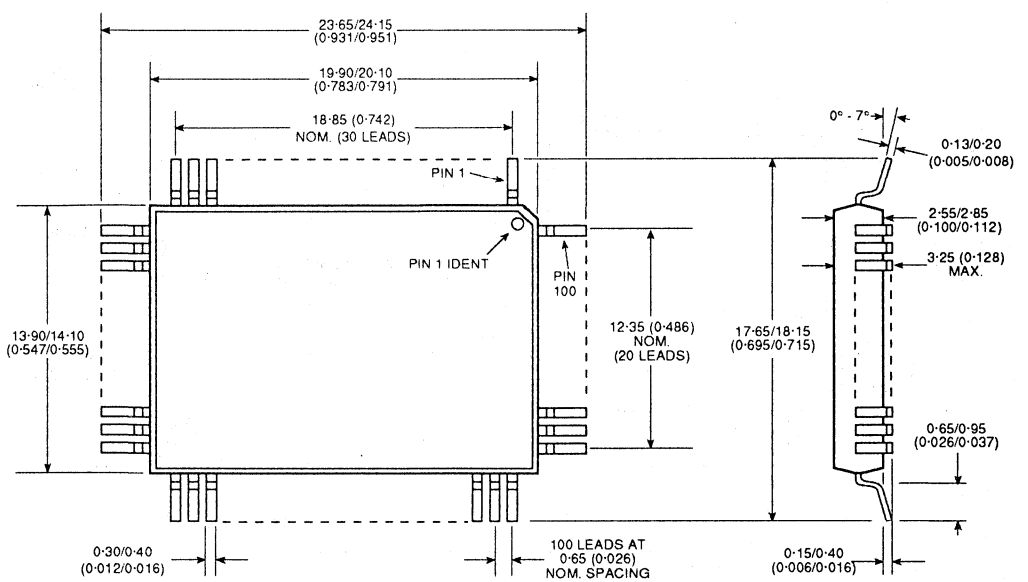
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

52-LEAD QUAD FLATPACK – GP52



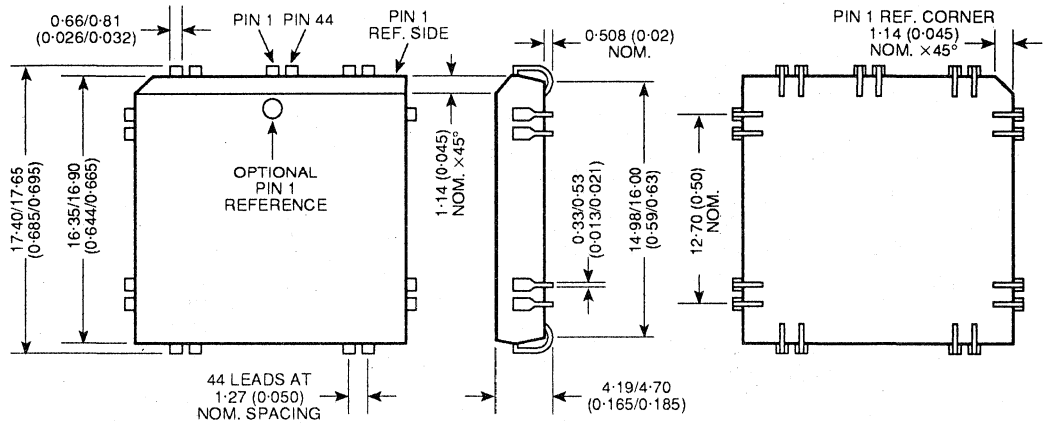
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

64-LEAD PLASTIC QUAD FLATPACK – GP64



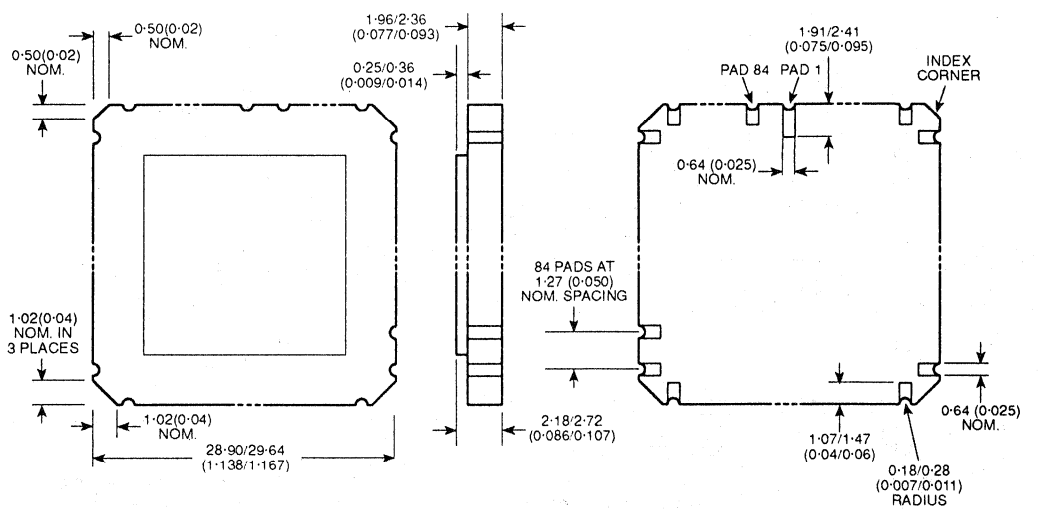
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

100-LEAD PLASTIC QUAD FLATPACK (RECTANGULAR) – GP100/R



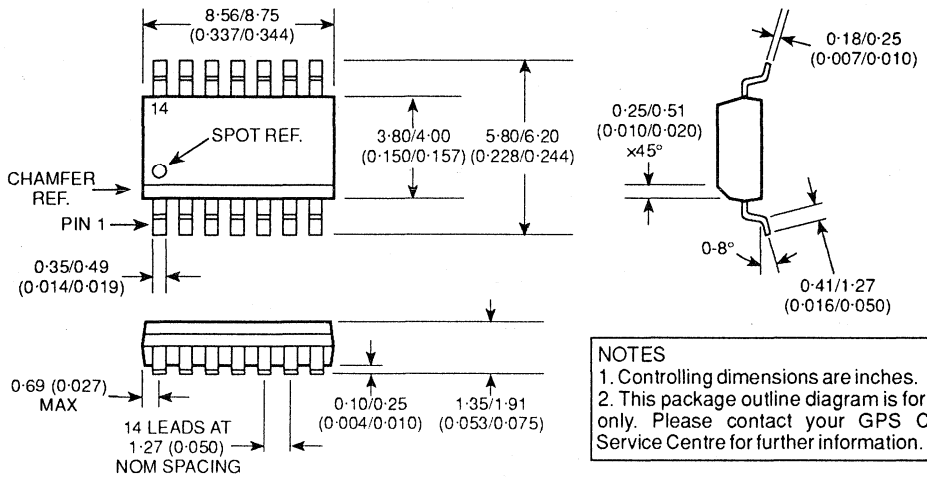
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

44-LEAD QUAD PLASTIC J-LEAD – HP44



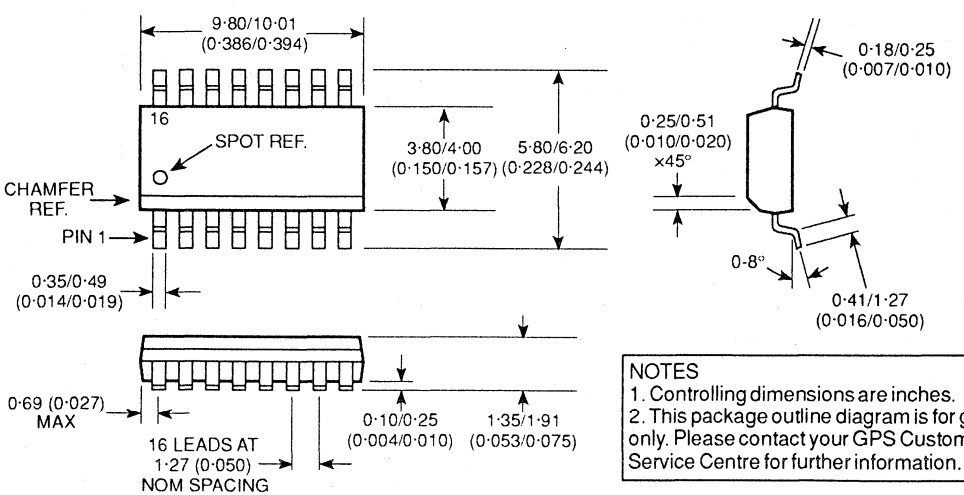
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

84-PAD SQUARE LEADLESS CHIP CARRIER – LC84



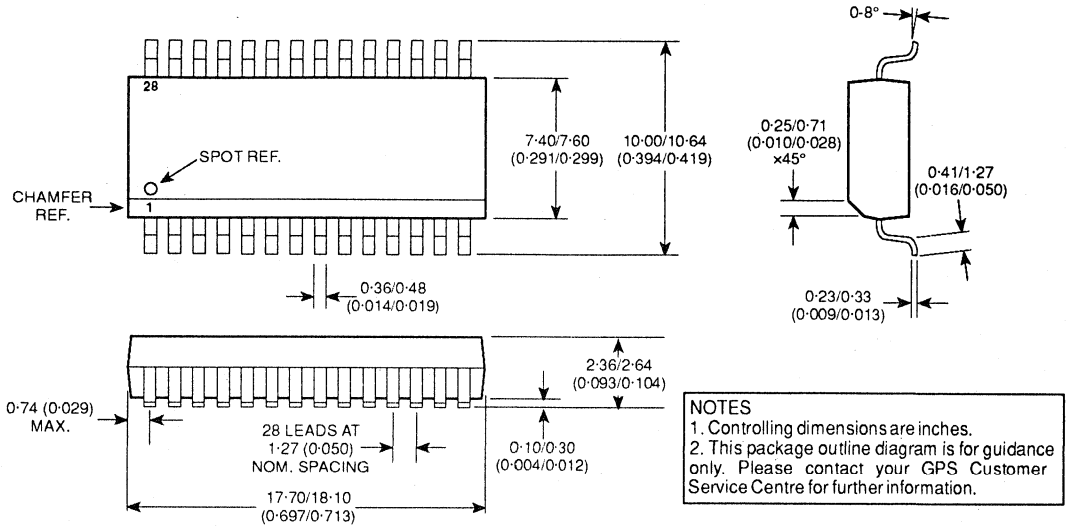
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

14-LEAD MINIATURE PLASTIC DIL - MP14



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

16-LEAD MINIATURE PLASTIC DIL - MP16



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

28-LEAD MINIATURE PLASTIC DIL - MP28

Section 12
GPS Locations

GEC PLESSEY
SEMICONDUCTORS

GPS Locations

Key: CS = Customer Services, D = Distributor, PO = Power Products Only, R = Representative, SD = ASIC Design.

FRANCE & BENELUX

CS SD **GEC Plessey Semiconductors,** Z.A. Courtaboeuf, Miniparc 6, Avenue des Andes, Bât. 2-BP 142, 91944, Les Ulis Cedex A. **France.** Tel: (1) 69 18 90 00. Fax: (1) 64 46 06 07.

CS PO **GEC Plessey Semiconductors,** 2 rue Henri-Bergson, 92665 Asnieres Cedex, **France.** Tel: (1) 40 80 54 00. Fax: (1) 40 80 55 87 ■ Griensven 10, Den Dungen, (N. Br.), 5275KE, **Netherlands.** Tel: 73 594 1107. Fax: 73 594 1119.

D **Omnitech Sertronique, France:** C.A. de Monthéard, 11 rue Edgar Brandt, 72016 Le Mans CEDEX. Tel: 43 86 74 74. Fax: 43 86 74 86 ■ 165 boulevard de Valmy, Evolic Batiment 1, 92706 Colombes. Tel: 1 46 13 07 80. Fax: 1 46 13 07 90 ■ Z.I. Prairie de Mauves, 64, Rue de l'Etrier, BP7405, 44074 Nantes CEDEX 03. Tel: 40 49 90 90. Fax: 40 68 06 72 ■ 99 boulevard de l'Artillerie, 69007 Lyon. Tel: 72 73 11 87. Fax: 72 73 18 00 ■ 37 rue Saint-Eloi, 76000 Rouen. Tel: 35 88 00 38. Fax: 35 15 06 22 ■ 20 rue Cabanis, 59041 Lille. Tel: 20 43 96 44. Fax: 20 56 00 49 ■ Parc Cadera Sud, Batiment F, 33700 Bordeaux Merignac. Tel: 56 34 46 00. Fax: 56 34 47 13.

D **3D, France:** 6-8 rue Ambroise Croisat, Z.I. des Glaises, 91120 Palaiseau. Tel: 1 64 47 29 29 Fax: 1 64 47 00 84 ■ 3 rue Berthelot, 69627 Villeurbanne CEDEX. Tel: 72 35 22 00. Fax: 72 34 67 72 ■ Z.I. du terroir, rue de l'industrie, 31140 Saint Alban. Tel: 61 37 44 00. Fax: 61 37 44 29 ■ Parc Club du golf, Batiment 1, 13856 Aix-en-Provence CEDEX 3. Tel: 42 16 77 88. Fax: 42 39 4728 ■ 1 rue de la Faisandereie, Bat B1 P.C. de Tanneries, F-67883 Tanneries CEDEX. Tel: 88 77 26 46. Fax: 88 76 13 30 ■ 6 rue Abbe Henri Gregoire, F-35000 Rennes. Tel: 99 32 44 33. Fax: 99 51 33 93 ■ 22 rue de Sedin, F-59175 Vendeville. Tel: 20 62 07 67. Fax: 20 62 07 66.

D **Tekelec-Airtronic BV,** PO Box 7140, NL-2701 Zoetermeer, **Netherlands.** Tel: 079-3461430. Fax: 079-3417504

D **ACAL NV,** Lozenberg 4, B-1932 Zaventem, **Belgium.** Tel: (2) 7205983. Fax: (2) 7254815.

PO R **Manudax NV,** Avenue Du Laerbeeklaan 74, 1090 Bruxelles, **Belgium.** Tel: 02 477 9322. Fax: 02 477 9320.

GERMANY, AUSTRIA & SWITZERLAND

CS SD **GEC Plessey Semiconductors,** Ungererstraße 129, 80805 München, **Germany.** Tel: 089/36 0906-0. Fax: 089/36 0906-55

D **AS Electronic Vertriebs GmbH,** In den Gaerten 2, D-61352 Bad Homburg, **Germany.** Tel: 06172 458931. Fax: 06172 42000.

D **Farnell Electronic Services GmbH,** Bahnhofstrasse 44, D-71696 Moeglingen, **Germany.** Tel: 071 41 4870. Fax: 07141 487210.

D **Micronetics GmbH,** Dieselstrasse 12, D-71272 Renningen, **Germany.** Tel: 07159 925830. Fax: 07159 9258355.

D **Welsbauer Elektronik GmbH,** Heiliger Weg 1, D-44135 Dortmund, **Germany.** Tel: 0231 579547. Fax: 0231 577514.

D **Eurodis Electronics GmbH,** Lamezanstrasse 10, A-1232 Wien, **Austria.** Tel: 1 610620. Fax: 1 61062151.

PO R **Novatronic GmbH,** Goergengasse 27/5, A-1190 Wien, **Austria.** Tel: 1 325 548. Fax: 1 325 513.

D **Basix AG,** Hardturmstr 181, CH-8010 Zuerich, **Switzerland.** Tel: 1 2761111. Fax: 1 2761234.

PO R **Schiesser Electronic AG,** Industrievertretungen, Hardstrasse 41, CH-5430 Wettingen, **Switzerland.** Tel: 056 4271 127. Fax: 056 4272 525.

ITALY

CS **GEC Plessey Semiconductors,** Via Fosse Ardeatine, N4, 20092 Cinisello Balsamo (MI). Tel: (02) 6607151. Fax: (02) 66040993.

D **Avnet EMG. S.r.l., Divisione Adelsy,** Via Novara 570, 20153 Milano. Tel: 02 381901. Fax: 02 38002988.

D **Eurelettronica SpA,** Via E. Fermi 8, 20090 Assago (MI). Tel: 02 457841. Fax: 02 4880275.

D **Eurodis Fanton Srl,** Via Melegnano, 22, 20019 Settimo Milanese (MI). Tel: 02 48912963. Fax: 02 4597913.

PO R **Sisram SpA,** Casella Postale 1168, 10100 Torino. Tel: 011 4331782/3/4. Fax: 011 4336521.

JAPAN

CS SD **GEC Plessey Semiconductors,** CTS Kojimachi Building (4th Floor), 2-12, Kojimachi, Chiyoda-ku, Tokyo 102. Tel: (03) 5276-5501. Fax: (03) 5276-5510.

D **Cornes & Company Ltd:** Ryukakusan Building, 2-5-12, Higashi Kanda, Chiyoda-ku,Tokyo 101. Tel: 3-5821-1628. Fax: 3-5821-1632 ■ 1-13-40 Nishi-hommachi, Nishi-ku, Osaka 550. Tel: 6 532 1012. Fax: 6 532-7749.

KOREA

CS **GEC Plessey Semiconductors,** 4th Floor, Cheonwoo Building, 736 Yogsam-Dong, Kangnam-Ku, Seoul 135-080. Tel: (2) 5668141. Fax: (2) 5697933

D **KML Corporation,** 6th Floor, Dukmyung Building, (A-Dong) 113-3, Banpo-Dong, Shucho-Gu, CPO Box 7981, Seoul. Tel: (02) 595 9101-6. Fax: (02) 595 9107.

PO R **Bochang Trading Corporation,** Room 1616, Samkoo Building, 16-49, Hangangro 3 Ka, Yongsan-Ku, Seoul. Tel: (02) 705 0890. Fax: (02) 705 1891.

		GEC Plessey Semiconductors, P O Box 660017, 1500 Green Hills Road, Scotts Valley, CA 95067-0017, **USA.** Tel: (408) 438 2900. Fax: (408) 438 7023
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CS SD		**GEC Plessey Semiconductors,** 2600 Michelson Drive, Suite 830, Irvine, CA 92715, **USA.** Tel: (714) 852-3900. Fax: (714) 852-3910 ■ 1735 Technology Drive, Suite 240, San Jose, CA 95110, **USA.** Tel: (408) 451-4700. Fax: (408) 451-4710 (CS)/(408) 451-4715 (SD) ■ 3 Allied Drive, Suite 125, Dedham, MA 02026, **USA.** Tel: (617) 251-0100. Fax: (617) 251-0104/PO: (617) 251-0106 (CS)/(617) 251-0105 (SD).
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